

STRUCTURES AND METHODS TO MINIMIZE PLASMA CHARGING DAMAGE IN SILICON ON INSULATION DEVICES

ABSTRACT

An SOI circuit configuration for minimizing plasma-induced charging damage during fabrication comprises charge collectors connected to a gate electrode and a semiconductor body, in which each one of the charge collectors have substantially the same shape and dimension. A connecting structure formed between a device fabrication on an SOI substrate and the substrate is delayed until the latter stages of processing.

(Fig. 5)



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