

Abstract of the Disclosure

A scan testing technique in which test data is pipelined to scan logic within
5 an integrated circuit. In system on a programmable chip (SOPC) designs, pipelines
are easily built in the programmable logic device (PLD) logic by configuring
programmable interconnects to connect registers in a pipelined manner so that test
data can be pipelined to scan the logic under test. In system on a chip (SOC)
designs, a smart test generator-analyzer is configured to recursively extract pipeline
10 information from a design so that test data can be pipelined to scan the logic under
test. Generally, test data is pipelined using existing functional logic and/or scan
chains. Furthermore, a failure analysis (FA) platform is described. The FA
platform is operable to take as its input a failing vector as well as a pipelined scan
vector and unroll the pipeline sequence to determine which vector caused the
15 failure.

Fig. 3