A METHOD OF FABRICATING A WAFER WITH STRAINE LAYERS FOR INCREASED ELECTRON AND HOLE MOBILITY FOR IMPROVING DEVICE PERFORMANCE

ABSTRACT

A method for making a SOI wafer with a strained silicon layer for increased electron and hole mobility is achieved. The method forms a porous silicon layer on a seed wafer. A H_2 anneal is used to form a smooth surface on the porous silicon. A strain free (relaxed) epitaxial Si_xGe_{1-x} layer is deposited and a bonding layer is formed. The seed wafer is then bonded to a handle wafer having an insulator on the surface. A spray etch is used to etch the porous Si layer resulting in a SOI handle wafer having portions of the porous Si layer on the relaxed Si_xGe_{1-x}. The handle wafer is then annealed in H_2 to convert the porous Si to a smooth strained Si layer on the relaxed SiGe layer of the SOI wafer.

FIG. 5