

DEVICES WITH CAVITY-DEFINED GATES AND METHODS OF MAKING THE SAME

Field of Invention

[0001] Embodiments of the present invention relate generally to electronic devices and, more specifically, in certain embodiments, to fin field-effect transistors.

Description of Related Art

[0002] Fin field-effect transistors (finFETs) are often built around a fin (e.g., a tall, thin semiconductive member) rising generally perpendicularly from a substrate. Typically, a gate traverses the fin by conformally running up one side of the fin, over the top, and down the other side of the fin. In some instances, the gate is disposed against the sides of the fin and does not extend over the top. Generally, a source and a drain are located on opposite sides of the gate near the ends of the fin. In operation, a current through the fin between the source and drain is controlled by selectively energizing the gate.

[0003] Some finFETs include gates formed with a sidewall-spacer process. In some versions of this process, the gates are formed by covering a fin with a conformal, conductive film and, then, anisotropically etching the conductive film. During the etch, the conductive material is removed faster from the horizontal surfaces than from the vertical surfaces. As a result, a portion of the conductive material remains against the vertical sidewalls of the fins, thereby forming the gate. An advantage of this process is that relatively narrow gates can be formed relative to gates patterned with photolithography, which is often subject to alignment and resolution constraints.

[0004] Although forming gates with a sidewall-spacer process avoids some process issues, it can introduce other failure mechanisms. Often the sidewalls of the fins are angled rather than vertical because the fins were formed with an etch step that was less than perfectly anisotropic. These angled sidewalls can narrow, and in some cases close, the process window for the sidewall spacer process. The angles place the bases of adjacent fins closer to one another, and when the conformal film is deposited in this narrower gap, the portions of the film covering the adjacent sidewalls can join, creating a film with a larger vertical thickness in the gap. The film can become so thick in the gap that the sidewall-spacer etch does not remove all of the conductive film between adjacent gates. The resulting conductive residue forms stringers that short adjacent finFETs and lower yields.

BRIEF DESCRIPTION OF DRAWINGS

[0005] FIGS. 1-24 illustrate an example of a manufacturing process in accordance with an embodiment of the present technique.

DETAILED DESCRIPTION

[0006] Some of the problems discussed above may be mitigated by certain embodiments of a new manufacturing process. In one embodiment described below, gates are formed in insulated caverns along the sides of fins. The caverns of this embodiment are constructed by forming a carbon mold in the shape of the gates, covering the carbon mold with an insulator, and then removing the carbon mold from under the insulator by combusting the mold. The resulting cavities are then at least partially filled with a gate insulator and a conductive gate material to form transistors. Because the cavities are insulated from one another before the gates are formed, the gates are believed to be less likely to short to other gates. This process and others are described below with reference to FIGS. 1-24.

[0007] As illustrated by FIG. 1, the manufacturing process begins with providing a substrate 110. The substrate 110 may include semiconductive materials such as single crystal or poly-crystalline silicon, gallium arsenide, indium phosphide, or other materials with semiconductor properties. Alternately, or additionally, the substrate 110 may include a non-semiconductor surface on which an electronic device may be constructed such as a plastic or ceramic work surface, for example. The term “substrate” encompasses bodies in a variety of stages of manufacture, including an unprocessed whole wafer, a partially-processed whole wafer, a fully-processed whole wafer, a portion of a diced wafer, or a portion of a diced wafer in a packaged electronic device.

[0008] In this embodiment, the substrate 110 includes an upper doped region 112 and a lower doped region 114. The upper doped region 112 and the lower doped region 114 may be differently doped. For example, the upper doped region 112 may include an n+ material and the lower doped region 114 may include a p- material. The depth of the upper doped region 112 may be generally uniform over a substantial portion of the substrate 110, such as throughout a substantial portion of an array area of a memory device, for example. The upper doped region 112 and lower doped region 114 may be formed by implanting or diffusing dopant materials. Alternatively, or additionally, one or both of these regions 112 and/or 114 may be doped during growth or deposition of all or part of the substrate 110, such as during epitaxial deposition of a semiconductive material or during growth of a semiconductive ingot from which wafers may be cut. As explained below, the upper doped region 112 may provide material used to form a source and a drain of a transistor, and the lower doped region 114 may provide material used to form a channel of the transistor.

[0009] Next, a deep trench mask 116 is formed, as illustrated by FIG. 2, and deep isolation trenches 118 are etched, as illustrated by FIG. 3. The deep trench mask 116 may be

photoresist or a hard mask, and the deep trench mask 116 may be patterned with photolithography equipment or other types of lithographic equipment, such as a nano-imprint system or an electron beam system. The deep trench mask 116 includes generally linear and generally parallel exposed regions with a width 120 generally equal to or less than $1/4 F$, $1/2 F$ or F and masked regions with a width 122 generally equal to or less than $3/4 F$, $3/2 F$, or $3 F$, where F is the resolution of the system used to pattern the deep trench mask 116.

[00010] In some embodiments, the deep trench mask 116 is formed by double pitching a mask (not shown). In one example of such a process, the deep trench mask 116 is formed first by masking off the areas between every other pair of exposed regions and, then, forming a poly-silicon sidewall spacer on the sides of the mask, over the areas corresponding to each of the exposed regions. Then the initial mask may be removed and a hard mask material, such as oxide, may be deposited over the remaining poly-silicon sidewall spacers, and the hard mask material may be etched back or planarized with chemical mechanical planarization (CMP) to expose the poly-silicon. Next, the poly-silicon may be selectively etched to form the exposed regions the oxide hard mask illustrated by FIG. 2. Because the width 122 of the exposed regions is generally defined by the width of a sidewall spacer, in some embodiments, the width 122 may be smaller than F .

[00011] As illustrated by FIG. 3, the regions of the substrate 110 exposed by the mask 116 may be etched to form the deep isolation trenches 118. In this embodiment, the etch is a generally anisotropic dry etch. The deep isolation trenches 118 may generally extend laterally in the Y direction and downward in the Z direction. The deep isolation trenches 118 may have a generally rectangular or trapezoidal cross-section, and, in some embodiments, their cross-section may be generally uniform through some distance in the Y-direction.

[00012] Next in the present embodiment, the deep trench mask 116 is removed, and the deep isolation trenches 118 are filled with a dielectric, as illustrated by FIG. 4. The deep trench mask 116 may be removed with a variety of techniques, such as reacting photoresist with oxygen in a furnace or in a plasma etch chamber or selectively wet etching the mask material. In some embodiments, the deep trench mask 116 is removed after filling the deep isolation trenches 118. In others, deep trench mask 116 may be removed prior to filling the deep isolation trenches 118. For example, a dielectric overburden may be deposited both over the deep trench mask 116 and in the deep isolation trenches 118, and the deep trench mask 116 may serve as a stop region during chemical-mechanical planarization (CMP) to remove the overburden. The deep isolation trenches 118 may be partially or entirely filled with various dielectric materials, such as high-density-plasma (HDP) oxide, spun-on-glass (SOG), or tetra-ethyl-ortho-silicate (TEOS), among others, to electrically isolate features. To further isolate features, in some embodiments, the bottom of the deep isolation trenches 118 may be implanted with a dopant selected to enhance isolation prior to filling the trenches 118. Additionally, the deep isolation trenches 118 may include various liner materials, such as silicon nitride for example, to relieve film stresses, improve adhesion, or function as a barrier material.

[00013] After filling the deep isolation trenches 118, a shallow trench mask 124 is formed on the substrate 110, as illustrated by FIG. 5. As with the deep trench mask 116, the shallow trench mask 124 may be photoresist or a hard mask, and it may be patterned with various lithographic systems, such as those discussed above. In some embodiments, the shallow trench mask 124 is a hard mask formed with a double-pitched-mask process similar to the process described above for the isolation trench mask 116, except that this mask is shifted in the X direction by $1/2$ pitch. The illustrated shallow trench mask 124 includes exposed regions with a space 126 that may have a width generally equal to or less than $1/4$ F, $1/2$ F or F and covered

regions with a width 128 that may be generally equal to or less than $3/4 F$, $3/2 F$, or $3 F$. The exposed regions may be generally linear, generally parallel, and interposed generally equidistant between the deep isolation trenches 118.

[00014] Next, the exposed regions of the substrate 110 may be etched to form shallow trenches 130, as illustrated by FIG. 6. The shallow trenches 130 may be generally linear, generally parallel, generally extend generally laterally in the Y direction and generally downward in the Z direction, and thus, may be generally parallel to the deep isolation trenches 118. In this embodiment, the shallow trenches 130 are formed with a generally anisotropic dry etch and are deeper than the upper doped region 112, but not as deep as the deep isolation trenches 118. The shallow trenches 130 may have a generally rectangular or generally trapezoidal profile that is generally uniform in the Y direction over a substantial distance.

[00015] As illustrated by FIG. 7, the shallow trenches 130 are filled with a sacrificial material, such as nitride. In this embodiment, the shallow trenches 130 are filled with a different material from the deep isolation trenches 118 so that the shallow trenches 130 can be selectively etched in a subsequent step without removing substantial amounts of material from the deep isolation trenches 118. In other embodiments though, these trenches 118 and 130 may include the same material.

[00016] Next, a fin mask 132 is formed, as illustrated by FIG. 8. The fin mask 132 may be made of photoresist, or it may be a hard mask. The fin mask 132 may be patterned with any of the lithographic systems described above or others. In this embodiment, the fin mask 132 defines a masked region with a width 134 and exposed regions with a width 136. The width 134 may be generally equal to or less than F , and the width 136 may be generally equal to or less than $3/2 F$. The masked regions may be generally straight, generally parallel to one another, and

are generally perpendicular to both the deep isolation trenches 118 and the shallow trenches 130, and generally extend in the X direction.

[00017] In some embodiments, the fin mask 132 is double pitched. Sidewall spacers 138 may be formed against the sidewalls of the fin mask 132, as illustrated by FIG. 9. The sidewall spacers 138 may be formed by depositing a conformal film on the substrate 110 and anisotropically etching the conformal film to remove it from the horizontal surfaces. The sidewall spacers 138 may be made of a different material from the fin mask 132 to facilitate selective removal of the fin mask 132 in a subsequent step. The sidewall spacers 138 may have a width 140 that is generally equal to or less than $1/4 F$, $1/2 F$, or F .

[00018] Next, the fin mask 132 is removed, as illustrated by FIG. 10, and fin rows 142 are formed, as illustrated by FIG. 11. The fin mask 132 may be removed with an etch or other process that selectively removes the fin mask material at a substantially higher rate than the other materials of the substrate 110. Each of the exposed sidewall spacers 138 may mask an area that generally corresponds with the top of the fin rows 142. In this embodiment, the fin rows 142 are etched with a generally anisotropic etch to a depth 144 that is generally greater than the depth of the shallow trenches 130, but not as deep as the deep isolation trenches 118. The fin rows 142 may have a generally trapezoidal cross-section that extends generally uniformly in the X direction over a substantial distance. In other embodiments, the fin rows 142 may have other profiles, such as generally rectangular or curved profiles.

[00019] Next, the spacers 138 may be removed, as illustrated by FIG. 12, or in some embodiments, the spacers 138 may be left on the fin rows 142 and removed during a subsequent step.

[00020] FIGS. 13 and 14 illustrate a sacrificial material 146 (which in this embodiment functions as, and may be referred to as a mold) that may be formed against the sidewalls of the fin rows 142. The sacrificial material 142 may be formed with a sidewall spacer process. Sacrificial material 142 may be formed from a material that may become flowable (e.g., it may become a fluid, such as a gas or a liquid) under procession conduction subsequently described with reference to FIG. 18. Examples of disposable-mold materials include carbon and certain polymers, both of which may be removed from the substrate 110 as a gas by reacting them with oxygen in a furnace. A conformal film may be deposited on the substrate 110, covering the upper doped region 112 and the lower doped region 114, and subsequently is anisotropically etched. The sidewall spacer etch may remove a portion of the lower doped region 114 to form recesses 148. The recesses 148 may have a width 150 generally equal to or less than $1 F$, $1/2 F$, or $1/4 F$. As explained below, continuing the sidewall spacer etch until it forms recesses 148 is believed to reduce the likelihood of gates formed with the molds 146 shorting to one another. In this embodiment, the sacrificial material 146 extends above the bottom of the upper doped region 112 and has a width 152 that may be less than or generally equal to $1 F$, $1/2 F$, or $1/4 F$.

[00021] After forming the sacrificial material 146, a dielectric region 154 may be formed over the sacrificial material 146, as illustrated by FIG. 15. In some embodiments, the dielectric region 154 may be an oxide deposited with a low-temperature process, such as atomic-layer-deposition (ALD). The illustrated dielectric 154 substantially or entirely envelops the sacrificial material 146 and includes an overburden 156.

[00022] The overburden 156 is consumed in a planarization step illustrated by FIG. 16. The substrate 110 may be planarized with an etch back, CMP, or other processes. In some embodiments, the overburden 156 may be removed until the top of the upper doped region 112, the deep isolation trench 118, and the shallow trenches 130 are exposed. The transition between

the dielectric region 154 and these structures 112, 118, and 130 may produce a phenomenon that triggers an endpoint to the process used to planarize the substrate 110. For example, this transition may yield a change in the optical properties of the substrate 110 (such as color), a change in the chemical properties of waste material leaving the substrate 110 (such as waste gases in an etch chamber or slurry pH), or a change in the mechanical properties of the substrate 110 (such as sliding friction).

[00023] Next, at least a portion of the material in the shallow trenches 130 may be removed, as illustrated by FIG. 17. In some embodiments, this material is a nitride, and it is removed with a dry etch that is selective against silicon and oxide to avoid losing substantial amounts of these materials. Clearing at least a portion of the shallow trenches 130 opens a passage to a sidewall 158 of the sacrificial material 146, and this passage may facilitate removal of the sacrificial material 146.

[00024] The sacrificial material 146 may be removed by way of the open passage through the shallow isolation trench 130, as illustrated by FIG. 18. To remove the sacrificial material 146, the substrate 110 may be exposed to an oxygen plasma, e.g., in a plasma etch chamber, or oxygen in a furnace. The plasma or other reactants flow in through the shallow isolation trench 130 and react with the sidewall 158 of the sacrificial material 146, e.g., by combusting the sacrificial material 146. In some embodiments, the byproducts of the reaction are gases, e.g. steam, carbon monoxide, and carbon dioxide, and the gases flow back out through the shallow isolation trench 130. In some embodiments, combustion continues until a substantial portion or substantially the entire sacrificial material 146 is burned and cavities 160 are formed. The resulting cavities 160 are bounded on one side by the dielectric 154 and on another side by the fin rows 142.

[00025] The shape of the cavities 160 is illustrated by FIG. 19, which illustrates cavities 160 without the other parts of substrate 110. Each of the cavities 160 may include two generally reflectively symmetric, generally linear, and generally parallel voids 162 and 164 and a plurality of trench segments 166. The illustrated trench segments 166 are disposed in a top portion of the voids 162 and 164 and join the voids 162 and 164 to one another. Adjacent cavities 160 may be substantially or entirely separated from one another by the dielectric 154 (FIG. 18).

[00026] Next, a gate dielectric 166 may be formed within the cavities 160, as illustrated by FIG. 20. The gate dielectric 166 may be either deposited, e.g., with CVD, or grown by exposing the substrate 110 to oxygen. In the illustrated embodiment, the gate dielectric 166 is grown by reacting silicon portions of the substrate 110 with oxygen, so the gate dielectric 166 is disposed on the exposed surfaces of the fin rows 142, including the surface of the shallow trench 130. The oxygen or other chemicals that react to form the gate dielectric 166 flow into the cavities 160 through the trench segments 166 and react with surfaces within the linear voids 162 and 164 (FIG. 19). In various embodiments, the gate dielectric 166 may be made from a variety of materials, including oxide, oxynitride, a hafnium-based high-k dielectric, or other appropriate materials.

[00027] Once the gate dielectric 166 is formed, gate material may be deposited within the cavities 166 to form gates 168, as illustrated by FIGS. 21, 22 and 23. The illustrated gates 168 may be formed by depositing titanium nitride or other appropriate conductive materials. The gate material may be conveyed to the substrate 110 and into the cavities 166 by gas-phase reactants. The reactants may flow into the cavities 166 through the shallow trench 130 and react on the surface of the cavities 166. In some embodiments, the gate material closes the shallow trench 130 before the cavities 166 are filled, thereby leaving voids 170. An overburden of gate

11

material may form on the surface of the substrate 110, and the overburden may be removed with a wet etch, a dry etch, or a CMP process.

[00028] FIG. 24 is an exploded, perspective view of an example of a transistor 171 formed with the above-described process. It should be noted, though, that the present technique is not limited to transistors and may be used to form other devices, such as capacitors or floating-gate transistors. The illustrated transistor 171 includes a fin 172, the gate dielectric 166, and the gate 168. The illustrated fin 172 includes two legs 174 and 176 separated by a generally U-shaped slot 178 corresponding with the shallow trench 130. A distal portion of the fin 172 is made from the upper doped region 112, and a lower portion of the fin 172 is made from the lower doped region 114. Edges 180 and 182 are generally defined by the deep isolation trenches 118 and may be longer than sides 184 and 185 of the fin 172. The illustrated gate 166 is disposed adjacent both the sides 184 and 185 and the surface of the slot 178.

[00029] In the illustrated embodiment, the gate 168 includes two side gates 186 and 188 and a top gate 190. The two side gates 186 and 188 are generally reflectively symmetric and both generally extend in the X direction with a generally uniform cross-section over a substantial distance. The shape of the side gates 186 and 188 is generally complementary to the shape of the sacrificial material 146 with the exception of the voids 170. The illustrated top gate 190 has a generally uniform cross-section in the Y direction and it joins the side gates 186 and 188 to one another. The top gate 190 may be generally solid, without a void, or in some embodiments, the top gate 190 may also include a void. The side gate 186 is disposed at least partially adjacent the side 185 of the fin 172, the top gate 190 is disposed at least partially within the slot 178, and the side gate 188 is disposed at least partially adjacent the side 184 of the fin 172. The illustrated transistor 171 may be characterized as a tri-gate transistor, because the gate 168 is disposed adjacent two sides and a top portion of the fin 172.

[00030] In operation, the two legs 174 and 176 may function as a source and a drain, and the transistor 171 may selectively control the flow of current between the source and the drain according to a voltage of the gate 168. The illustrated transistor 171 includes three channels: a generally horizontal channel represented by arrows 192 and two generally vertical channels represented by arrows 194. The generally horizontal channel 192 may be established by electric fields emanating from the top gate 190, and the generally vertical channels 194 may be established by electric fields emanating from the two side gates 186 and 188.

[00031] While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

CLAIMS

1. A device, comprising:
a fin row comprising a plurality of fin field-effect transistors, wherein each fin field-effect transistor comprises three channels;
a hollow gate disposed adjacent the fin row.
2. The device of claim 1, wherein the gate comprises a plurality of trench segments that cross through a distal portion of a plurality of the fin field-effect transistors.
3. The device of claim 1, wherein each fin field-effect transistor among the plurality of fin field-effect transistors comprises a generally U-shaped distal portion.
4. A device, comprising:
a fin row comprising a plurality of fin field-effect transistors; and
a hollow gate disposed adjacent the fin row,
wherein a fin width of each fin field-effect transistor among the plurality of fin field-effect transistors is less than the photolithographic-resolution limit.
5. A device, comprising:
a plurality of tri-gate transistors each comprising a top gate and two hollow side gates, wherein the top gate is at least partially disposed within a slot in a fin of the transistor; and
a plurality of dielectric members each disposed between the hollow side gates of adjacent tri-gate transistors, wherein the dielectric members extend into recesses deeper than the hollow side gates.

6. The device of claim 5, wherein the recesses are sidewall-spacer-over-etch recesses.
7. The device of claim 5, wherein the recesses are narrower than the photolithograph-resolution limit.
8. The device of claim 5, wherein at least one of the top gate or the two side gates are formed within a cavity.
9. The device of claim 8, wherein each of the top gate and the two side gates are formed within a cavity.
10. A device, comprising:
 - a fin comprising two legs; and
 - a gate, wherein the gate comprises:
 - a first hollow side gate formed along a first side of the fin;
 - a second hollow side gate formed along a second side of the fin, opposite the first side; and
 - a top gate formed on top of the fin.
11. The device, as set forth in claim 10, wherein a first of the two legs comprises a source of a transistor, and wherein a second of the two legs comprises a drain of the transistor.
12. The device, as set forth in claim 11, wherein the transistor comprises three channels.

13. The device, as set forth in claim 12, wherein a first of the three channels is generally horizontal, and wherein a second and third of the three channels are generally vertical.
14. The device, as set forth in claim 10, wherein the fin comprises a trench formed between each of the two legs.
15. The device, as set forth in claim 14, wherein the trench is generally U-shaped.
16. The device, as set forth in claim 10, wherein each of the first side gate, the second side gate and the top gate are electrically coupled to one another.