CLAIMS

1. A qubit comprising:

a substrate;

a first capacitor structure having a lower portion formed on a surface of the substrate and at least one first raised portion extending above the surface of the substrate;

a second capacitor structure having a lower portion formed on the surface of the substrate and at least one second raised portion extending above the surface of the substrate, the first capacitor structure and the second capacitor structure formed of a superconducting material;

a junction between the first capacitor structure and the second capacitor structure, the junction disposed at a predetermined distance from the surface of the substrate and having a first end in contact with one of the at least one first raised portion and a second end in contact with one of the at least one second raised portion; and

a cavity formed between the junction and the substrate.

2. The qubit of claim 1, wherein the junction is formed of an insulating material sandwiched between superconducting material.

3. The qubit of claim 2, wherein the superconducting material of the junction is aluminum.

4. The qubit of any one of the preceding claims, wherein the junction comprises a Josephson junction.

5. The qubit of any one of the preceding claims, wherein the superconducting material of the first capacitor structure and the second capacitor structure is Niobium (Nb) and the substrate comprises Silicon (Si).

6. The qubit of any one of the preceding claims, wherein the first capacitor structure and the second capacitor structure are of a trapezoidal shape.

7. A method comprising:

forming a first trench and a second trench in a substrate;

depositing a superconducting material layer upon a surface of the first trench and a surface of the second trench to form a first capacitor structure and a second capacitor structure, respectively, and wherein the first capacitor structure and the second capacitor structure are formed of a superconducting material;

forming a junction between the first capacitor structure and the second capacitor structure; and

removing a portion of the substrate to form a lower portion of the first capacitor structure on a surface of the substrate and at least one first raised portion of the first capacitor structure extending above the surface of the substrate, and a lower portion of the second capacitor structure on the surface of the substrate and at least one second raised portion extending above the surface of the substrate, wherein the junction is disposed at a predetermined distance from the surface of the substrate and having a first end in contact with one of the at least one first raised portion and a second end in contact with one of the at least one second raised portion.

8. The method of claim 7, further comprising:

depositing a sacrificial material on the substrate; and

etching a portion of the sacrificial material to form at least one qubit pocket on the substrate.

9. The method of claim 8, wherein the etching of the portion of the sacrificial layer is performed using a lithographic process.

10. The method of claim 8 or 9, further comprising:

wherein forming the first trench and the second trench comprises etching the substrate at the at least one qubit pocket.

11. The method of claim 10, wherein etching the substrate at the at least one qubit pocket is performed using an anisotropic wet etching process.

12. The method of any one of claims 7 to 11, further comprising removing the superconducting material from non-trench portions of the substrate.

13. The method of any one of claims 7 to 12, wherein the junction is formed using an evaporation process.

14. The method of claim 13, wherein the evaporation process is a shadow evaporation process.

15. The method of any one of claims 13 to 14, wherein the evaporation process includes a first evaporation in a first direction and a second evaporation in a second direction, the first direction being perpendicular to the second direction.

16. The method of any one of claims 7 to 15, wherein the removing of the portion of the substrate includes a subtractive etching process.

17. The method of any one of claims 7 to 16, wherein the junction is formed of a metal material.

18. The method of any one of claims 7 to 17, wherein the junction comprises a Josephson junction.

19. A semiconductor fabrication system comprising a lithography component, the semiconductor fabrication system when operated to fabricate a semiconductor device performing operations comprising:

forming a first trench and a second trench in a substrate;

depositing a superconducting material layer upon a surface of the first trench and a surface of the second trench to form a first capacitor structure and a second capacitor structure, respectively, and wherein the first capacitor structure and the second capacitor structure are formed of a superconducting material;

forming a junction between the first capacitor structure and the second capacitor structure; and

removing a portion of the substrate to form a lower portion of the first capacitor structure on a surface of the substrate and at least one first raised portion of the first

capacitor structure extending above the surface of the substrate, and a lower portion of the second capacitor structure on the surface of the substrate and at least one second raised portion extending above the surface of the substrate, wherein the junction is disposed at a predetermined distance from the surface of the substrate and having a first end in contact with one of the at least one first raised portion and a second end in contact with one of the at least one second raised portion.

20. The semiconductor fabrication system of claim 19, the operations further comprising:

depositing a sacrificial material on the substrate; and

etching a portion of the sacrificial material to form at least one qubit pocket on the substrate.

21. The semiconductor fabrication system of claim 20, wherein the etching of the portion of the sacrificial layer is performed using a lithographic process.

22. The semiconductor fabrication system of claim 20 or 21, wherein forming the first trench and the second trench comprises etching the substrate at the at least one qubit pocket.

23. The semiconductor fabrication system of claim 22, wherein etching the substrate at the at least one qubit pocket is performed using an anisotropic wet etching process.

24. The semiconductor fabrication system of any one of claims 19 to 23, further comprising removing the superconducting material from non-trench portions of the substrate.