

FIG. 1A

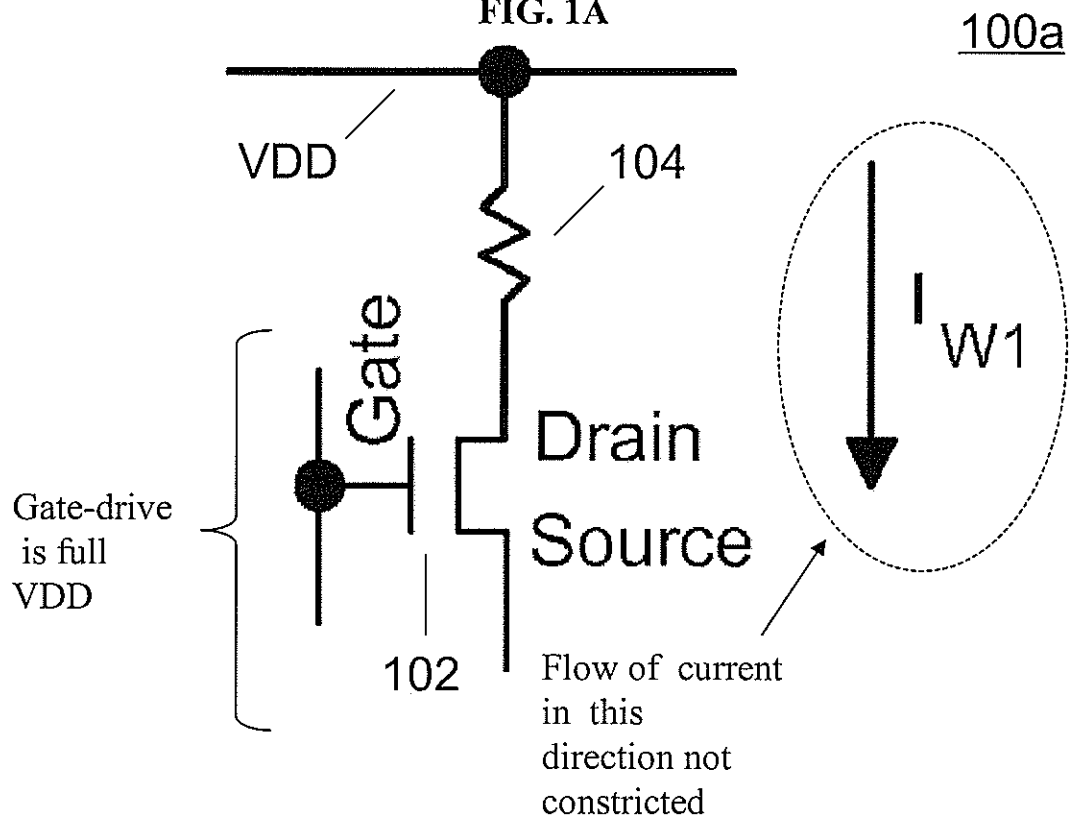


FIG. 1B

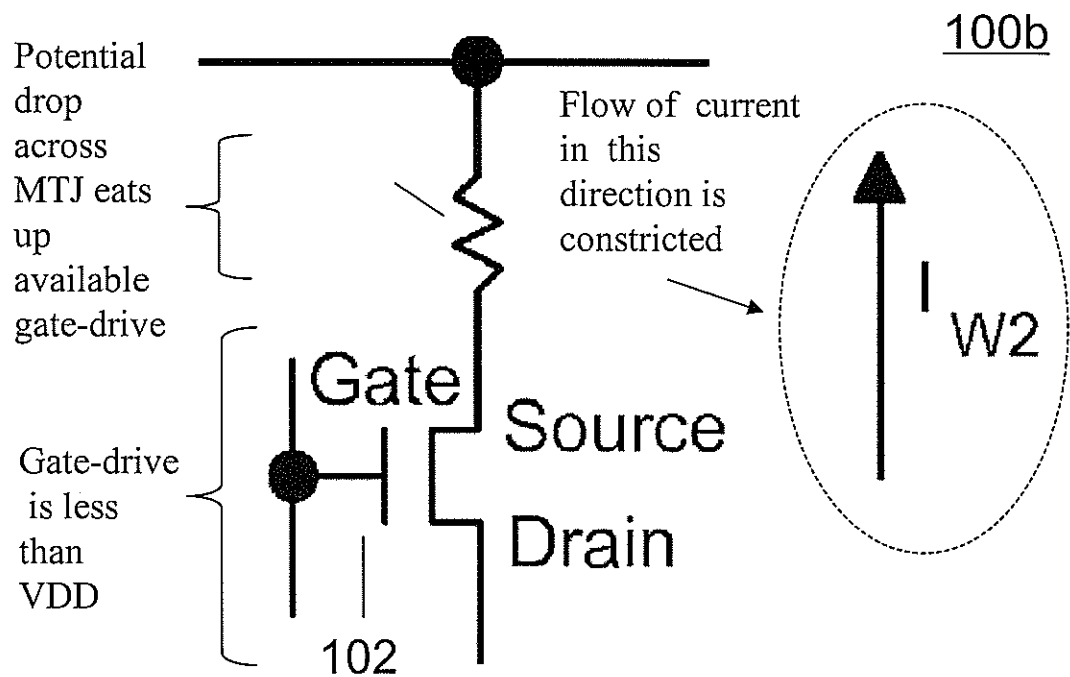


FIG. 1C

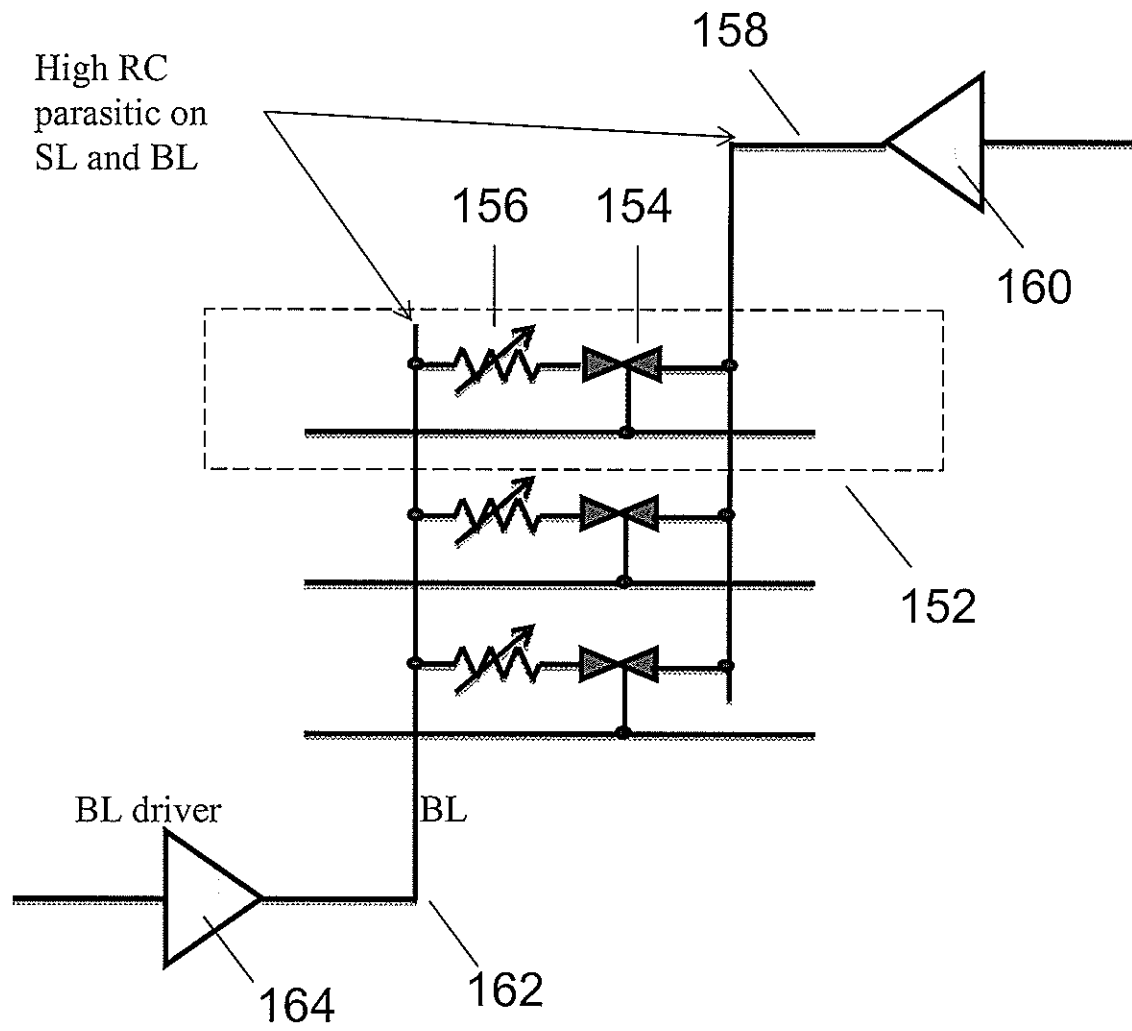
100c

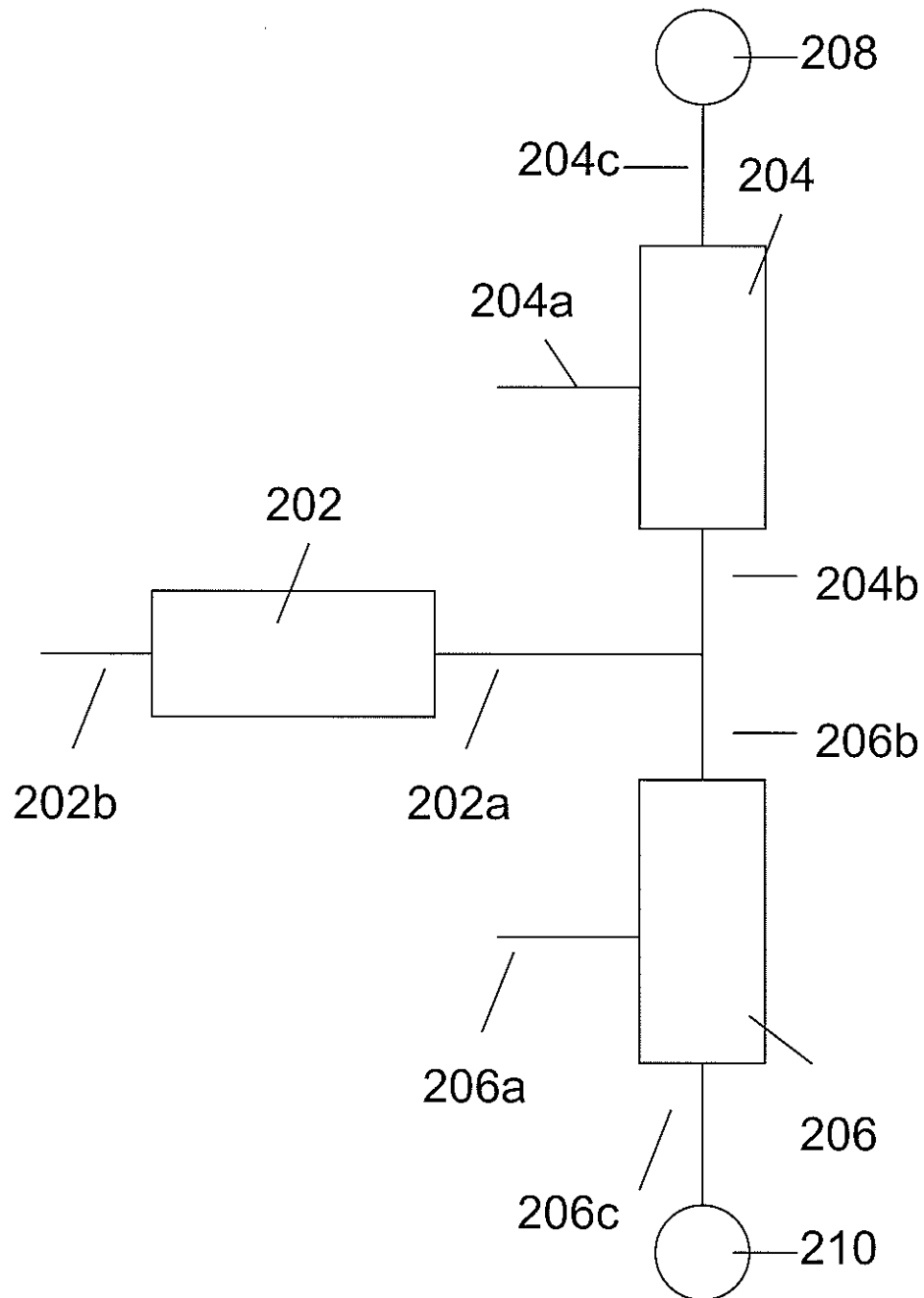
FIG. 2200

FIG. 3A

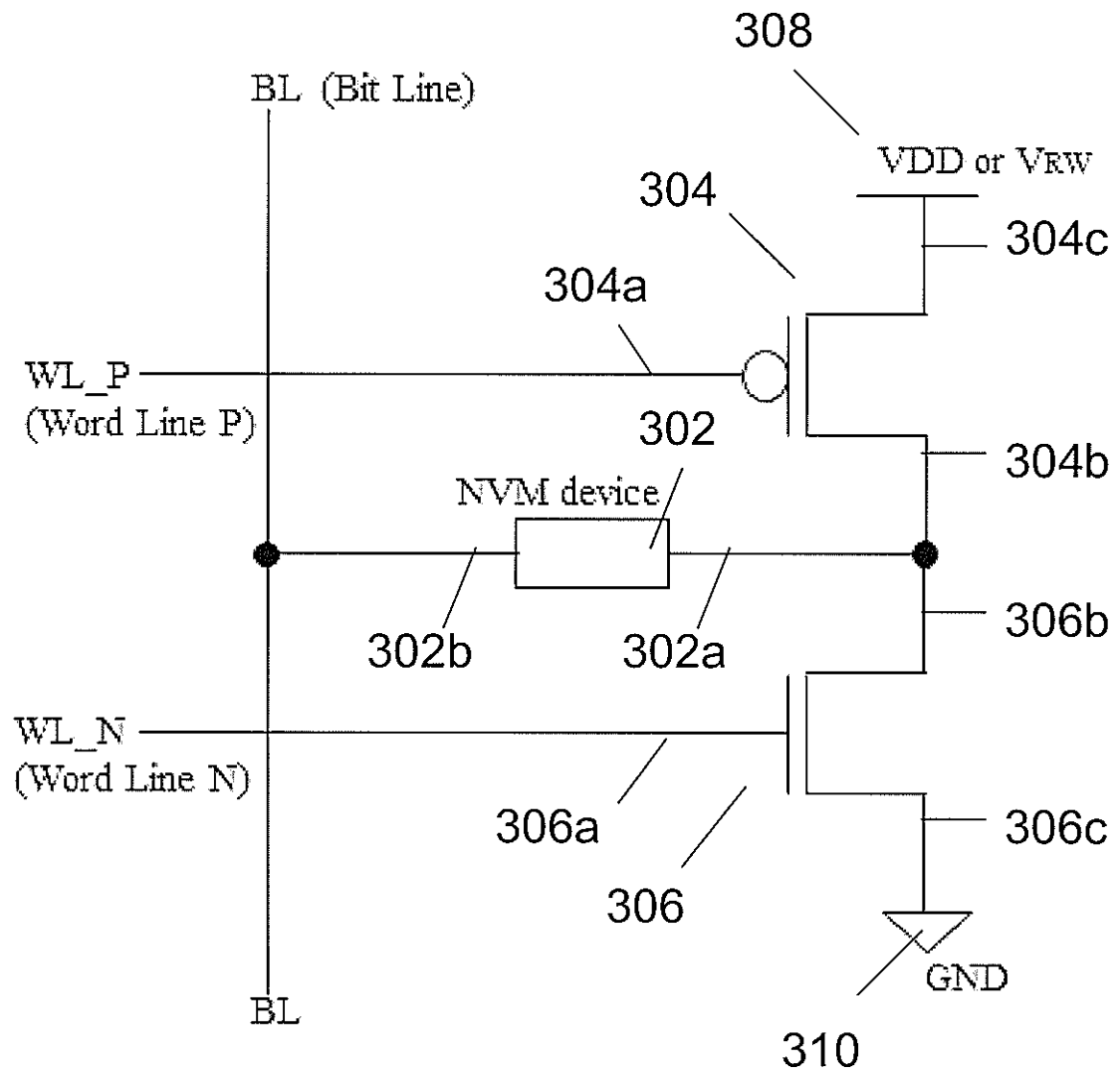
300a

FIG. 3B

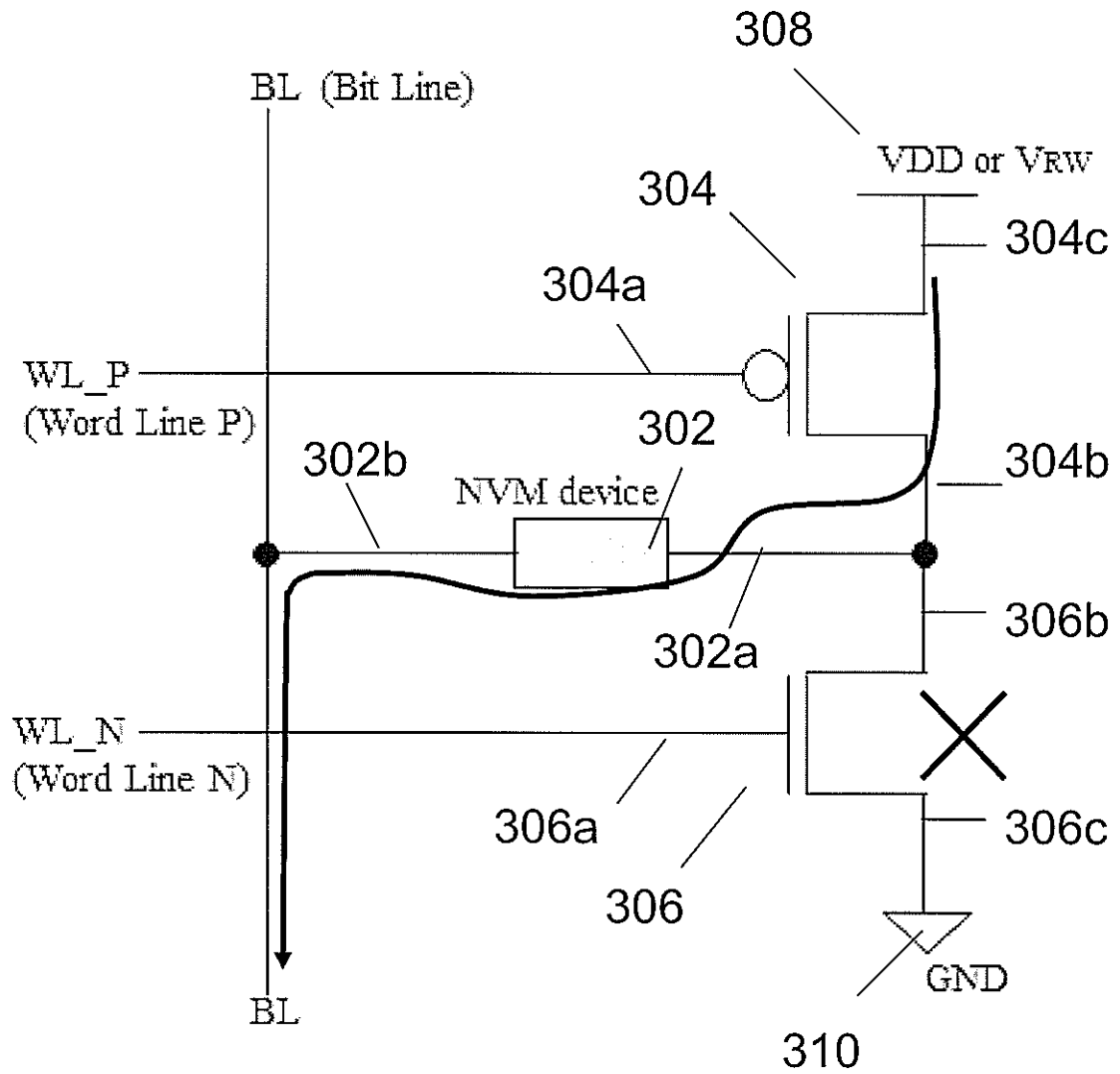
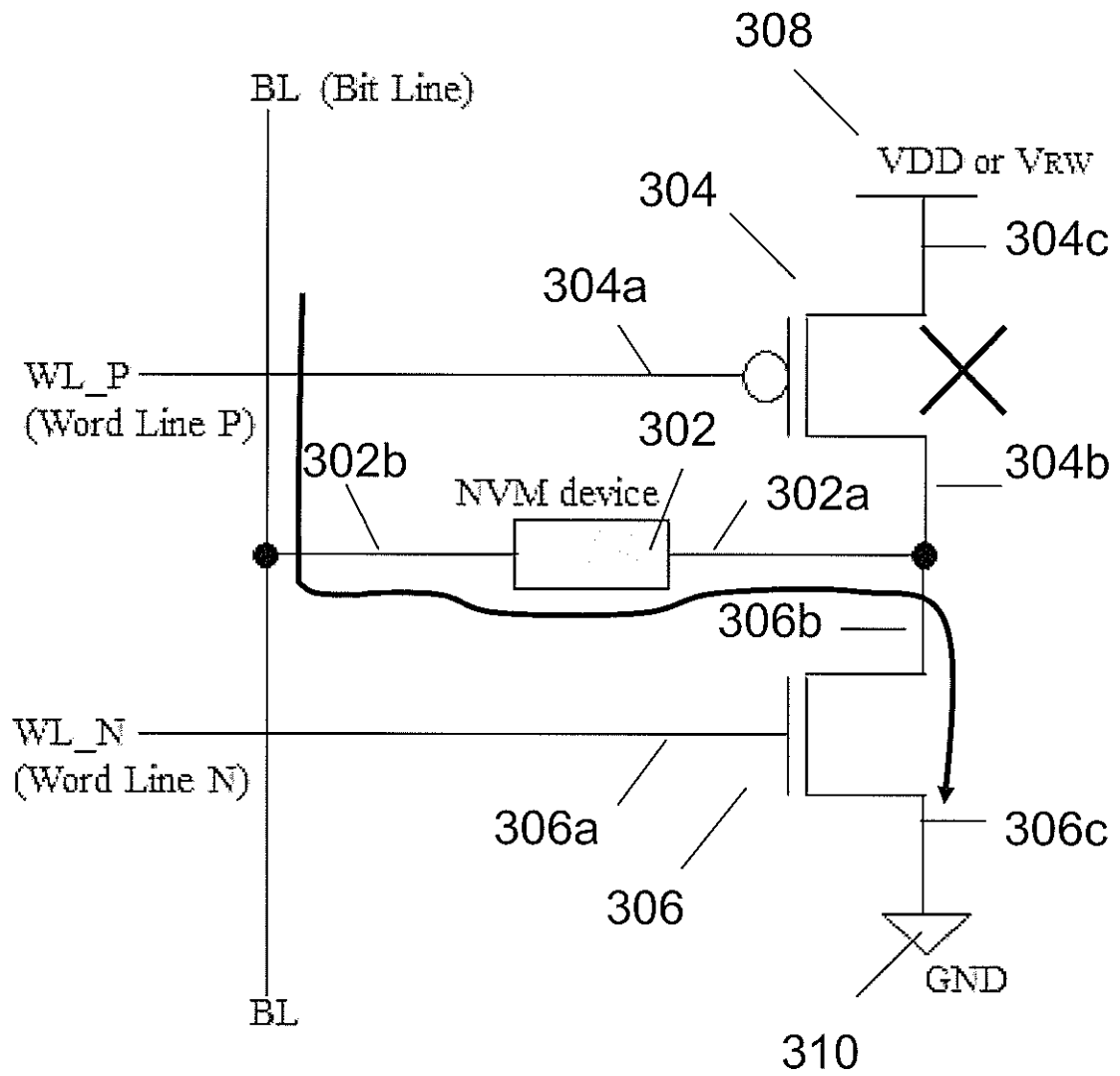
300b

FIG. 3C

300c

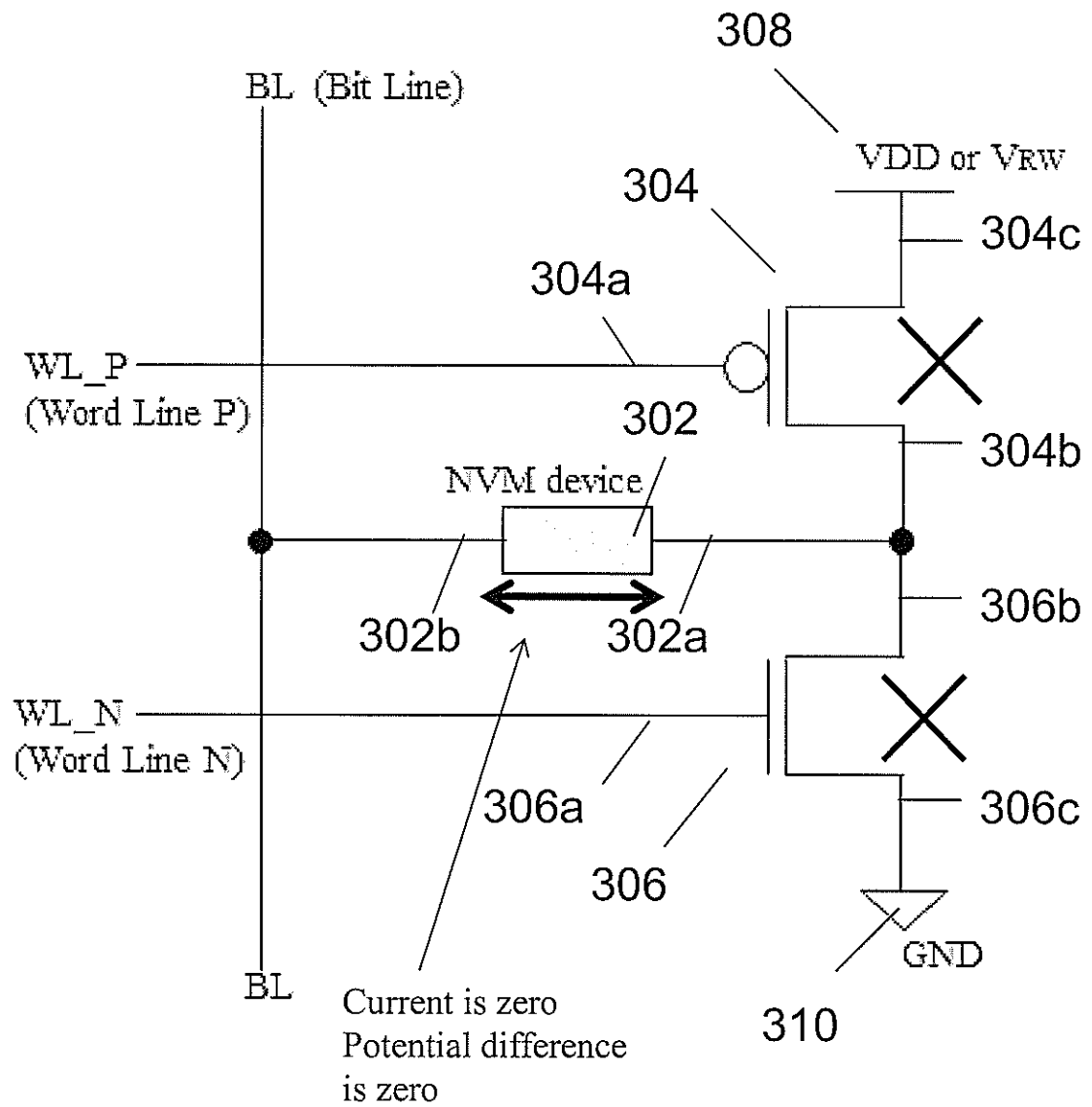
300d

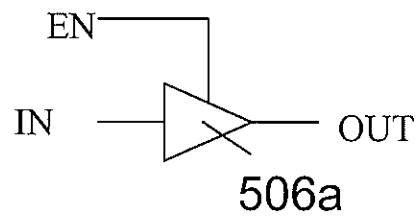
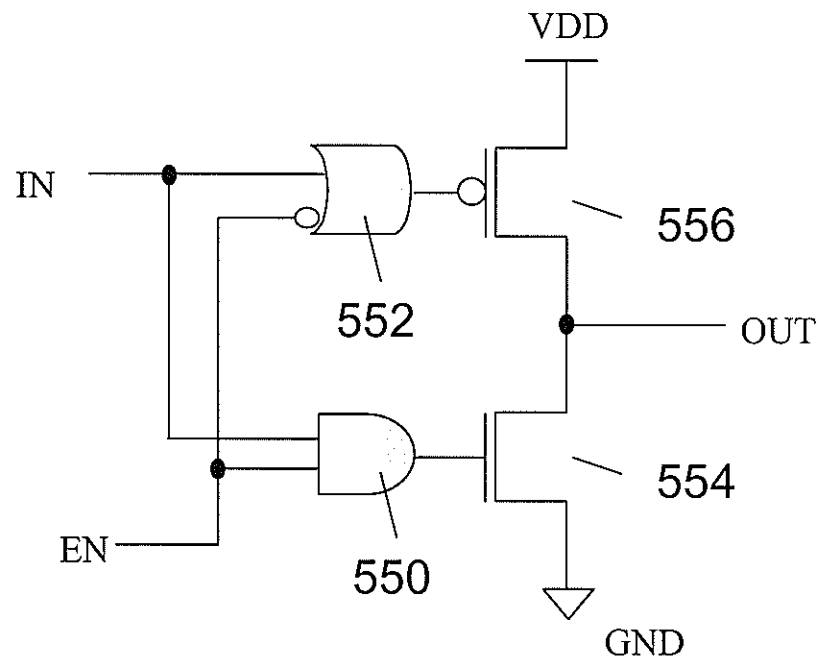
FIG. 5B500b**FIG. 5C**500c

FIG. 5D

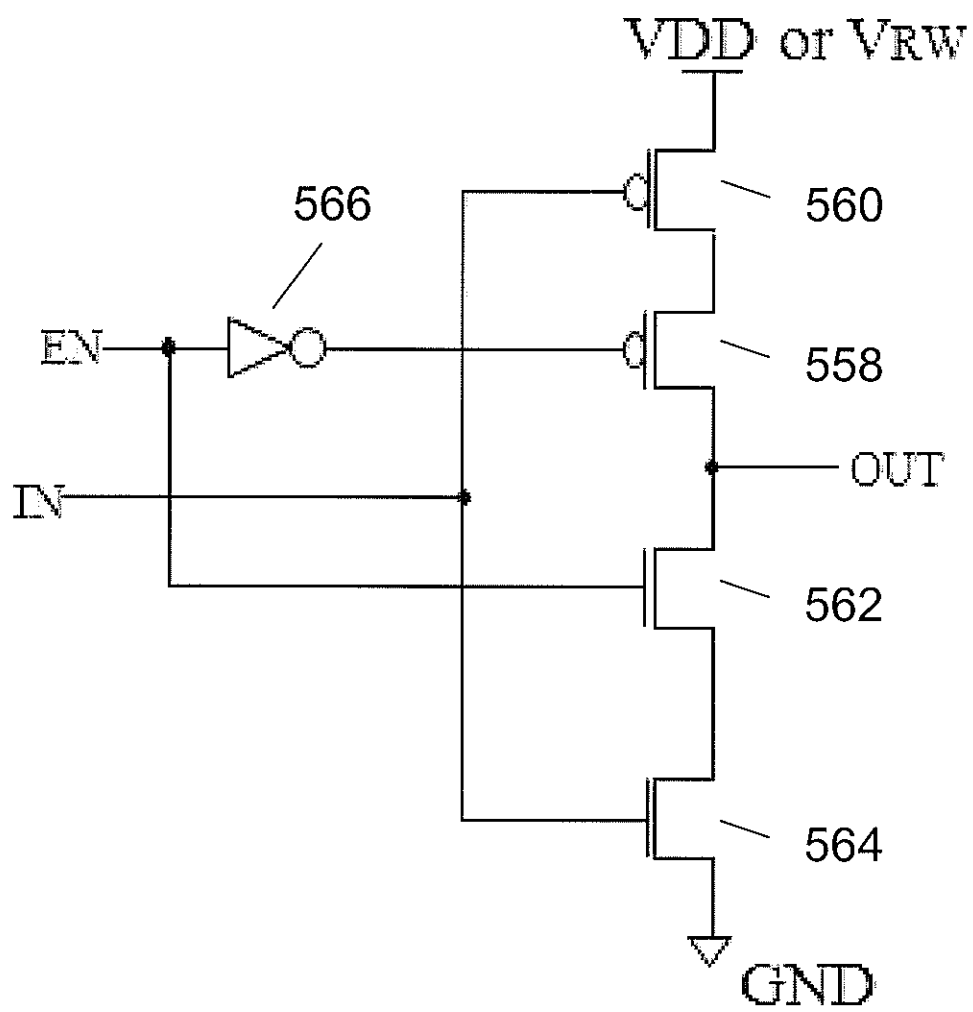
500d

FIG. 5E

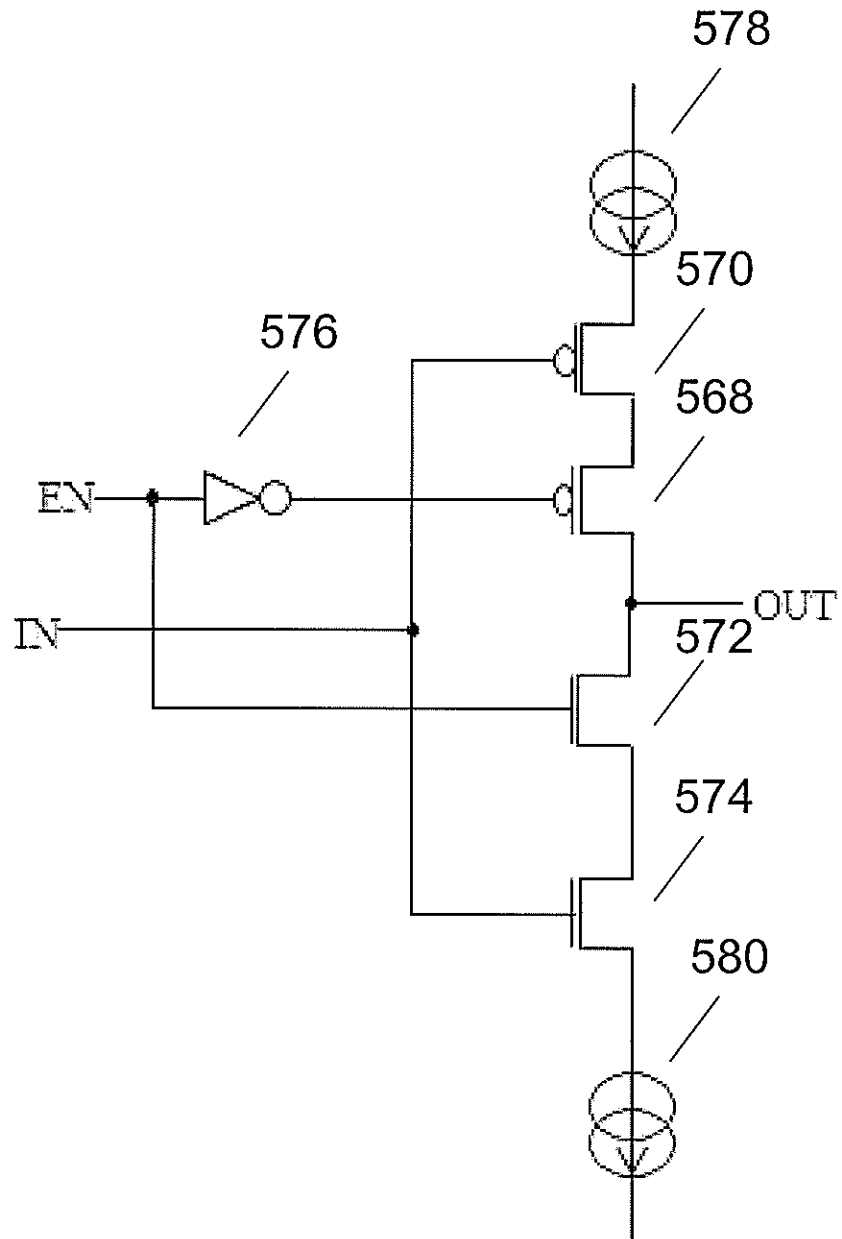
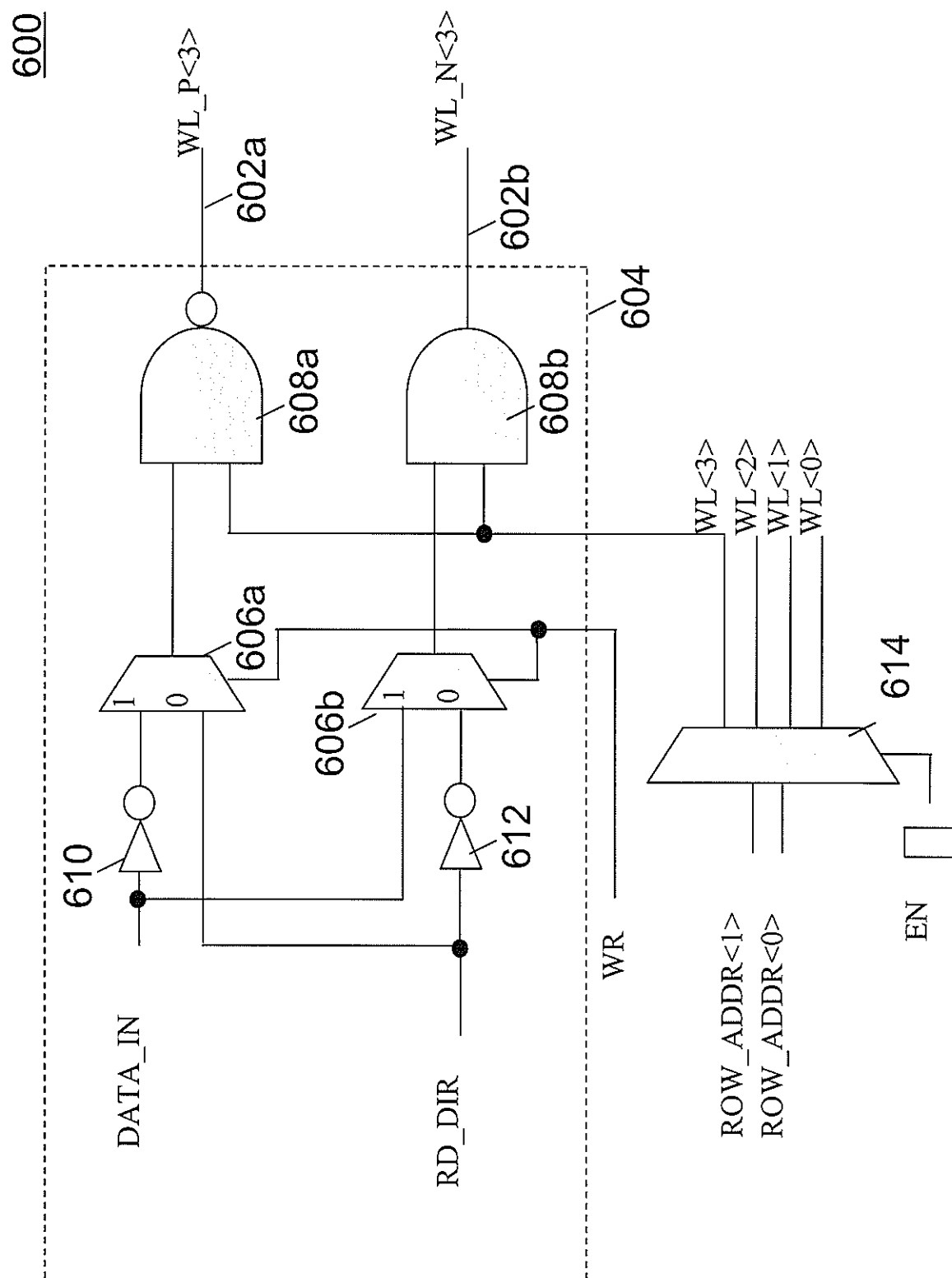
500e

FIG. 6



ROW ADDR<1>

ROW ADDR<0>

 $WL<3>$ $\langle WL \rangle$ $WL < 1$ $\langle 0 | T M$

EN

614

WR

DATA IN

RD DIR

 $\overline{WL} \ P<3>$ $WL_N<3>$

604

602a

602b

608a

9809

606a

9909

612

FIG. 7

700

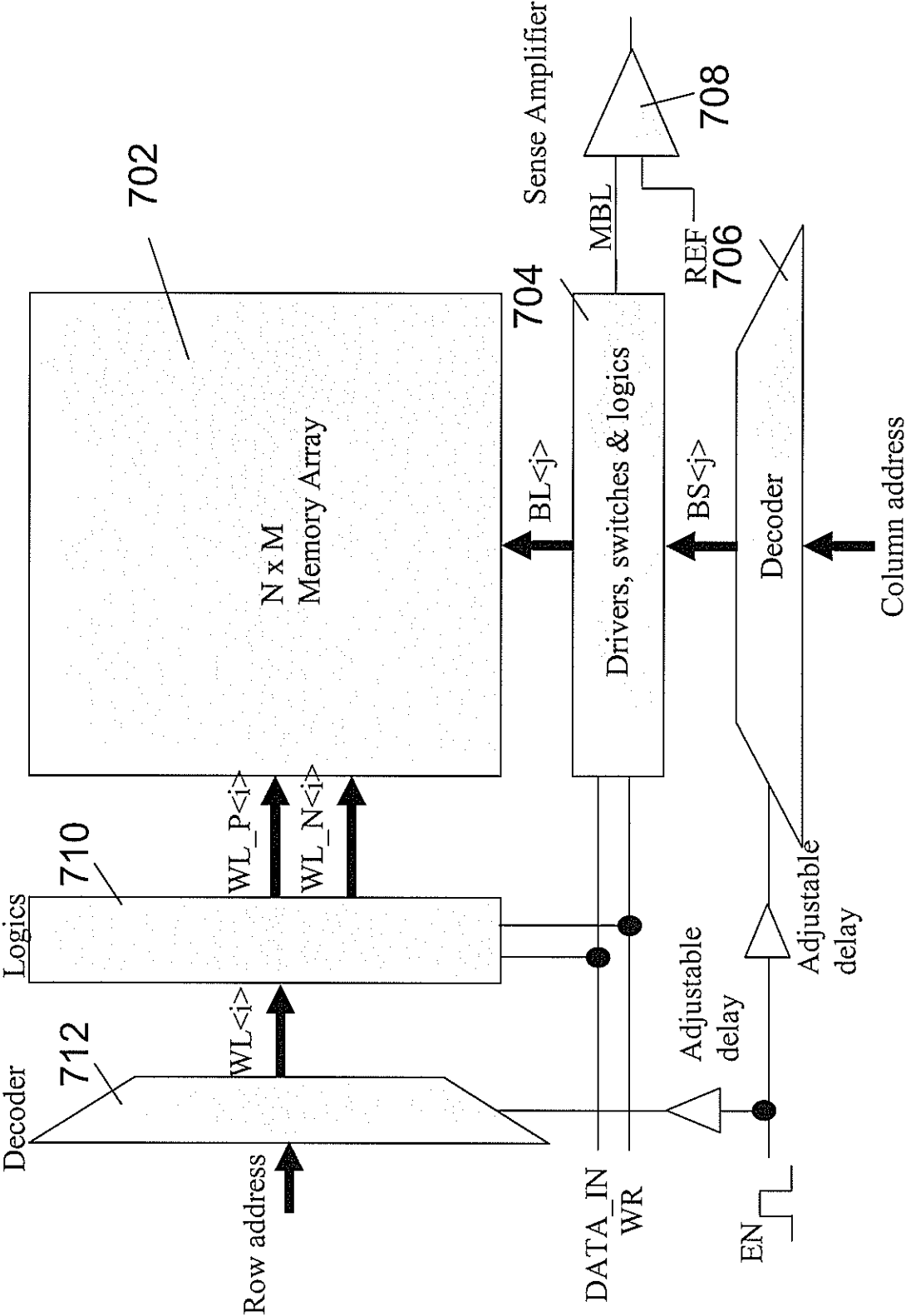
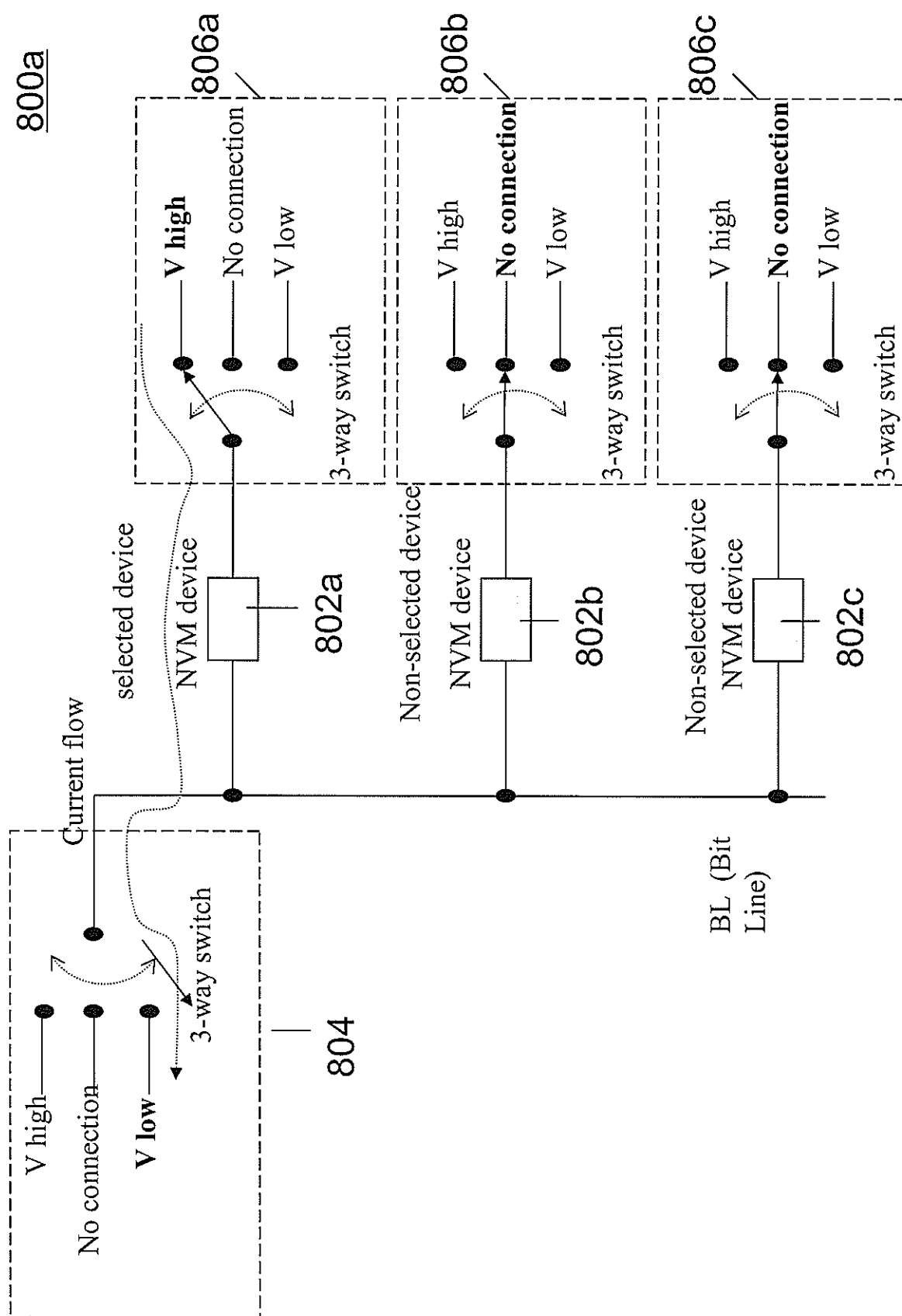


FIG. 8A



[illegible]

FIG. 9

900

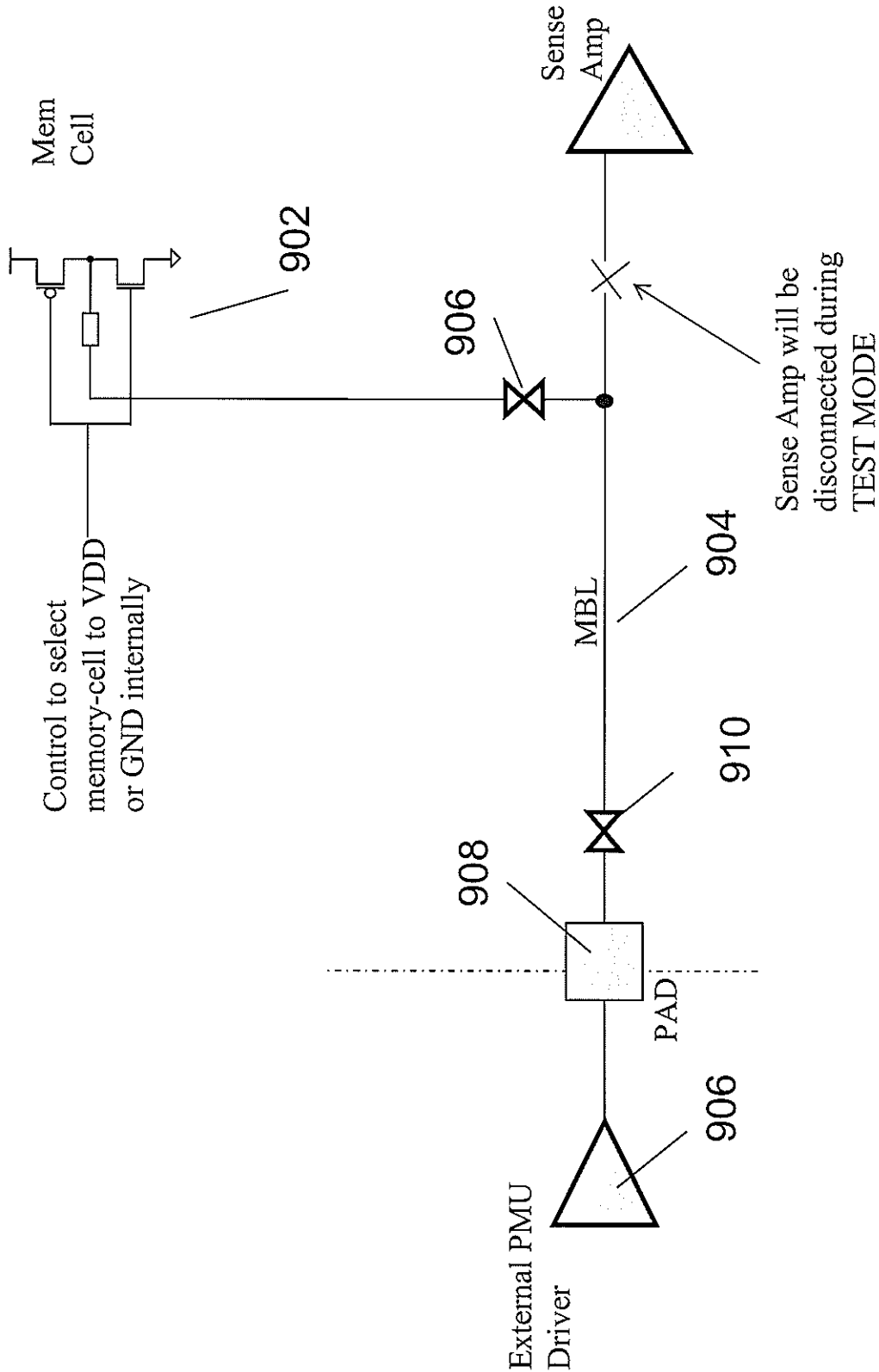


FIG. 10

1000

couple a first controlled electrode of a first transistor and a first controlled electrode of a second transistor to a first electrode of a data cell

1002

electrically connect a first reference voltage to a second controlled electrode of the first transistor such that the first electrode of the data cell is electrically connected to the first reference voltage via the first transistor when the first transistor is activated by a first word line voltage applied to the control electrode of the first transistor

1004

electrically connect a second reference voltage to a second controlled electrode of the second transistor such that the first electrode of the data cell is electrically connected to the second reference voltage via the second transistor when the first transistor is activated by a second word line voltage applied to the control electrode of the second transistor

1006

FIG. 11

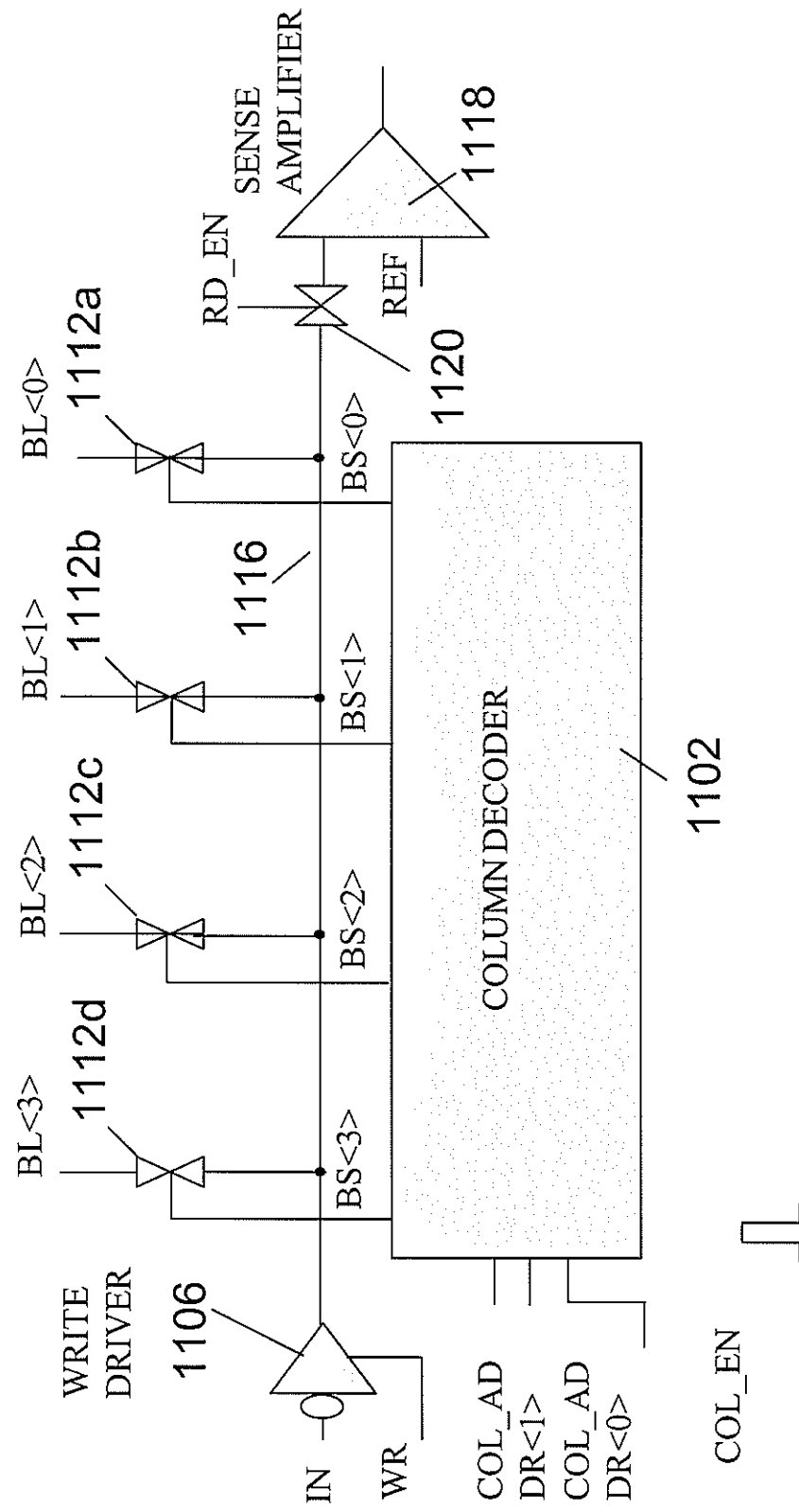
1100

FIG. 12

1200

