

Drawings

[Fig. 1(a)]

- a First device
- b Second device
- c Reset
- 101 Anomaly detector
- 102 First device reset part
- 103 Second device reset part

[Fig. 1(b)]

- a First device
- b Second device
- c Reset
- 111 Collating part
- 112 Reset part

[Fig. 1(c)]

- a First device
- b Second device
- c Reset
- 121 Second device reset part
- 122 Anomaly recognition part
- 123 Informative part
- 124 First device reset part

[Fig. 2]

- 2 Controller
- 3 Input/output unit

5 Terminal board

[Fig. 3]

a Host system

b Reset

c Input value

d Operation clock

e Timer clear signal

f Asynchronous communication

g KILL signal K1

h KILL signal K2

i Reset signal R1

j Reset signal R2

10 First system

20 Second system

12, 22 Peripheral system

11 Master CPU

14, 24 Watchdog timer

21 Slave CPU

[Fig. 4]

a KILL signal K1

b KILL signal K2

c Reset signal R1

d Reset signal R2

e Asynchronous communication

f Reset

10 First system
11 Master CPU
14, 24 Watchdog timer
20 Second system
21 Slave CPU

[Fig. 5]

a Host system
b Reset
c Input value
d Operation clock
e Timer clear signal
f Asynchronous communication
g KILL signal K1
h KILL signal K2
i Reset signal R1
j Reset signal R2
10 First system
20 Second system
12, 22 Peripheral system
11 Master CPU
14, 24 Watchdog timer
21 Slave CPU

[Fig. 6]

a Host system
b Reset

- c Operation clock
- d Timer clear signal
- e Asynchronous communication
- f KILL signal K1
- g KILL signal K2
- h Reset signal R1
- i Reset signal R2
- j Output ON/OFF
- 10A First system
- 20A Second system
- 12A, 22A Peripheral system
- 11A Master CPU
- 14A, 24A Watchdog timer
- 21A Slave CPU

[Fig. 7]

- a Reset
- b Asynchronous communication
- c KILL signal K1
- d KILL signal K2
- e KILL signal K3
- f Reset signal R1
- g Reset signal R2
- h Reset signal R3
- 30 First system
- 31 Master CPU

34, 44, 54 Watchdog timer

40 Second system

41 Slave CPU

50 Third system

51 Slave CPU

[Fig. 8]

a KILL signal K

b PV value

c Status

d PV value + Status + Code

78 Output part

13B, 23B Communication block

14B, 24B Code generation part

11B, 21B PV value processing part

12B, 22B Diagnostic part

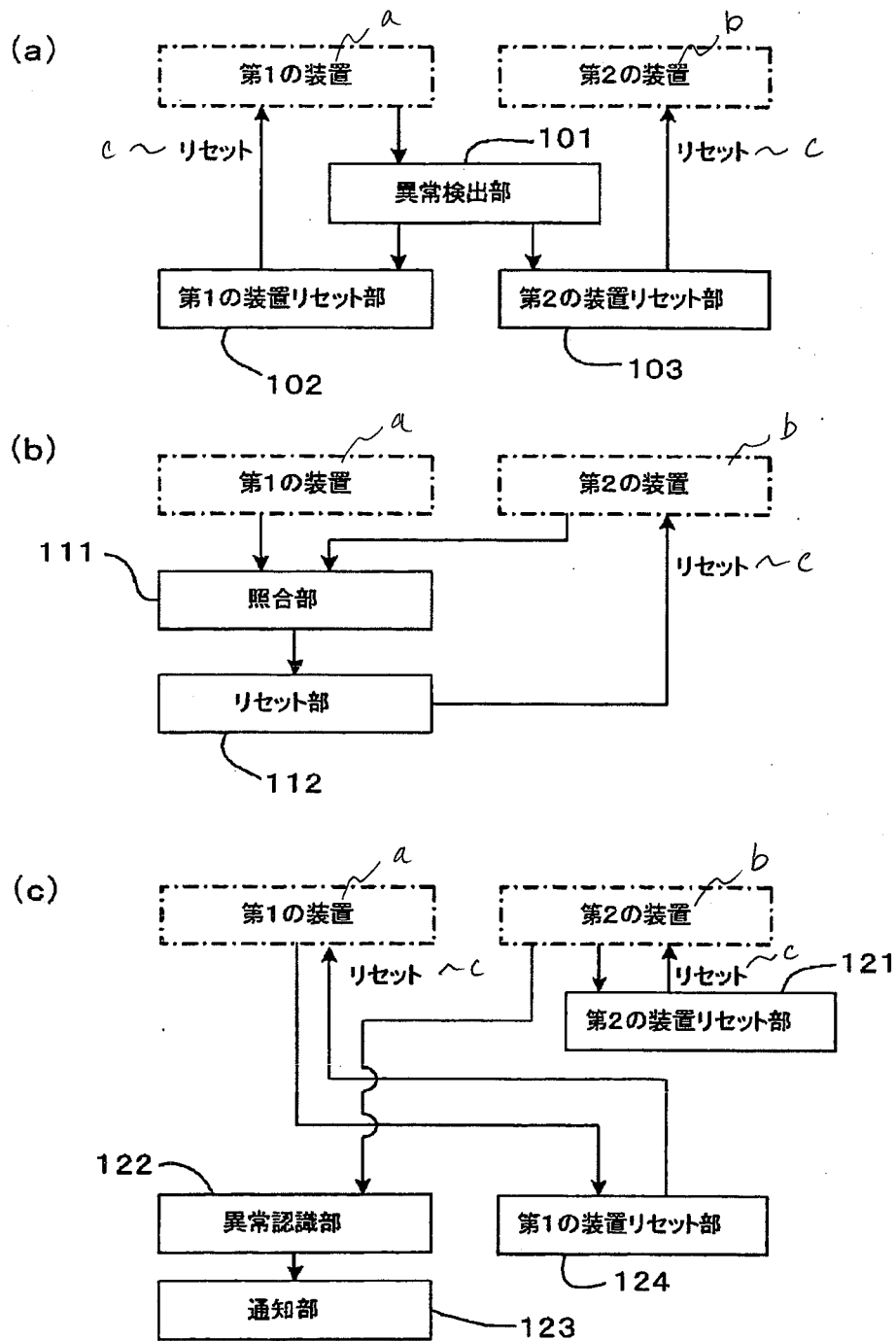
75, 77 Diagnostic circuit

74, 76 Peripheral circuit

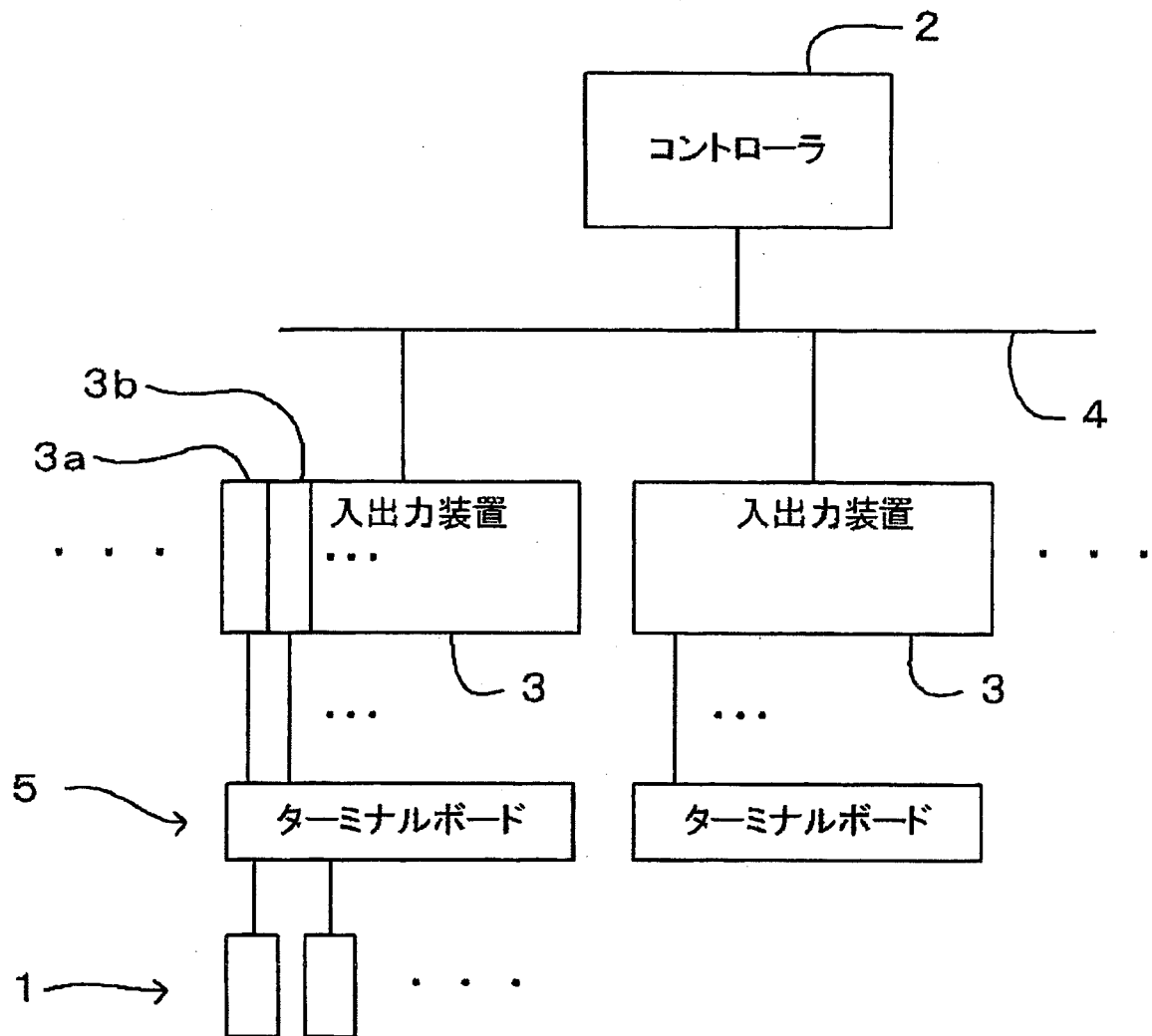
72, 73 Input buffer

71 Input part

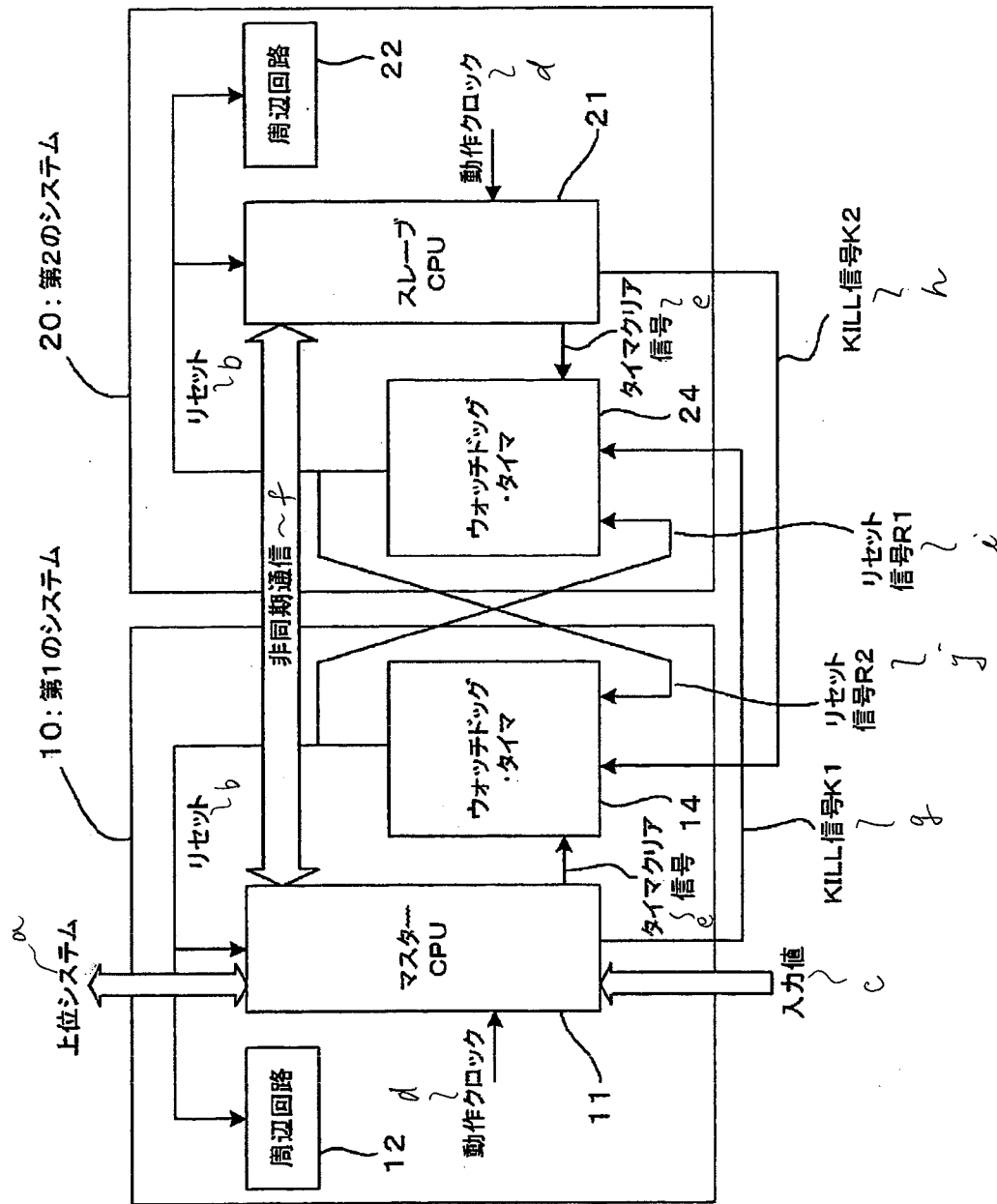
[図1] Fig.1



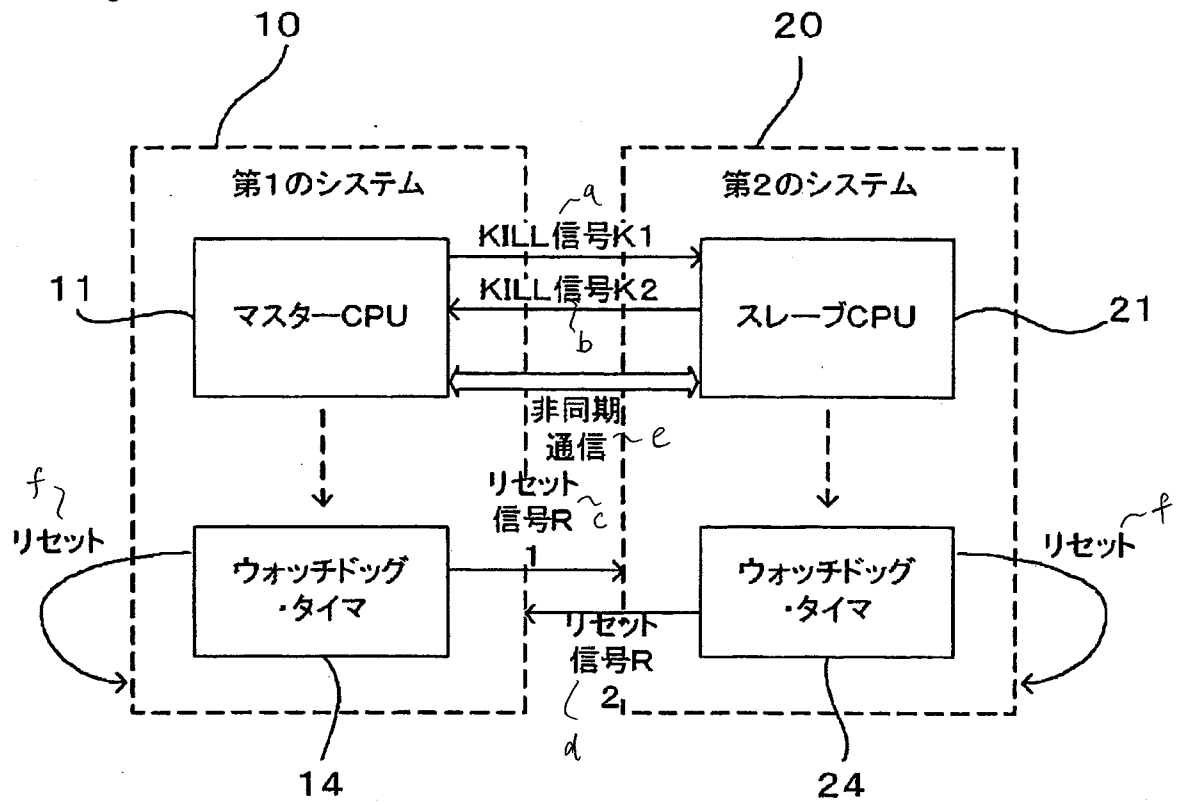
[図2] Fig. 2



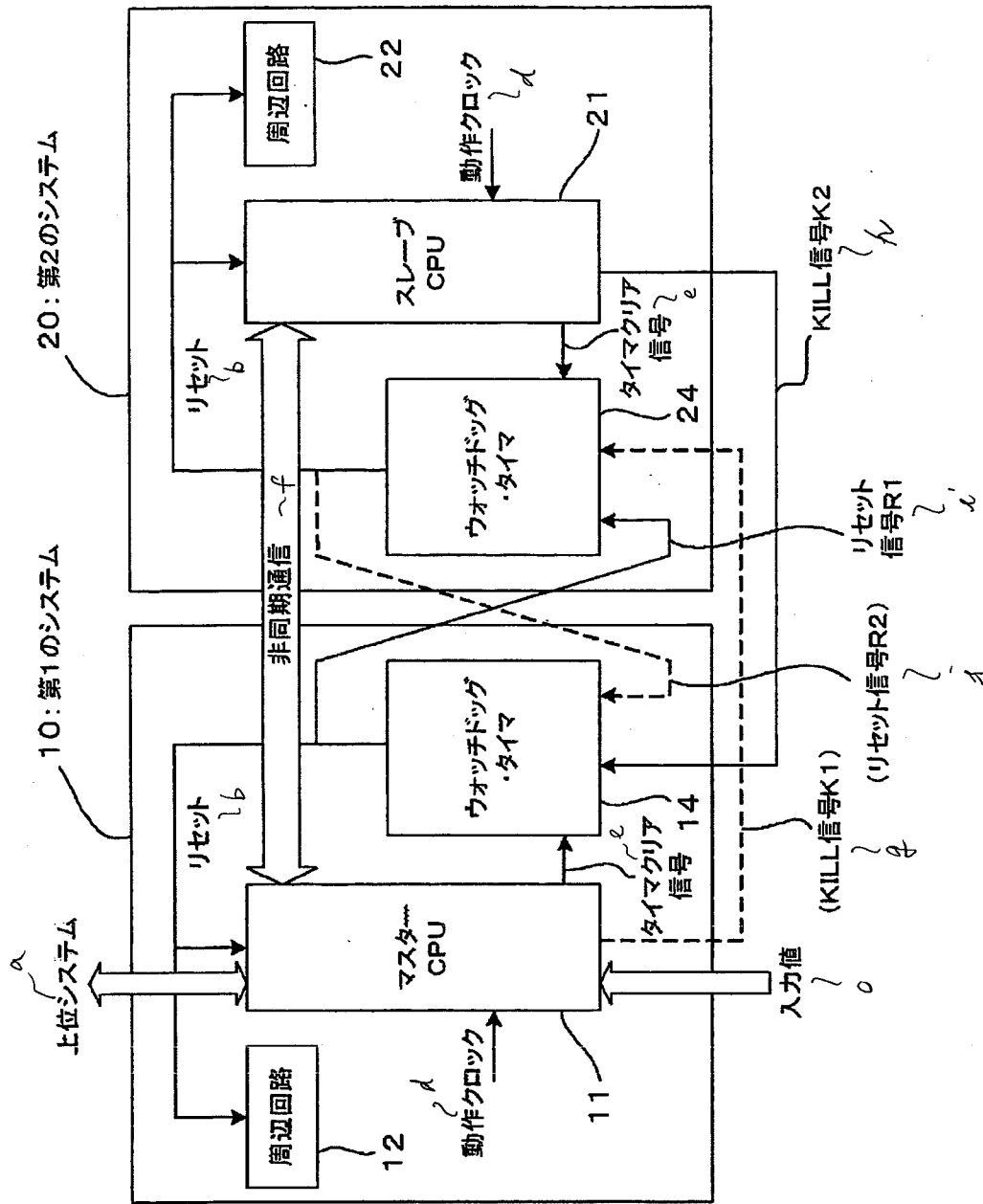
[図3] Fig. 3



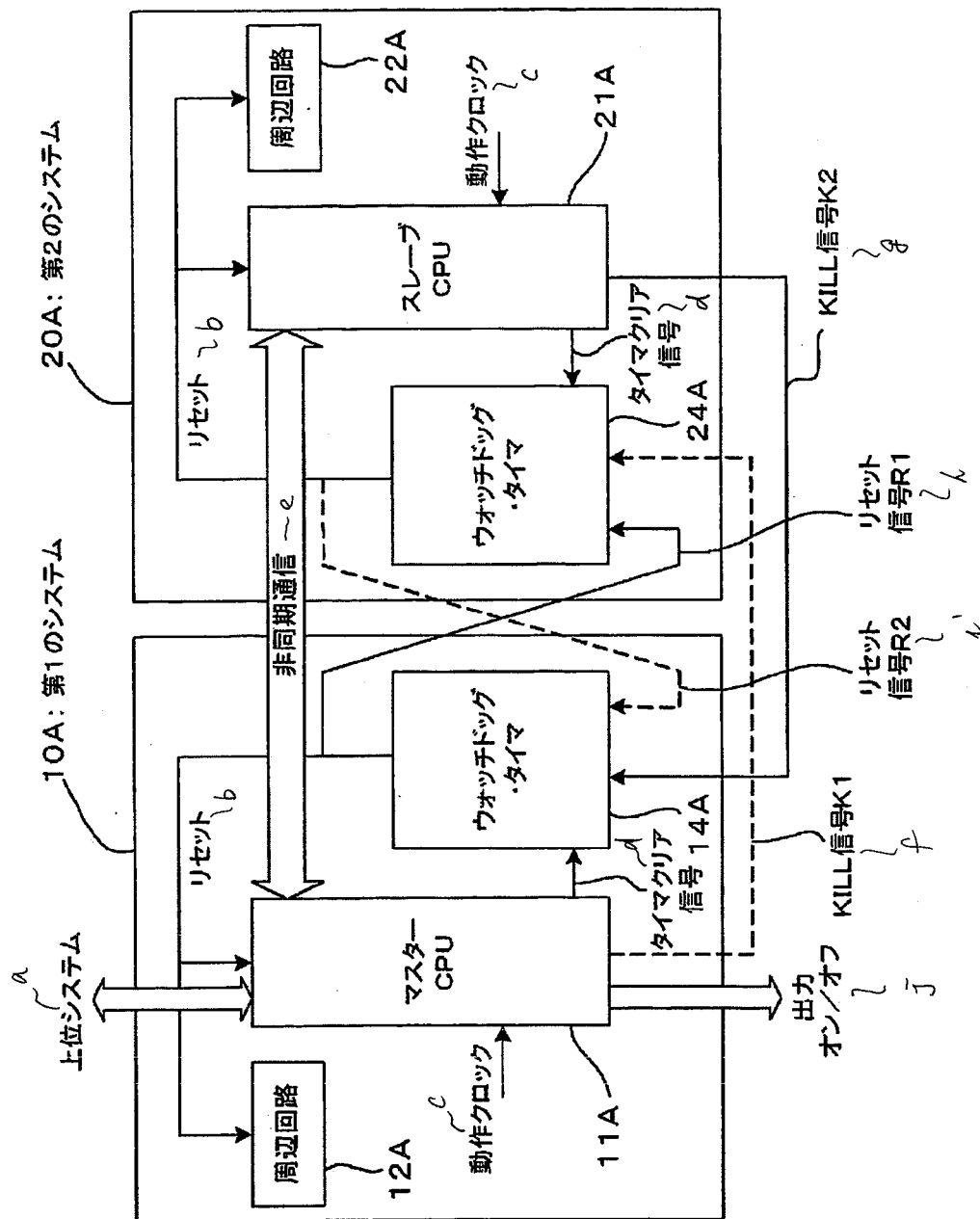
[図4] Fig. 4



[図5] Fig. 5



[図6] Fig. 6



[図8] Fig. 8

