

SEMICONDUCTOR DEVICE INCLUDING MULTIPLE DIES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent application is based on and claims priority to Korean Patent Application No. 10-2024-0152967, filed on 31 October 2024, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] The disclosure relates to a semiconductor device, and more particularly, to a semiconductor device having a stack structure of a plurality of dies.

BACKGROUND

[0003] To enhance the performance and storage capacity of semiconductor devices, semiconductor devices having a structure where a plurality of semiconductor dies are stacked are being used widely. As semiconductor devices are down-scaled, the size of dynamic random access memory (DRAM) devices is also reduced, and in DRAM devices having a 1T-1C structure where one capacitor is connected to one transistor, there is a problem where a leakage current occurring through a channel region increases progressively. Therefore, there is a need for vertical channel transistors including a channel layer extending in a vertical direction for decreasing a leakage current.

SUMMARY

[0004] One or more embodiments provide a semiconductor device having a structure where a plurality of semiconductor dies including a vertical channel transistor having good electrical performance are stacked.

[0005] According to an aspect of the disclosure, a semiconductor device may include a plurality of dies stacked in a vertical direction, wherein each of the plurality of dies includes: a

first substrate; a cell capacitor on the first substrate; a cell transistor on the cell capacitor; a second substrate, wherein a vertical level of the second substrate is higher than a vertical level of the cell transistor; a peripheral circuit transistor on the second substrate; and a through via passing through the first substrate and the second substrate in the vertical direction.

[0006] According to an aspect of the disclosure, a semiconductor device may include: a first die; and a second die on the first die, wherein each of the first die and the second die includes: a first substrate; a cell capacitor on the first substrate; a cell transistor on the cell capacitor; a second substrate, wherein a vertical level of the second substrate is higher than a vertical level of the cell transistor; a peripheral circuit transistor on the second substrate; a through via passing through the first substrate and the second substrate in a vertical direction; a wiring pattern that at least partially vertically overlaps with the through via, wherein a vertical level of the wiring pattern is higher than a vertical level of the peripheral circuit transistor; a front-side pad on an upper surface of the wiring pattern; and a backside pad on a lower surface of the through via.

[0007] According to an aspect of the disclosure, a semiconductor device may include: a first substrate including a first through via hole; a cell capacitor on the first substrate; a cell transistor on the cell capacitor; a second substrate, wherein a vertical level of the second substrate is higher than a vertical level of the cell transistor, and the second substrate includes a second through via hole that vertically overlaps with the first through via hole; a peripheral circuit transistor on the second substrate; a through via contact extending in a vertical direction in a via hole passing through the second substrate, and the through via contact electrically connects the peripheral circuit transistor to the cell transistor; a through via passing through the first through via hole and the second through via hole in the vertical direction; a through via insulation layer on a sidewall of the through via; a wiring pattern at least partially vertically overlapping with the through via, wherein a vertical level of the wiring pattern is higher than a

vertical level of the peripheral circuit transistor; a front-side pad on an upper surface of the wiring pattern; a front-side insulation layer on the upper surface of the wiring pattern, and an upper surface of the front-side insulation layer being coplanar with an upper surface of the front-side pad; a backside pad on a lower surface of the through via; and a backside insulation layer on a lower surface of the first substrate, and a lower surface of the backside insulation layer being coplanar with a lower surface of the backside pad.

BRIEF DESCRIPTION OF DRAWINGS

[0008] Embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0009] FIG. 1 is a schematic diagram illustrating a semiconductor device according to embodiments;

[0010] FIG. 2 is a perspective view schematically illustrating each semiconductor die of FIG. 1;

[0011] FIG. 3 is a cross-sectional view illustrating a region A of FIG. 1;

[0012] FIG. 4 is a cross-sectional view schematically illustrating a cell array region of FIG. 2;

[0013] FIG. 5 is a cross-sectional view schematically illustrating a cell array region according to embodiments; and

[0014] FIGS. 6, 7, 8, 9A, 9B, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22A, and 22B are schematic diagrams illustrating a method of manufacturing a semiconductor device, according to embodiments.

DETAILED DESCRIPTION

[0015] It will be understood that when an element or layer is referred to as being “on,” “connected to,” or “coupled to” another element or layer, it can be directly on, connected to, or coupled to the other element or layer or intervening elements or layers may be present. In

contrast, when an element or layer is referred to as being “directly on,” “directly connected to,” or “directly coupled to” another element or layer, there are no intervening elements or layers present.

[0016] FIG. 1 is a schematic diagram illustrating a semiconductor device 1 according to embodiments. FIG. 2 is a perspective view schematically illustrating each semiconductor die 10 of FIG. 1. FIG. 3 is a cross-sectional view illustrating a region A of FIG. 1. FIG. 4 is a cross-sectional view schematically illustrating a cell array region MCA of FIG. 2.

[0017] Referring to FIGS. 1 to 4, the semiconductor device 1 may include a plurality of semiconductor dies 10, which may be stacked in a vertical direction Z. Each of the plurality of semiconductor dies 10 may be disposed at an overlapping position in the vertical direction Z, and each of the plurality of semiconductor dies 10 may be electrically connected to a corresponding semiconductor die 10.

[0018] In embodiments, each of the plurality of semiconductor dies 10 may include a memory chip (e.g., a dynamic random access memory (DRAM) device). In embodiments, each of the plurality of semiconductor dies 10 may be a high bandwidth memory (HBM) device. In embodiments, the plurality of semiconductor dies 10 may not be disposed on a buffer die, and the semiconductor device 1 may be a buffer-less semiconductor device.

[0019] In other embodiments, the plurality of semiconductor dies 10 may be attached to the buffer die, and the buffer die may include a logic chip. In embodiments, the plurality of semiconductor dies 10 may be attached to a partial region of an interposer, and the logic chip may be mounted in another region of the interposer.

[0020] In embodiments, each of the plurality of semiconductor dies 10 may include at least one through via 12, which passes through a die body 10M and extends in the vertical direction Z. Each of the plurality of semiconductor dies 10 may include at least one front-side pad 14P, which is provided at (e.g., in or on) an uppermost surface of a corresponding

semiconductor die 10, and at least one backside pad 16P, which is provided at (e.g., in or on) a lowermost surface of the corresponding semiconductor die 10. In embodiments, the at least one front-side pad 14P and the at least one backside pad 16P may be electrically connected to the at least one through via 12.

[0021] In embodiments, each of the plurality of semiconductor dies 10 may include a front-side insulation layer 14I that defines an uppermost surface of a corresponding semiconductor die 10, and a backside insulation layer 16I that defines a lowermost surface of the corresponding semiconductor die 10. The front-side insulation layer 14I may be disposed on an upper surface of the die body 10M of the semiconductor die 10, and the front-side insulation layer 14I may include an upper surface, which may be disposed coplanar with an upper surface of the front-side pad 14P. The backside insulation layer 16I may be disposed on a lower surface of the die body 10M of the semiconductor die 10, and the backside insulation layer 16I may include a lower surface, which may be disposed coplanar with a lower surface of the backside pad 16P.

[0022] In embodiments, the plurality of semiconductor dies 10 may be attached or adhered to each other by a metal-oxide hybrid bonding process. In embodiments, a front-side pad 14P included in one semiconductor die 10 may contact a backside pad 16P included in another one semiconductor die 10 disposed immediately on the one semiconductor die 10, and a front-side insulation layer 14I included in the one semiconductor die 10 may contact a backside insulation layer 16I included in the other one semiconductor die 10 disposed immediately on the one semiconductor die 10.

[0023] In embodiments, the plurality of semiconductor dies 10 may include a first die C1, a second die C2, a third die C3, a fourth die C4, a fifth die C5, and a sixth die C6, which may be stacked in the vertical direction Z. In embodiments, a front-side pad 14P included in the first die C1 may contact a backside pad 16P included in the second die C2, and a front-side

insulation layer 14I included in the first die C1 may contact a backside insulation layer 16I included in the second die C2. Also, a front-side pad 14P included in the second die C2 may contact a backside pad 16P included in the third die C3, and a front-side insulation layer 14I included in the second die C2 may contact a backside insulation layer 16I included in the third die C3. Relationships between the third die C3, the fourth die C4, the fifth die C5, and the sixth die C6 may be the same as or similar to the relationships described above with respect to the first die C2, the second die C2, and the third die C3. In this manner, the plurality of semiconductor dies 10 may be stacked in the vertical direction Z by a metal-oxide hybrid bonding process.

[0024] In embodiments, the number of semiconductor dies 10 stacked in the vertical direction Z is not limited to the number illustrated in FIG. 1. For example, the number of semiconductor dies 10 may be 2 to 5 or 7 to 100.

[0025] In embodiments, each of the plurality of semiconductor dies 10 may include a DRAM device having a one transistor - one capacitor (1T-1C) structure where one cell transistor CTR (see FIG. 2) is electrically connected to one cell capacitor CAP (see FIG. 2).

[0026] As illustrated in FIG. 2, each of the plurality of semiconductor dies 10 may include a cell region CELL and a connection region CON. The cell region CELL of each of the plurality of semiconductor dies 10 may be a region where the cell transistor CTR, the cell capacitor CAP, and a peripheral circuit transistor PTR are disposed, and the connection region of each of the plurality of semiconductor dies 10 may be a region where the at least one through via 12 is disposed.

[0027] In embodiments, the cell region CELL may include a cell array region MCA and a peripheral circuit region PCA, which are disposed at different vertical levels with respect to each other. The cell array region MCA and the peripheral circuit region PCA may overlap each other in the vertical direction Z. As illustrated in FIG. 1, the peripheral circuit region PCA

may be disposed on the cell array region MCA, and each of the semiconductor devices (e.g., the semiconductor dies 10) may have a periphery over cell (POC) structure.

[0028] In embodiments, the cell array region MCA may be a memory cell region of the DRAM device, and for example, the cell transistor CTR and the cell capacitor CAP may be disposed in the cell array region MCA. In embodiments, the peripheral circuit region PCA may be a core region or a peripheral circuit region of the DRAM device. The peripheral circuit region PCA may include the peripheral circuit transistor PTR for transferring a signal and/or power to the cell transistor CTR and the cell capacitor CAP each included in the cell array region MCA. In embodiments, the peripheral circuit transistor PTR may configure various circuits such as a command decoder, a control logic, an address buffer, a row decoder, a column decoder, a sense amplifier, and a data input/output (I/O) circuit.

[0029] In embodiments, the peripheral circuit region PCA may be attached to the cell array region MCA by a bonding process. In embodiments, the peripheral circuit region PCA may be attached to the cell array region MCA by an oxide bonding process.

[0030] As illustrated in FIG. 3, each of the semiconductor dies 10 may include a first substrate 110, the cell capacitor CAP disposed on the first substrate 110, and the cell transistor CTR disposed on the cell capacitor CAP. Also, each of the semiconductor dies 10 may include a second substrate 210 disposed at a vertical level which is higher than a vertical level of the first substrate 110, and may include the peripheral circuit transistor PTR disposed on the second substrate 210. Each of the semiconductor dies 10 may include the at least one through via 12, which passes through the first substrate 110 and the second substrate 210 and extends in the vertical direction Z.

[0031] Each of the semiconductor dies 10 may include a wiring pattern WP disposed at a vertical level which is higher than a vertical level of the peripheral circuit transistor PTR. The wiring pattern WP may be electrically connected to the peripheral circuit transistor PTR

and the second substrate 210 and may include a portion which vertically overlaps with the at least one through via 12. The portion of the wiring pattern WP may be disposed to cover an upper surface of the through via 12. The wiring pattern WP may include a multilayer of a plurality of metal wiring lines. A wiring insulation layer 230 may be further disposed on an upper surface, a sidewall, and a lower surface of each of the plurality of metal wiring lines included in the wiring pattern WP.

[0032] Each of the semiconductor dies 10 may include a third interlayer insulation layer 238, the at least one front-side pad 14P, and the front-side insulation layer 14I, which may be disposed on the upper surface of the wiring pattern WP.

[0033] In some embodiments, the at least one front-side pad 14P may include copper or a copper alloy. At least a portion of a sidewall of the at least one front-side pad 14P may be surrounded by the front-side insulation layer 14I and the third interlayer insulation layer 238. In embodiments, the third interlayer insulation layer 238 may surround a lower portion of the sidewall of the at least one front-side pad 14P. In embodiments, the front-side insulation layer 14I may be disposed on the third interlayer insulation layer 238 and may surround an upper portion of the sidewall of the at least one front-side pad 14P. In embodiments, the front-side insulation layer 14I may have an upper surface coplanar with the upper surface of the at least one front-side pad 14P.

[0034] In some embodiments, the third interlayer insulation layer 238 may include silicon oxide, and the front-side insulation layer 14I may include at least one of silicon oxide, silicon nitride, silicon oxynitride, and silicon carbon nitride.

[0035] In some embodiments, a lower pad UWP may be further disposed between the wiring pattern WP and the at least one front-side pad 14P, and the lower pad UWP may include at least one of aluminum, tungsten, copper, and nickel. The lower pad UWP may be formed to

have a width which is greater than a width of the front-side pad 14P, and an entire lower surface of the front-side pad 14P may be disposed on a flat upper surface of the lower pad UWP.

[0036] Each of the semiconductor dies 10 may include the at least one backside pad 16P connected to a lower end of the at least one through via 12. In some embodiments, the at least one backside pad 16P may include copper or a copper alloy. At least a portion of a sidewall of the at least one backside pad 16P may be surrounded by the backside insulation layer 16I. The backside insulation layer 16I may include a lower surface coplanar with a lower surface of the at least one backside pad 16P. In some embodiments, the backside insulation layer 16I may include at least one of silicon oxide, silicon nitride, silicon oxynitride, and silicon carbon nitride.

[0037] In embodiments, the at least one through via 12 may pass through the first substrate 110 and the second substrate 210 and may extend in the vertical direction Z. A through via insulation layer 12I may be disposed on a sidewall of each of the at least one through via 12. In some embodiments, the through via insulation layer 12I may be disposed on the entire sidewall of the through via 12.

[0038] In embodiments, the first substrate 110 may include a first through via hole H1 passing through the first substrate 110, and the second substrate 210 may include a second through via hole H2, which passes through the second substrate 210 and is disposed at a position vertically overlapping with the first through via hole H1. The through via 12 may pass through the first through via hole H1 and the second through via hole H2 and may extend in the vertical direction Z, and for example, the through via 12 may extend in the vertical direction Z so that portions of the through via 12 are disposed in the first through via hole H1 and the second through via hole H2. The through via insulation layer 12I may surround a sidewall of the through via 12, may pass through the first through via hole H1 and the second through via hole H2, and may extend in the vertical direction Z.

[0039] In embodiments, the through via 12 may include an upper surface disposed at a vertical level which is higher than a vertical level of an upper surface of the second substrate 210, and may include a lower surface disposed at a vertical level which is lower than a vertical level of a lower surface of the first substrate 110. In embodiments, the through via insulation layer 12I may include an upper surface disposed at a vertical level which is higher than a vertical level of an upper surface of the second substrate 210, and may include a lower surface disposed at a vertical level which is lower than a vertical level of a lower surface of the first substrate 110. For example, a first portion of the through via insulation layer 12I may be disposed between an inner wall of the first through via hole H1 and a sidewall of the through via 12, and a second portion of the through via insulation layer 12I may be disposed between an inner wall of the second through via hole H2 and the sidewall of the through via 12. The sidewall of the through via 12 may be surrounded by the through via insulation layer 12I, and thus, the through via 12 may be electrically insulated from the first substrate 110 and the second substrate 210.

[0040] In embodiments, the first substrate 110 may include silicon (e.g., polycrystalline silicon, single crystalline silicon, or amorphous silicon). In some other embodiments, the first substrate 110 may include at least one from among germanium (Ge), silicon germanium (SiGe), silicon carbide (SiC), gallium arsenide (GaAs), indium arsenide (InAs), and indium phosphide (InP).

[0041] In embodiments, the cell capacitor CAP may be disposed on the first substrate 110, and the cell capacitor CAP may be a capacitor of a metal-insulator-metal (MIM) type. In embodiments, the cell capacitor CAP may include a first electrode 122, a capacitor dielectric layer 124, and a second electrode 126.

[0042] In other embodiments, instead of the cell capacitor CAP, a memory component such as a variable resistance memory device, a phase change memory device, or a magnetic memory device may be disposed.

[0043] In embodiments, an interface insulation layer 132 may be disposed between the first substrate 110 and the cell capacitor CAP, and a buried insulation layer 134 (e.g., a first buried insulation layer 134_1) may be disposed on the interface insulation layer 132 to surround a lower surface and a sidewall of the cell capacitor CAP. The buried insulation layer 134 may be disposed to cover the cell capacitor CAP on the first substrate 110, and the through via 12 and the through via insulation layer 12I may pass through the buried insulation layer 134 and may extend in the vertical direction Z. In embodiments, at least a portion of a sidewall of the through via insulation layer 12I may contact the buried insulation layer 134.

[0044] In embodiments, the cell capacitor CAP may be attached to the first substrate 110 by a bonding process. In embodiments, after the cell capacitor CAP and the first buried insulation layer 134_1 surrounding the cell capacitor CAP are formed, the interface insulation layer 132 may be formed on the first substrate 110, and the interface insulation layer 132 may be attached to the first buried insulation layer 134_1 by an oxide bonding process.

[0045] In embodiments, the cell transistor CTR may be a transistor of a vertical channel transistor type. In embodiments, the cell transistor CTR may include a channel layer AP extending in the vertical direction Z, a word line WL disposed on one sidewall of the channel layer AP, a back gate line BG disposed on another sidewall of the channel layer AP, and a bit line BL disposed on an upper surface of the channel layer AP. A gate insulation layer GI may be disposed between the channel layer AP and the word line WL and between the channel layer AP and the back gate line BG.

[0046] In embodiments, a landing pad LP may be disposed on a lower surface of the channel layer AP, and the first electrode 122 of the cell capacitor CAP may be disposed to extend in the vertical direction Z with the landing pad LP therebetween.

[0047] In embodiments, the channel layer AP may include at least one of silicon, germanium, and silicon germanium. In embodiments, the channel layer AP may be provided in plural, and in some embodiments, the plurality of channel layers AP may be arranged in a matrix form in a first horizontal direction X and a second horizontal direction Y.

[0048] In embodiments, a plurality of word lines WL and a plurality of back gate lines BG may be alternately arranged in the first horizontal direction X and may extend in the second horizontal direction Y. In embodiments, the plurality of word lines WL and the plurality of back gate lines BG may include titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), molybdenum (Mo), molybdenum nitride (MoN), ruthenium (Ru), tungsten (W), tungsten nitride (WN), cobalt (Co), titanium silicon nitride (TiSiN), tungsten silicon nitride (WSiN), or a combination thereof.

[0049] In embodiments, the bit line BL may be disposed on the upper surface of the channel layer AP and may extend in the first horizontal direction X. In embodiments, the bit line BL may include Ti, TiN, Ta, TaN, Mo, MoN, Ru, W, WN, Co, TiSiN, WSiN, polysilicon, or a combination thereof.

[0050] In embodiments, the gate insulation layer GI may include at least one material from among hafnium oxide (HfO), hafnium silicate (HfSiO), hafnium oxide nitride (HfON), hafnium silicon oxide nitride (HfSiON), lanthanum oxide (LaO), lanthanum aluminum oxide (LaAlO), zirconium oxide (ZrO), zirconium silicon oxide (ZrSiO), zirconium oxide nitride (ZrON), zirconium silicon oxide nitride (ZrSiON), tantalum oxide (TaO), titanium oxide (TiO), barium strontium titanium oxide (BaSrTiO), barium titanium oxide (BaTiO), lead zirconium titanium oxide (PbZrTiO), strontium tantalum bismuth oxide (SrTaBiO), bismuth iron oxide

(BiFeO), strontium titanium oxide (SrTiO), yttrium oxide (YO), aluminum oxide (AlO), and lead scandium tantalum oxide (PbScTaO).

[0051] In embodiments, the landing pad LP may be disposed between the lower surface of the channel layer AP and the first electrode 122, and the landing pad LP may include Ti, TiN, Ta, TaN, Mo, MoN, Ru, W, WN, Co, TiSiN, WSiN, polysilicon, or a silicide material thereof.

[0052] In embodiments, the cell transistor CTR may be covered by the buried insulation layer 134. In embodiments, a portion of the cell transistor CTR including the channel layer AP, the word line WL, and the back gate line BG may be covered by a second buried insulation layer 134_2 of the buried insulation layer 134, and the bit line BL may be covered by a third buried insulation layer 134_3 of the buried insulation layer 134.

[0053] In embodiments, a cell wiring structure 136, which may at least partially pass through the buried insulation layer 134 and is electrically connected to the cell capacitor CAP and the cell transistor CTR, may be disposed. The cell wiring structure 136 may include a first wiring 136_1 covered by the second buried insulation layer 134_2 and the third buried insulation layer 134_3, a first contact 136_2 covered by the second buried insulation layer 134_2 and the third buried insulation layer 134_3 and connected to the first wiring 136_1 or the cell transistor CTR, a second wiring 136_3 covered by the first buried insulation layer 134_1, and a second contact 136_4 covered by the first buried insulation layer 134_1 and connected to the second wiring 136_3 or the cell capacitor CAP.

[0054] In embodiments, the first wiring 136_1 and the first contact 136_2 may be electrically connected to the cell transistor CTR, and for example, may be electrically connected to the word line WL, the back gate line BG, and/or the bit line BL. In embodiments, the second wiring 136_3 and the second contact 136_4 may be electrically connected to the cell capacitor CAP.

[0055] A first interlayer insulation layer 138 may be disposed on the lower surface of the first substrate 110. The first interlayer insulation layer 138 may surround a portion of a sidewall of the through via insulation layer 12I and may surround a portion of a sidewall of the backside pad 16P. The backside insulation layer 16I may be disposed on a lower surface of the first interlayer insulation layer 138.

[0056] In embodiments, the second substrate 210 may be disposed at a vertical level which is higher than a vertical level of the first substrate 110. The second substrate 210 may include silicon (e.g., polycrystalline silicon, single crystalline silicon, or amorphous silicon). In some other embodiments, the second substrate 210 may include at least one from among Ge, SiGe, SiC, GaAs, InAs, and InP.

[0057] A second interlayer insulation layer 234 may be disposed on a lower surface of the second substrate 210, and a lower surface of the second interlayer insulation layer 234 may contact an upper surface of the buried insulation layer 134 (e.g., the third buried insulation layer 134_3).

[0058] The peripheral circuit transistor PTR may be disposed on the upper surface of the second substrate 210. The peripheral circuit transistor PTR may include at least one of a flat-type transistor, a FinFET transistor, a multi-bridge channel transistor, and a buried channel array transistor.

[0059] The wiring pattern WP electrically connected to the peripheral circuit transistor PTR and the second substrate 210 may be disposed on the upper surface of the second substrate 210, and the wiring insulation layer 230 covering the peripheral circuit transistor PTR and the wiring pattern WP may be disposed on the upper surface of the second substrate 210.

[0060] In embodiments, the via hole 210H may be disposed to pass through the second substrate 210, and a via insulation layer 222 may be disposed in the via hole 210H. The through via contact 220 may pass through the via insulation layer 222 and may extend in the vertical

direction Z, and the wiring pattern WP may be electrically connected to the cell wiring structure 136 by the through via contact 220.

[0061] According to embodiments, each of the semiconductor dies 10 may include the cell transistor CTR disposed on the first substrate 110, the peripheral circuit transistor PTR disposed on the second substrate 210, and the through via 12 passing through the first substrate 110 and the second substrate 210, and the plurality of semiconductor dies 10 may be stacked in the vertical direction Z and connected together via the front-side pad 14P and the backside pad 16P. The semiconductor device 1 may be high in degree of integration, and moreover, may have good electrical performance.

[0062] FIG. 5 is a cross-sectional view schematically illustrating a cell array region MCA-1 according to embodiments.

[0063] Referring to FIG. 5, a cell transistor CTR may be disposed in an opening portion of a mold insulation layer MS. The cell transistor CTR may include a channel layer AP including a vertical cross-sectional surface having a reversed-U shape. Two word lines WL may be disposed apart from each other between two vertical extension portions of the channel layer AP.

[0064] In embodiments, the channel layer AP may include an oxide semiconductor. In embodiments, the oxide semiconductor may include at least one of zinc tin oxide (Zn_xSn_yO), indium zinc oxide (In_xZn_yO), zinc oxide (ZnO_x), indium gallium zinc oxide ($In_xGa_yZn_zO$), indium gallium silicon oxide ($In_xGa_ySi_zO$), indium tungsten oxide (In_xW_yO), indium oxide (In_xO), tin oxide (Sn_xO), titanium oxide (Ti_xO), zinc oxynitride (Zn_xON_z), magnesium zinc oxide (Mg_xZn_yO), zirconium indium zinc oxide ($Zr_xIn_yZn_zO$), hafnium indium zinc oxide ($Hf_xIn_yZn_zO$), tin indium zinc oxide ($Sn_xIn_yZn_zO$), aluminum tin indium zinc oxide ($Al_xSn_yIn_zZn_aO$), silicon indium zinc oxide ($Si_xIn_yZn_zO$), aluminum zinc tin oxide

($\text{Al}_x\text{Zn}_y\text{Sn}_z\text{O}$), gallium zinc tin oxide ($\text{Ga}_x\text{Zn}_y\text{Sn}_z\text{O}$), and zirconium zinc tin oxide ($\text{Zr}_x\text{Zn}_y\text{Sn}_z\text{O}$).

In embodiments, the channel layer AP may further include an n-type impurity ion. For example, the n-type impurity ion may be doped in the channel layer AP through an ion implantation process.

[0065] FIGS. 6 to 8, 9A, 9B, 10 to 21, 22A, and 22B are schematic diagrams illustrating a method of manufacturing a semiconductor device 1, according to embodiments.

[0066] Referring to FIG. 6, a mask pattern may be formed on a second substrate 210, and a via hole 210H may be formed by removing a portion of the second substrate 210 using the mask pattern as an etch mask. Subsequently, a via insulation layer 222 may be formed in the via hole 210H using an insulating material.

[0067] A peripheral circuit transistor PTR may be formed on the second substrate 210, and a first wiring insulation layer 230_1 covering the peripheral circuit transistor PTR may be formed. In embodiments, the first wiring insulation layer 230_1 may include at least one of silicon oxide, silicon nitride, silicon oxynitride, and a low-k dielectric material.

[0068] In embodiments, the peripheral circuit transistor PTR may include at least one of a flat-type transistor, a FinFET transistor, a multi-bridge channel transistor, and a buried channel array transistor.

[0069] Referring to FIG. 7, a first carrier substrate 310 may be attached to the first wiring insulation layer 230_1. In embodiments, an interface insulation layer 312 may be formed on the first carrier substrate 310, and the interface insulation layer 312 may bond the first carrier substrate 310 to the second substrate 210 to contact an upper surface of the first wiring insulation layer 230_1.

[0070] In embodiments, the interface insulation layer 312 may include at least one of silicon oxide, silicon nitride, silicon oxynitride, and silicon carbon nitride.

[0071] In some embodiments, the interface insulation layer 312 may be bonded to the first wiring insulation layer 230_1 by an oxide bonding process. In some embodiments, plasma treatment may be performed on a surface of each of the interface insulation layer 312 and the first wiring insulation layer 230_1. In some embodiments, surface treatment using a chemical material may be performed on the surface of each of the interface insulation layer 312 and the first wiring insulation layer 230_1. In some embodiments, high temperature annealing may be performed on the surface of each of the interface insulation layer 312 and the first wiring insulation layer 230_1.

[0072] Referring to FIG. 8, a structure where the second substrate 210 is bonded to the first carrier substrate 310 may be reversed.

[0073] Subsequently, a grinding process for removing a thickness of a portion of a surface of the second substrate 210 may be performed. The grinding process may be performed so that an upper surface (in the orientation shown in FIG. 8) of the via insulation layer 222 is exposed. A thickness of the second substrate 210 may be reduced by the grinding process.

[0074] Subsequently, a second interlayer insulation layer 234 may be formed on an upper surface of the second substrate 210. The second interlayer insulation layer 234 may be formed to cover the upper surface of the second substrate 210 and an entire upper surface of the via insulation layer 222.

[0075] Referring to FIGS. 9A and 9B, a cell transistor CTR may be formed on the second carrier substrate 320. For example, a channel layer AP, a word line WL, a back gate line BG, and a gate insulation layer GI, which are elements of the cell transistor CTR, may be first formed.

[0076] In embodiments, the channel layer AP may extend in a vertical direction Z, and the gate insulation layer GI may be formed at each of both sides of the channel layer AP. Subsequently, the word line WL may be formed on one sidewall of the channel layer AP with

the gate insulation layer GI therebetween, and the back gate line BG may be formed on the other sidewall of the channel layer AP with the gate insulation layer GI therebetween.

[0077] In some embodiments, an interface insulation layer 322 may be disposed between the second carrier substrate 320 and the channel layer AP. In embodiments, the second carrier substrate 320, the interface insulation layer 322, and the channel layer AP may be a portion of a wafer of a silicon-on-insulator (SOI) type. For example, the wafer of the SOI type where the interface insulation layer 322 and a silicon layer are disposed on the second carrier substrate 320 may be provided, and the channel layer AP may be formed by patterning the silicon layer.

[0078] In other embodiments, the second carrier substrate 320 may be provided as a wafer of a bulk silicon type. The interface insulation layer 322 may be formed on the second carrier substrate 320, and the channel layer AP may be formed on the interface insulation layer 322 by an epitaxial process, a chemical vapor deposition (CVD) process, and an atomic layer deposition (ALD) process.

[0079] In embodiments, the cell transistor CTR may be formed on the second carrier substrate 320, and a second buried insulation layer 134_2 covering the cell transistor CTR may be formed.

[0080] Subsequently, a cell capacitor CAP may be formed on the cell transistor CTR and the second buried insulation layer 134_2. In embodiments, a first electrode 122 extending in a vertical direction Z may be formed on each channel layer AP (or on a landing pad LP connected to the channel layer AP), and a capacitor dielectric layer 124 and a second electrode 126 may be sequentially formed on the first electrode 122.

[0081] Subsequently, a first buried insulation layer 134_1 covering the cell capacitor CAP may be formed. In embodiments, the first buried insulation layer 134_1 may include a plurality of insulation layers. For example, a second wiring 136_3 may be formed on each of a

plurality of insulation layers configuring the first buried insulation layer 134_1, and a second contact 136_4 passing through at least one of the plurality of insulation layers configuring the first buried insulation layer 134_1 may be formed.

[0082] Here, the first buried insulation layer 134_1 and the second buried insulation layer 134_2 may be referred to as a buried insulation layer 134.

[0083] Referring to FIG. 10, a first substrate 110 may be attached to the buried insulation layer 134. For example, the first substrate 110 may be attached to the buried insulation layer 134 with the interface insulation layer 132 therebetween.

[0084] In embodiments, the interface insulation layer 132 may be formed on the first substrate 110, and the interface insulation layer 132 may bond the second carrier substrate 320 to the first substrate 110 to contact an upper surface of the buried insulation layer 134 (e.g., the first buried insulation layer 134_1 (see FIG. 9B)).

[0085] In embodiments, the interface insulation layer 132 may include at least one from among silicon oxide, silicon nitride, silicon oxynitride, and silicon carbon nitride.

[0086] In some embodiments, the interface insulation layer 132 may be bonded to the buried insulation layer 134 by an oxide bonding process. In some embodiments, plasma treatment may be performed on a surface of each of the interface insulation layer 132 and the buried insulation layer 134. In some embodiments, surface treatment using a chemical material may be performed on the surface of each of the interface insulation layer 132 and the buried insulation layer 134. In some embodiments, high temperature annealing may be performed on the surface of each of the interface insulation layer 132 and the buried insulation layer 134.

[0087] Referring to FIG. 11, a structure where the first substrate 110 is bonded to the second carrier substrate 320 may be reversed.

[0088] Referring to FIG. 12, the second carrier substrate 320 (see FIG. 11) may be removed. In embodiments, the second carrier substrate 320 may be removed by performing a

grinding process and/or an etching process so that an upper surface of the interface insulation layer 322 is exposed.

[0089] Subsequently, an upper surface of each of the buried insulation layer 134 and a plurality of channel layers AP may be exposed by removing the interface insulation layer 322.

[0090] In some embodiments, a source/drain region may be formed in an upper side of each of the plurality of channel layers AP by implanting an impurity ion into a portion of the upper surface of each of the plurality of channel layers AP.

[0091] Referring to FIG. 13, a bit line BL extending in a first horizontal direction X may be formed on the upper surface of each of the plurality of channel layers AP. The bit line BL may be electrically connected to a set of channel layers AP which are disposed apart from one another in the first horizontal direction X.

[0092] Subsequently, the first contact 136_2 (see FIG. 4) and a wiring structure 136 (e.g., the first wiring 136_1 electrically connected to the bit line BL, the word line WL, and the back gate line BG) (see FIG. 4) electrically connected to the bit line BL, the word line WL, and the back gate line BG may be formed, and a third buried insulation layer 134_3 covering the bit line BL, the first wiring 136_1, and the first contact 136_2 may be formed.

[0093] Referring to FIG. 14, the first carrier substrate 310 may be bonded to the first substrate 110.

[0094] In embodiments, the first carrier substrate 310 may be bonded to the first substrate 110 so that the second substrate 210 is disposed at a vertical level which is higher than a vertical level of the cell transistor CTR disposed on the first substrate 110.

[0095] In embodiments, a peripheral circuit transistor PTR may be disposed on the upper surface of the second substrate 210, and the second interlayer insulation layer 234 may be disposed on a lower surface of the second substrate 210. Here, the second substrate 210 may be disposed at a vertical level which is higher than a vertical level of the first substrate 110 so

that the second interlayer insulation layer 234 is disposed on an upper surface of the buried insulation layer 134 (e.g., the third buried insulation layer 134_3). A lower surface of the second interlayer insulation layer 234 may contact the upper surface of the buried insulation layer 134.

[0096] In embodiments, the second interlayer insulation layer 234 may be bonded to the buried insulation layer 134 by an oxide bonding process. In some embodiments, plasma treatment may be performed on a surface of each of the second interlayer insulation layer 234 and the buried insulation layer 134. In some embodiments, surface treatment using a chemical material may be performed on the surface of each of the second interlayer insulation layer 234 and the buried insulation layer 134. In some embodiments, high temperature annealing may be performed on the surface of each of the second interlayer insulation layer 234 and the buried insulation layer 134.

[0097] Referring to FIG. 15, the first carrier substrate 310 (see FIG. 14) may be removed. In embodiments, the first carrier substrate 310 may be removed by performing a grinding process and/or an etching process so that the upper surface of the interface insulation layer 312 (see FIG. 14) is exposed.

[0098] Subsequently, an upper surface of the first wiring insulation layer 230_1 may be exposed by removing the interface insulation layer 312.

[0099] Referring to FIG. 16, a mask pattern may be formed on an upper surface of the first wiring insulation layer 230_1, and a portion of the first wiring insulation layer 230_1 and a portion of the via insulation layer 222 may be removed using the mask pattern as an etch mask, and then, a through via contact 220 may be formed by filling a conductive material in a region from which each of the portion of the first wiring insulation layer 230_1 and the portion of the via insulation layer 222 have been removed. The through via contact 220 may pass through the first wiring insulation layer 230_1 and the via insulation layer 222 and may extend

in the vertical direction Z. The through via contact 220 may be disposed on the cell wiring structure 136 and may be electrically connected to the cell wiring structure 136.

[0100] Referring to FIG. 17, a mask pattern may be formed on the upper surface of the first wiring insulation layer 230_1, and a through via hole H12 passing through a portion of the first wiring insulation layer 230_1, a portion of the second substrate 210, a portion of the second interlayer insulation layer 234, a portion of the buried insulation layer 134, and a portion of the first substrate 110 may be formed using the mask pattern as an etch mask. For example, the through via hole H12 may pass through the second substrate 210 and may extend in the vertical direction Z, and the through via hole H12 may not pass all the way through the first substrate 110.

[0101] Referring to FIG. 18, a through via insulation layer 12I may be formed on an inner wall of the through via hole H12. The through via insulation layer 12I may include silicon oxide, silicon nitride, or silicon oxynitride.

[0102] In embodiments, the through via insulation layer 12I may be formed on the through via hole H12 to have a relatively uniform thickness.

[0103] Referring to FIG. 19, a through via 12 may be formed in the through via hole H12.

[0104] In embodiments, the through via 12 may be formed by an electroplating process or an electroless plating process using copper or a copper alloy. In embodiments, before the through via 12 is formed, a seed layer may be further formed on an inner wall of the through via hole H12 by a sputtering process using copper, titanium, silver, or platinum.

[0105] Referring to FIG. 20, a wiring pattern WP and a wiring insulation layer 230 may be formed on an upper surface of the through via 12. A portion of the wiring pattern WP and a portion of the wiring insulation layer 230 may be disposed at positions vertically overlapping

with the through via 12, and the wiring pattern WP may be electrically connected to the through via 12.

[0106] Subsequently, a lower pad UWP electrically connected to the wiring pattern WP may be formed on the wiring insulation layer 230. A third interlayer insulation layer 238 may be formed on the lower pad UWP, and a front-side insulation layer 14I may be formed on the third interlayer insulation layer 238.

[0107] Subsequently, a front-side pad opening portion may be formed by removing a portion of each of the front-side insulation layer 14I and the third interlayer insulation layer 238, and a front-side pad 14P may be formed in the front-side pad opening portion.

[0108] In embodiments, the front-side pad 14P may be formed by an electroplating process or an electroless plating process using copper or a copper alloy. In embodiments, before the front-side pad 14P is formed, a seed layer may be further formed on an inner wall of the front-side pad opening portion by a sputtering process using copper, titanium, silver, or platinum.

[0109] In embodiments, by performing a planarization process such as a chemical mechanical polishing process on an upper side of the front-side pad 14P, a portion of the upper side of the front-side pad 14P may be removed so that an upper surface of the front-side pad 14P and an upper surface of the front-side insulation layer 14I are disposed coplanar with each other.

[0110] Referring to FIG. 21, a partial thickness of the first substrate 110 may be removed from a lower surface of the first substrate 110. In embodiments, a process for removing a portion of the lower surface of the first substrate 110 may be a grinding process. In embodiments, the grinding process may be performed so that a lower surface of the through via insulation layer 12I disposed on a lower surface of the through via 12 is exposed. In other embodiments, in a state where the lower surface of the through via insulation layer 12I is

exposed after the grinding process, an etching process for further removing a partial thickness of the first substrate 110 from the lower surface of the first substrate 110 may be further performed.

[0111] In embodiments, a portion of the through via insulation layer 12I disposed at the lower surface of the through via 12 may be removed, and the lower surface of the through via 12 may be exposed. In embodiments, the lower surface of the through via 12 may be disposed at a level which is lower than a level of the lower surface of the first substrate 110, and the lower surface of the through via 12 may protrude downward with respect to the lower surface of the first substrate 110.

[0112] Subsequently, a first interlayer insulation layer 138 may be formed to have a sufficient thickness for covering a bottom portion of the through via 12 on the lower surface of the first substrate 110. Subsequently, a backside insulation layer 16I may be formed on a lower surface of the first interlayer insulation layer 138.

[0113] A backside pad opening portion again exposing the lower surface of the through via 12 may be formed by removing a portion of the backside insulation layer 16I and a portion of the first interlayer insulation layer 138, and a backside pad 16P may be formed in the backside pad opening portion.

[0114] In embodiments, the backside pad 16P may be formed by an electroplating process or an electroless plating process using copper or a copper alloy. In embodiments, before the backside pad 16P is formed, a seed layer may be further formed on an inner wall of the backside pad opening portion by a sputtering process using copper, titanium, silver, or platinum.

[0115] In embodiments, by performing a planarization process such as a chemical mechanical polishing process on a bottom portion of the backside pad 16P, a portion of a lower side of the backside pad 16P may be removed so that a lower surface of the backside pad 16P and a lower surface of the backside insulation layer 16I are disposed coplanar with each other.

[0116] By performing the process described above, one semiconductor die 10 may be formed. According to embodiments, the process may be performed multiple times to form a plurality of the semiconductor dies 10.

[0117] Referring to FIGS. 22A and 22B, one semiconductor die 10 (e.g., a first die C1) may be bonded to another semiconductor die 10 (e.g., a second die C2).

[0118] A process of bonding the first die C1 to the second die C2 may include a metal-oxide hybrid bonding process. In embodiments, a front-side pad 14P included in the first die C1 may contact a backside pad 16P included in the second die C2, and a front-side insulation layer 14I included in the first die C1 may contact a backside insulation layer 16I included in the second die C2.

[0119] In this manner, a plurality of semiconductor dies 10 may be stacked in the vertical direction Z by a metal-oxide hybrid bonding process, and thus, the semiconductor device 1 described above with reference to FIGS. 1 to 4 may be manufactured.

[0120] According to embodiments, each of the semiconductor dies 10 may include the cell transistor CTR of the vertical channel transistor type disposed on the first substrate 110, the peripheral circuit transistor PTR disposed on the second substrate 210, and the through via 12 passing through the first substrate 110, the buried insulation layer 134, and the second substrate 210, and the plurality of semiconductor dies 10 may be stacked in the vertical direction Z through the front-side pad 14P and the backside pad 16P. The semiconductor device 1 may be high in degree of integration, and moreover, may have good electrical performance.

[0121] According to an embodiment, each semiconductor die may include a vertical channel transistor disposed on a first substrate and a peripheral circuit transistor disposed on a second substrate and may also include a through via passing through the first substrate and the second substrate, and a plurality of dies may be stacked in a vertical direction and connected

by a front-side pad and a backside pad. The semiconductor device may be high in degree of integration, and moreover, may have good electrical performance.

[0122] Hereinabove, non-limiting example embodiments have been described with reference to the accompanying drawings. Embodiments have been described by using the terms described herein, but these terms have been merely used for describing example embodiments and have not been used for limiting a meaning or limiting the scope of the disclosure. Therefore, it may be understood by those of ordinary skill in the art that various modifications and other equivalent embodiments may be included in the scope of the disclosure.

[0123] While non-limiting example embodiments have been described with reference to the accompanying drawings, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
a plurality of dies stacked in a vertical direction,
wherein each of the plurality of dies comprises:
a first substrate;
a cell capacitor on the first substrate;
a cell transistor on the cell capacitor;
a second substrate, wherein a vertical level of the second substrate is higher than
a vertical level of the cell transistor;
a peripheral circuit transistor on the second substrate; and
a through via passing through the first substrate and the second substrate in the
vertical direction.
2. The semiconductor device of claim 1, wherein each of the plurality of dies
further comprises:
a wiring pattern that at least partially vertically overlaps with the through via, wherein
a vertical level of the wiring pattern is higher than a vertical level of the peripheral circuit
transistor;
a front-side pad on an upper surface of the wiring pattern; and
a backside pad on a lower surface of the through via.
3. The semiconductor device of claim 2, wherein the plurality of dies comprise a
first die and a second die on the first die, and
the through via of the first die and the through via of the second die are electrically
connected to each other, and the second die is on an upper surface of the first die such that the
backside pad of the second die is attached to the front-side pad of the first die.

4. The semiconductor device of claim 2, wherein each of the plurality of dies further comprises:

a front-side insulation layer on the upper surface of the wiring pattern, and an upper surface of the front-side insulation layer is coplanar with an upper surface of the front-side pad; and

a backside insulation layer on a lower surface of the first substrate, and a lower surface of the backside insulation layer is coplanar with a lower surface of the backside pad,

the plurality of dies comprise a first die and a second die on the first die, and

the upper surface of the front-side insulation layer of the first die contacts a lower surface of the backside insulation layer of the second die.

5. The semiconductor device of any one of claims 1 to 4, wherein each of the plurality of dies further comprises a through via contact extending in the vertical direction in a via hole passing through the second substrate and electrically connecting the peripheral circuit transistor to the cell transistor.

6. The semiconductor device of any one of claims 1 to 5, wherein the cell transistor comprises:

a channel layer extending in the vertical direction;

a word line on one sidewall of the channel layer and extending in a first horizontal direction; and

a bit line on an upper surface of the channel layer and extending in a second horizontal direction intersecting with the first horizontal direction.

7. The semiconductor device of claim 6, wherein the channel layer comprises silicon, germanium, silicon germanium, or an oxide semiconductor.

8. The semiconductor device of claim 1, wherein each of the plurality of dies further comprises a through via insulation layer surrounding a sidewall of the through via,

the first substrate comprises a first through via hole passing through the first substrate,

the second substrate comprises a second through via hole passing through the second substrate, the second through via hole vertically overlapping with the first through via hole, and

the through via is vertically overlapping with the first through via hole and the second through via hole.

9. The semiconductor device of claim 8, wherein the through via comprises an upper surface, wherein a vertical level of the upper surface of the through via is higher than a vertical level of an upper surface of the second substrate, and

the through via comprises a lower surface, wherein a vertical level of the lower surface of the through via is lower than a vertical level of a lower surface of the first substrate.

10. The semiconductor device of claim 8, wherein the through via insulation layer comprises an upper surface, wherein a vertical level of the upper surface of the through via insulation layer is higher than a vertical level of an upper surface of the second substrate, and

the through via insulation layer comprises a lower surface, wherein a vertical level of the lower surface of the through via insulation layer is lower than a vertical level of a lower surface of the first substrate.

11. The semiconductor device of any one of claims 8 to 10, wherein a first portion of the through via insulation layer is between the sidewall of the through via and an inner wall of the first through via hole,

a second portion of the through via insulation layer is between the sidewall of the through via and an inner wall of the second through via hole, and

the through via is electrically insulated from the first substrate or the second substrate.

12. The semiconductor device of any one of claims 8 to 11, wherein each of the plurality of dies further comprises:

a buried insulation layer between the first substrate and the second substrate and on the cell transistor,

the through via insulation layer is on an entire sidewall of the through via, and

at least a portion of a sidewall of the through via insulation layer contacts the buried insulation layer.

13. A semiconductor device comprising:

a first die; and

a second die on the first die,

wherein each of the first die and the second die comprises:

a first substrate;

a cell capacitor on the first substrate;

a cell transistor on the cell capacitor;

a second substrate, wherein a vertical level of the second substrate is higher than a vertical level of the cell transistor;

a peripheral circuit transistor on the second substrate;

a through via passing through the first substrate and the second substrate in a vertical direction;

a wiring pattern that at least partially vertically overlaps with the through via, wherein a vertical level of the wiring pattern is higher than a vertical level of the peripheral circuit transistor;

a front-side pad on an upper surface of the wiring pattern; and

a backside pad on a lower surface of the through via.

14. The semiconductor device of claim 13, wherein each of the first die and the second die further comprises:

a front-side insulation layer on the upper surface of the wiring pattern, wherein an upper surface of the front-side insulation layer is coplanar with an upper surface of the front-side pad; and

a backside insulation layer on a lower surface of the first substrate, wherein a lower surface of the backside insulation layer is coplanar with a lower surface of the backside pad; and

a buried insulation layer between the first substrate and the second substrate and on the cell transistor, at least a portion of the through via passing through the buried insulation layer.

15. The semiconductor device of claim 14, wherein the backside pad of the second die contacts the front-side pad of the first die, and

the lower surface of the backside insulation layer of the second die contacts the upper surface of the front-side insulation layer of the first die.

16. The semiconductor device of any one of claims 13 to 15, wherein the through via of the first die is electrically connected to the through via of the second die.

17. The semiconductor device of any one of claims 13 to 16, wherein each of the first die and the second die further comprises a through via contact extending in the vertical direction in a via hole passing through the second substrate and electrically connecting the peripheral circuit transistor to the cell transistor.

18. The semiconductor device of any one of claims 13 to 17, wherein the cell transistor comprises:

- a channel layer extending in the vertical direction;

- a word line on one sidewall of the channel layer and extending in a first horizontal direction; and

- a bit line, wherein a vertical level of the bit line is higher than a vertical level of the channel layer, and the bit line extends in a second horizontal direction intersecting with the first horizontal direction.

19. A semiconductor device comprising:

- a first substrate including a first through via hole;

- a cell capacitor on the first substrate;

- a cell transistor on the cell capacitor;

- a second substrate, wherein a vertical level of the second substrate is higher than a vertical level of the cell transistor, and the second substrate includes a second through via hole that vertically overlaps with the first through via hole;

- a peripheral circuit transistor on the second substrate;

a through via contact extending in a vertical direction in a via hole passing through the second substrate, and the through via contact electrically connects the peripheral circuit transistor to the cell transistor;

a through via passing through the first through via hole and the second through via hole in the vertical direction;

a through via insulation layer on a sidewall of the through via;

a wiring pattern at least partially vertically overlapping with the through via, wherein a vertical level of the wiring pattern is higher than a vertical level of the peripheral circuit transistor;

a front-side pad on an upper surface of the wiring pattern;

a front-side insulation layer on the upper surface of the wiring pattern, and an upper surface of the front-side insulation layer being coplanar with an upper surface of the front-side pad;

a backside pad on a lower surface of the through via; and

a backside insulation layer on a lower surface of the first substrate, and a lower surface of the backside insulation layer being coplanar with a lower surface of the backside pad.

20. The semiconductor device of claim 19, wherein the cell transistor comprises:

a channel layer extending in the vertical direction;

a word line on one sidewall of the channel layer and extending in a first horizontal direction; and

a bit line, wherein a vertical level of the bit line is higher than a vertical level of the channel layer, and the bit line extends in a second horizontal direction intersecting with the first horizontal direction.