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COMPLETE SPECIFICATION

Semiconductor Integrated Circuit Arrangement

We, SHARP KABUSHIKI KAISHA, formerly Hayakawa Denikogyo Kabushiki Kaisha, a Japanese Company, of 22—22 Nagaike-cho, Abeno-ku, Osaka-shi, Osaka-fu, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

10 This invention relates to a semiconductor integrated circuit arrangement, especially to an improved semiconductor integrated circuit arrangement which is arranged so that many kinds of circuit function can be exhibited by a single circuit configuration.

15 Recently, the integration of a semiconductor circuit has been extensively investigated from many points of view. This tendency is especially to be noted in the field of electronic computers (of the table type) and various investigations have been made in connection with many kinds of digital circuit for electronic computers. Especially, substantial development according to purpose has been
20 made up to now in connection with gates, inverters and the other circuits using MOS (metal oxide semiconductor) field effect transistors. However, most of those semiconductor integrated circuits have only one respective circuit function according to their purposes. To constitute a complicated circuit such as an electronic computer including such semiconductor integrated circuits each having a single function, necessarily has an unavoidable defect such that many kinds of, and also
30 a number of, semiconductor integrated circuits must be used in combination. Especially since, in the manufacture of a semiconductor integrated circuit, one evaporation mask cannot be used commonly many times but can
40 make only a few units, the manufacturing

cost per semiconductor integrated circuit device is very expensive.

Accordingly, an object of this invention is to provide an improved semiconductor integrated circuit device constituted so as to be capable of exhibiting many kinds of function.

Another object of this invention is to integrate a number of semiconductor devices on a single semiconductor substrate to provide a circuit arrangement which can operate as a whole as a single integrated circuit device having many kinds of function.

According to the invention there is provided a semiconductor integrated circuit arrangement having a substrate of one conductivity type, a plurality of MOS type field effect transistors each having semiconductor layers of the other conductivity type providing source and drain electrodes formed thereon and a metal layer which can be used as the control or gate electrode deposited on an insulating layer on a portion between the source and drain electrodes, a plurality of terminals connected to said electrodes on said substrate, and a semiconductor region having said one conductivity type but higher conductivity and usable as a substrate electrode is formed on the semiconductor substrate and a conductor to be attached to said semiconductor region is independently provided as a single external terminal without being commonly connected to any other portion of the circuit, the whole arrangement being such that a plurality of MOS field effect transistors having no D.C. coupling between the substrate and the source (or drain) electrode are formed. A circuit device according to this invention is constituted so as to be able to execute as many functions as possible by making mutual connections between a plurality of internal elements feasible. The circuit device according to this in-

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vention has a plurality of terminals and can be easily used as a gate, inverter or other circuit used in a digital device by properly selecting input and output terminals, source terminals and grounding terminals. In other words, the abovementioned terminals of a prior device only have their inherent functions but each terminal of a device of this invention may be, for example, an input terminal or a source terminal in accordance with the purpose for which it is to be used.

In order that the invention may be clearly understood and readily carried into effect apparatus in accordance therewith will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a fundamental structural diagram of a MOS field effect transistor integrated circuit device;

Figure 2 is a circuit diagram representing an embodiment of a semiconductor integrated circuit arrangement according to this invention;

Figures 3(A) to 3(D) are circuit diagrams representing applications thereof;

Figure 4 is a circuit diagram representing another embodiment according to this invention;

Figures 5(A) to 5(F) are circuit diagrams representing applications thereof;

Figure 6 is a circuit diagram representing a further embodiment according to this invention; and

Figures 7(A) to 7(E) are circuit diagrams representing applications thereof.

Referring to Figures 1, P-type diffusion layers 2 and 3 which can serve as the source electrode and the drain electrode respectively are deposited on a surface of a N-type semiconductor substrate 1 and a metal layer 5 which can serve as the gate electrode is moreover deposited on an insulating oxide layer 4 bridging said P-type diffusion layers 2 and 3. This device includes a substrate terminal 6 attached to the semiconductor substrate 1 through a N⁺-type diffusion layer, a source terminal 7, a drain terminal 8 and a gate terminal 9. The substrate terminal 6 is taken out of the integrated device as one terminal similar to the other terminals 7, 8 and 9. Thereby, the non-directionality of a field effect transistor is utilised. The d.c. coupling between the gate terminal 9 and the source terminal 7 or the drain terminal 8 is removed and many circuit functions are obtainable in the vertical and horizontal directions.

In Figure 2, for the purpose of simplification of the description, the respective structural elements are field effect transistors of the P-channel enhancement type, in which zero volt corresponds to a binary "1" and $-V_{DD}$ volt corresponds to a binary "0". This device includes ten MOS field effect transistors and is provided with fifteen terminals A_1 to S_1 connected to the respective elec-

trode terminals of the respective transistors and serving as external terminals having no specific application in a semiconductor integrated circuit device. S_1 is an independent terminal which is directly attached to the semiconductor substrate. In a field effect transistor, it is necessary to apply a reverse bias between the substrate and the source or the drain, and, therefore, the substrate must be put at the highest potential within the circuit, that is zero potential. This circuit device can provide many circuit functions such as 2 "and"—2 "or" gate, 3 "and" gate, 4 "and"—2 "or" gate, inverter, amplifier, gates for addition and subtraction, etc., by properly selecting input and output terminals, source terminals and the like from the above terminals.

This circuit comprises two sets of symmetric circuits, said each set comprising five field effect transistors and having an internal connection as follows. The first electrode and the third electrode of the first structural element T_{11} are mutually connected and the second electrode thereof is connected to the third electrode of the second structural element T_{12} . The first electrode and the second electrode of the second structural element T_{12} are led out as the external terminals A_1 and F_1 respectively. The first electrode and the third electrode of the third structural element T_{13} are mutually connected and this joint is connected to the joint of the first electrode and the third electrode of the first structural element T_{11} and moreover led out as the external terminal K_1 . The second electrode of the third structural element T_{13} is connected to the third electrode of the fourth structural element T_{14} and this joint is led out as the external terminal J_1 . The first electrode of the fourth element T_{14} , the respective third electrodes of the second and fifth structural elements T_{12} and T_{15} and the second electrode of the first structural element T_{11} are connected in common and further led out as the external terminal M_1 . The second electrode of the fourth structural element T_{14} and the first and second electrodes of the fifth structural element T_{15} are led out as the separate external terminals E_1 , B_1 and G_1 respectively. Applied examples of this circuit device will be described below.

The circuit arrangement of the other set which includes the structural elements T_{16} — T_{20} corresponds to that of the set which includes the structural elements T_{11} — T_{15} . In such circuit as the above, the second and the third electrodes aside from the first or control electrode are not designated as the source region or the drain region respectively and the choice is up to the users. Further, the substrate in said circuit is taken out of the container independently by an external terminal, and, therefore, at the time of voltage application between, for example, the second

electrode of the structural element T_{12} and the third electrode of the structural element T_{11} there is no restriction for the application of reverse bias between the substrate and the source or drain region.

EXAMPLE 1

As shown in Figure 3(A), the terminal K_1 is connected to the potential source $-V_{DD}$ and the terminal E_1 is grounded. If the terminals $A_1, B_1, C_1, D_1, F_1, G_1, H_1$ and I_1 are used as input terminals and the terminals M_1, N_1, J_1 and L_1 are used as output terminals, logic equations are as follows, the subindexes "1" being omitted in the equations.

$$\begin{aligned} M &= \bar{A}F + \bar{B}G \\ N &= \bar{C}H + \bar{D}I \\ J &= \bar{M} = \bar{A}F \cdot \bar{B}G = (A + \bar{F})(B + \bar{G}) \\ L &= \bar{N} = \bar{C}H \cdot \bar{D}I = (C + \bar{H})(D + \bar{I}) \end{aligned}$$

That is, a circuit function of an amplifier comprising a 2 "and"-2 "or" (one of said two "and" gates includes a NO signal) exclusive logic gate, an inverter and a two stage inverter is provided based upon an "and" circuit and a "nand" circuit.

EXAMPLE 2

As shown in Figure 3(B), in the arrangement of Example 1, the terminals M_1 and N_1 are connected to each other and the terminals M_1, N_1, J_1 and L_1 are used as output terminals. Then, logic equations are as follows.

$$\begin{aligned} M &= N = \bar{A}F + \bar{B}G + \bar{C}H + \bar{D}I \\ J &= L = \bar{M}(A + \bar{F})(B + \bar{G})(C + \bar{H})(D + \bar{I}) \end{aligned}$$

That is, as the whole, circuit functions of 2 "and"-2 "or" gate (input of said two "and" gates is a truth signal), 3 "and" and 4 "and" gates (both truth and NO signals are possible) are provided.

EXAMPLE 3

As shown in Figure 3(C), in the arrangement of Example 2, the connection between the terminals M_1 and N_1 is released. Under this condition, a complementary signal of Example 2 can be derived even if the two stage inverter is removed. That is, if two inputs are a_1 and a_2 and $A_1 = G_1 = a_1, B_1 = F_1 = a_2, M_1 = C_1 = I_1$ and $H_1 = D_1 = FC$ carry output derived from carry flip-flop, and this carry from the lower position is applied to the adder as an adder input same as said two inputs a_1 and a_2 , the next signal is derived from the terminal N_1 and a circuit function of a pure binary three-input adder is provided.

$$FA = a_1 a_2 FC + \bar{a}_1 a_2 FC + a_1 \bar{a}_2 FC + a_1 a_2 \bar{F}C$$

In the case that these connections in the

source side are also used as input terminals, if a logic constituted of a transistor whose drain side is common to that of said transistor is an exclusive logic, it is necessary to insert a diode whose cathode is in the source side. That is a purpose of preventing an influence of a signal applied from one of the source sides to a signal supply circuit to the other source side.

EXAMPLE 4

As shown in Figure 3(D), the terminals K_1, F_1, G_1, H_1 and I_1 are grounded, the terminals $J_1, M_1, L_1, N_1, A_1, B_1, C_1$ and D_1 are used as input terminals and the terminal E_1 is connected to the source $-V_{DD}$ and used as an output terminal. Then, a logic equation is as follows.

$$E = JMAB + LNCD$$

That is, a circuit function of 4 "and"-2 "or" gate including one NO signal is provided. If the terminals M_1 and N_1 are moreover opened, a following equation is established and a 3 "and"-2 "or" gate according to only truth signal is constituted.

$$E = JAB + LCD$$

In any case of the above, it is necessary to add resistors to the outsides of the terminals M_1, N_1 and E_1 and, in the case that the source of the transistor is used as an input terminal, it is necessary to insert a diode. Observing the structural element T_{14} , for example, in such circuit as the above, its second electrode directly coupled to the external terminal E is operating as the source region (or electrode) in the configuration of Figure 3(A), but in the configuration shown in Figure 3(D) the second electrode is working as the drain region (or electrode). Thus, the interchangeability of the source and the drain is effectively utilized.

An arrangement shown in Figure 4 is another embodiment of a semiconductor integrated circuit arrangement according to this invention which is constituted of twelve MOS field effect transistors T_{21} to T_{32} and has twelve external terminals A_2 to S_2 . S_2 is a terminal which is directly attached to the semiconductor substrate and is taken out of the container as an independent terminal. This circuit can provide circuit functions of dynamic memory, static memory, inverter and the like by properly selecting input and output terminals, source terminals and grounding terminals.

This circuit comprises four sets of symmetric circuits, said set comprising three field effect transistors and having internal connection as follows. The first electrode and the third electrode of the first structural element T_{21} are mutually connected and led out as the external terminal E_2 . The second electrode of the first structural element T_{21} is con-

connected to the third electrode of the second structural element T_2 and led out as the external terminal A_2 . The first electrode of the second structural element T_{22} is connected to the third electrode of the third structural element T_{23} . The second electrode of the third structural element T_{23} is independently led out as the external terminal G_2 . The second electrode of the second structural element T_{22} and the first electrode of the third structural element T_{23} are respectively connected to conductors which are common to the respective sets, and led out as the external terminals K_2 and F_2 respectively.

EXAMPLE 5

Figure 5(A) represents an arrangement using two of the arrangements of Figure 4, in which terminals belonging to the first arrangement are indicated as A_{21} , B_{21} , ... and corresponding terminals belonging to the second arrangement are indicated as A_{22} , B_{22} , ... Symbols A_2 , B_2 , ... obtained by removing the second indexes correspond to the terminals of the same symbols of Figure 4. Primes are attached to the structural elements of the second set.

The terminal E_2 is connected to the source $-V_{DD}$ and the terminal K_2 is grounded. The terminal G_{21} is used as an input terminal and the terminals A_{21} and G_{22} , A_{22} and H_{21} , B_{21} and H_{22} , B_{22} and I_{21} , C_{21} and I_{22} , C_{22} and J_{21} , and D_{21} and J_{22} are respectively connected to each other. When a synchronizing signal ϕ_1 is supplied to one terminal F_{21} and another synchronizing signal ϕ_2 having different phase is supplied to the other terminal F_{22} , this circuit operates as a four bit dynamic memory (flip-flop) and its output is derived from the terminal D_{22} . Figure 5(B) is a chart representing phase relationship of said synchronizing signals ϕ_1 and ϕ_2 .

EXAMPLE 6

Using two of the arrangements of Figure 4, as in Example 5, reference symbols are given to the respective terminals in accordance with Example 5. As shown in Figure 5(C) by a part thereof, the terminals E_{21} and F_{21} are connected to the source $-V_{DD}$ and the terminals K_{21} , K_{22} and E_{22} are grounded. The terminals A_{21} and H_{21} , B_{21} and G_{21} , C_{21} and J_{21} , and D_{21} and I_{21} are respectively connected to each other and the synchronizing signal ϕ_1 is supplied to the terminal F_{22} . Further, the terminals A_{22} and G_{21} , B_{22} and H_{21} , C_{22} and I_{21} , and D_{22} and J_{21} are mutually respectively connected. The terminals G_{22} , H_{22} , I_{22} and J_{22} are used as input terminals and the terminals A_{21} , B_{21} , C_{21} and D_{21} are used as output terminals. Thereby, a two-bit static flip-flop is provided. However, there is shown in the drawing one-bit static flip-flop only. In this case, four symmetric circuit arrangements each including at least three struc-

tural elements are necessary to constitute a one-bit memory. In this case, moreover, since the source $-V_{DD}$ is always applied to the first electrode of the structural elements T_{23} , T_{26} in the first arrangement, said two structural elements only serve as conductors. Since the first and third electrodes of the structural elements T'_{23} , T'_{21} , T'_{24} of the second arrangement are grounded, on the other hand, said structural elements are opened and these two elements T_{23} and T_{26} do not perform special circuit operations.

EXAMPLE 7

As shown in Figure 5(D), in the arrangement of Figure 4, the terminals G_2 , H_2 , I_2 and J_2 are used as input terminals and the terminals A_2 , B_2 , C_2 and D_2 are used as output terminals. Thus, four inverters are obtained. Provided, the terminal F_2 is connected to the source $-V_{DD}$. The terminal K_2 is grounded.

EXAMPLE 8

As shown in Figure 5(E), in the arrangement of Figure 4, the terminals E_2 and K_2 are grounded. If a dynamic input pulse is supplied to the terminals G_2 , H_2 , I_2 and J_2 and a time selection signal T_1 is supplied to the terminal F_2 , delayed output signals are obtained from the output terminals A_2 , B_2 , C_2 and D_2 by a storing action of field effect transistor. Said delayed output signals can be utilized as driving signals in the case that a memory content of the dynamic memory is indicated by a display tube of the time division control type. That is, this semiconductor integrated circuit arrangement provides a display tube driving circuit device. In this case, however, the structural elements T_{21} , T_{24} , T_{27} , ... are redundant.

EXAMPLE 9

As shown in Figure 5(F), when the terminal F_2 is connected to the source $-V_{DD}$ and the terminals A_2 , B_2 , C_2 , D_2 , G_2 , H_2 , I_2 and J_2 are used as input terminals. As a negative potential from the source $-V_{DD}$ is always being applied to the control electrode of the structural elements T_{23} , T_{26} , T_{29} and T_{32} , inputs from the terminals G_2 , H_2 , I_2 and J_2 as they are just pass through said structural elements to be transferred to the control electrodes of the structural elements T_{22} , T_{25} , T_{28} and T_{31} of the next stage. Thus, substantially same operation as that of the gate described in the Example 1 is performed, and the logic equation is given as follows.

$$K = \bar{G}A + \bar{H}B + \bar{I}C + \bar{J}D$$

That is, a 2 "and"-4 "or" gate is provided. In this case, it is necessary to connect diodes having their cathodes in the same terminal side as the abovementioned diodes in Example 3.

Now, referring to Figure 6, there is shown

a further embodiment of a semiconductor integrated circuit arrangement of this invention. This arrangement comprises twelve MOS type N-channel field effect transistors T_{41} to T_{52} and is provided with twelve terminals A_3 to S_3 having no specified use as the external terminals. By properly selecting input and output terminals, source terminals and the like from said terminals A_3 to S_3 , many circuit functions such as inverter, display tube driver, transistor gate, exclusive logic gate, etc. can be provided.

This circuit arrangement comprises four blocks of symmetric circuits, each of said blocks comprising three field effect transistors and having internal connection as follows. The first block including structural elements T_{41} , T_{42} and T_{43} will be explained. The first electrode of the first structural element T_{41} is connected to the third electrode of the third structural element T_{43} and the second electrode of the first structural element T_{41} is connected to the third electrode of the second structural element T_{42} and led out as the external terminal C_3 . The first electrode and the second electrode of the second structural element T_{42} are connected to the first electrode of the third structural element T_{43} and led out as the common external terminal L_3 . The second electrode of the third structural element T_{43} is led out as the external terminal D_3 . The third electrode of the first structural element T_{41} is connected to the third electrode of the first structural element T_{44} in the next block and further led out as the external terminal A_3 . The substrate is attached with the terminal S_3 . Said terminal S_3 is always grounded. This circuit arrangement can be used as follows:

EXAMPLE 10

The above arrangement operates as an inverter by use of terminal connection as follows. The terminals A_3 , B_3 and S_3 are grounded and the terminal L_3 is connected to a source V_{DD} . The terminals D_3 , F_3 , H_3 and J_3 are used as input signal receiving terminals and the terminals G_3 , E_3 , G_3 and I_3 are used as output terminals. For example, if an input signal a_1 is supplied to the terminal D_3 , the element T_{41} operates as a transistor inverter and the element T_{42} operates as its load resistor. An output signal a_1 is obtained from the terminal C_3 . This arrangement becomes equivalent to that of Figure 5(D) as abovementioned.

EXAMPLE 11

According to the following terminal connection, this arrangement operates as a display tube driver. The terminals A_3 , B_3 and S_3 are grounded. The terminals D_3 , F_3 , H_3 and J_3 are used as input signal receiving terminals, the terminal L_3 is used as a timing signal receiving terminal and the terminals

C_3 , E_3 , G_3 and I_3 are used as output terminals. One set of display tube drivers constituted of the structural elements T_{41} , T_{42} and T_{43} is shown in Figure 7(A) and its signal waveforms are shown in Figure 7(B).

In the case of supplying an input signal to the terminal D_3 and a timing signal to the terminal L_3 , since the structural element T_{43} is driven into the ON-state during a period in which the timing signal exists, the input signal is transmitted to a point X as it is. Said signal is stored at said point X due to an internal capacitance of the MOS field effect transistor also after completion of the timing signal, that is, after the structural element T_{43} is cut off. Thereby, this arrangement operates as a dynamic display tube driver and the element T_{42} operates as a load of the element T_{41} .

EXAMPLE 12

The terminal S_3 is grounded and the terminal L_3 is connected to the source V_{DD} . The terminals A_3 and B_3 are used as receiving terminals of the input signals a_1 and a_2 , respectively, and the terminals D_3 , F_3 , H_3 and J_3 are used as receiving terminals for condition input signals $\bar{j}_1$, $\bar{j}_2$, $\bar{j}_3$ and $\bar{j}_4$. Output signals a_1j_1 , a_1j_2 , a_2j_3 and a_2j_4 are obtained from the terminals C_3 , E_3 , G_3 and I_3 respectively. That is, as shown in Figure 7(C), the elements T_{41} to T_{46} provide a transistor gate added with switching elements for condition inputs. This is equivalently shown by a switching circuit as shown in Figure 7(D).

EXAMPLE 13

An exclusive "or" gate can be constituted by utilizing bidirectional property of MOS field effect transistor as follows. The terminal S_3 is grounded and the terminal L_3 is connected to the source V_{DD} . The terminals C_3 , D_3 , E_3 , F_3 , G_3 , H_3 , I_3 and J_3 are used as input terminals and the terminals A_3 and B_3 are used as output terminals. In this case, the terminals C_3 and F_3 , D_3 and E_3 , H_3 and I_3 , and G_3 and J_3 are used so as to be equivalent to each other. A gate circuit comprising the elements T_{41} to T_{46} is shown in Figure 7(E). If an input signal a_1 is supplied to the terminals C_3 and F_3 and an input signal b_1 is supplied to the terminals D_3 and E_3 , an output $a_1b_1 + a_1\bar{b}_1$ is obtained from the output terminal A_3 to which an external resistor R is connected.

As described in the above, this invention provides a single semiconductor integrated circuit arrangement having various possible uses and has advantageous features such as simplification of the manufacturing process, consolidation of manufacturing jigs and tools and manufacturing cost reduction resulting from mass production.

WHAT WE CLAIM IS:—

1. A semiconductor integrated circuit ar-

a further embodiment of a semiconductor integrated circuit arrangement of this invention. This arrangement comprises twelve MOS type N-channel field effect transistors T_{41} to T_{52} and is provided with twelve terminals A_3 to S_3 having no specified use as the external terminals. By properly selecting input and output terminals, source terminals and the like from said terminals A_3 to S_3 , many circuit functions such as inverter, display tube driver, transistor gate, exclusive logic gate, etc. can be provided.

This circuit arrangement comprises four blocks of symmetric circuits, each of said blocks comprising three field effect transistors and having internal connection as follows. The first block including structural elements T_{41} , T_{42} and T_{43} will be explained. The first electrode of the first structural element T_{41} is connected to the third electrode of the third structural element T_{43} and the second electrode of the first structural element T_{41} is connected to the third electrode of the second structural element T_{42} and led out as the external terminal C_3 . The first electrode and the second electrode of the second structural element T_{42} are connected to the first electrode of the third structural element T_{43} and led out as the common external terminal L_3 . The second electrode of the third structural element T_{43} is led out as the external terminal D_3 . The third electrode of the first structural element T_{41} is connected to the third electrode of the first structural element T_{44} in the next block and further led out as the external terminal A_3 . The substrate is attached with the terminal S_3 . Said terminal S_3 is always grounded. This circuit arrangement can be used as follows:

EXAMPLE 10

The above arrangement operates as an inverter by use of terminal connection as follows. The terminals A_3 , B_3 and S_3 are grounded and the terminal L_3 is connected to a source V_{DD} . The terminals D_3 , F_3 , H_3 and J_3 are used as input signal receiving terminals and the terminals G_3 , E_3 , G_3 and I_3 are used as output terminals. For example, if an input signal a_1 is supplied to the terminal D_3 , the element T_{41} operates as a transistor inverter and the element T_{43} operates as its load resistor. An output signal a_1 is obtained from the terminal C_3 . This arrangement becomes equivalent to that of Figure 5(D) as abovementioned.

EXAMPLE 11

According to the following terminal connection, this arrangement operates as a display tube driver. The terminals A_3 , B_3 and S_3 are grounded. The terminals D_3 , F_3 , H_3 and J_3 are used as input signal receiving terminals, the terminal L_3 is used as a timing signal receiving terminal and the terminals

C_3 , E_3 , G_3 and I_3 are used as output terminals. One set of display tube drivers constituted of the structural elements T_{41} , T_{42} and T_{43} is shown in Figure 7(A) and its signal waveforms are shown in Figure 7(B).

In the case of supplying an input signal to the terminal D_3 and a timing signal to the terminal L_3 , since the structural element T_{43} is driven into the ON-state during a period in which the timing signal exists, the input signal is transmitted to a point X as it is. Said signal is stored at said point X due to an internal capacitance of the MOS field effect transistor also after completion of the timing signal, that is, after the structural element T_{43} is cut off. Thereby, this arrangement operates as a dynamic display tube driver and the element T_{42} operates as a load of the element T_{41} .

EXAMPLE 12

The terminal S_3 is grounded and the terminal L_3 is connected to the source V_{DD} . The terminals A_3 and B_3 are used as receiving terminals of the input signals a_1 and a_2 , respectively, and the terminals D_3 , F_3 , H_3 and J_3 are used as receiving terminals for condition input signals j_1 , j_2 , j_3 and j_4 . Output signals a_{1j1} , a_{1j2} , a_{2j3} and a_{2j4} are obtained from the terminals C_3 , E_3 , G_3 and I_3 respectively. That is, as shown in Figure 7(C), the elements T_{41} to T_{46} provide a transistor gate added with switching elements for condition inputs. This is equivalently shown by a switching circuit as shown in Figure 7(D).

EXAMPLE 13

An exclusive "or" gate can be constituted by utilizing bidirectional property of MOS field effect transistor as follows. The terminal S_3 is grounded and the terminal L_3 is connected to the source V_{DD} . The terminals C_3 , D_3 , E_3 , F_3 , G_3 , H_3 , I_3 and J_3 are used as input terminals and the terminals A_3 and B_3 are used as output terminals. In this case, the terminals C_3 and F_3 , D_3 and E_3 , H_3 and I_3 , and G_3 and J_3 are used so as to be equivalent to each other. A gate circuit comprising the elements T_{41} to T_{46} is shown in Figure 7(E). If an input signal a_1 is supplied to the terminals C_3 and F_3 and an input signal b_1 is supplied to the terminals D_3 and E_3 , an output $a_1b_1 + a_1\bar{b}_1$ is obtained from the output terminal A_3 to which an external resistor R is connected.

As described in the above, this invention provides a single semiconductor integrated circuit arrangement having various possible uses and has advantageous features such as simplification of the manufacturing process, consolidation of manufacturing jigs and tools and manufacturing cost reduction resulting from mass production.

WHAT WE CLAIM IS:—

1. A semiconductor integrated circuit ar-



5 rangement having a substrate of one conductivity type, a plurality of MOS type field effect transistors each having semiconductor layers of the other conductivity type providing source and drain electrodes formed thereon and a metal layer which can be used as the control or gate electrode deposited on an insulating layer on a portion between the source and drain electrodes, a plurality of terminals connected to said electrodes on said substrate, and a semiconductor region having said one conductivity type but higher conductivity and usable as a substrate electrode is formed on the semiconductor substrate and a conductor to be attached to said semiconductor region is independently provided as a single external terminal without being commonly connected to any other portion of the circuit, the whole arrangement being such that a plurality of MOS field effect transistors having no D.C. coupling between the substrate and the source (or drain) electrode are formed.

2. A circuit arrangement in accordance with Claim 1, in which said circuit comprises at least five field effect transistors as structural elements, the control and third electrodes of the first and third structural elements being connected together, the second electrode of the first structural element being connected to the third electrode of the second structural element and their joint being connected to the control electrode of the fourth structural element and the third electrode of the fifth structural element, the second electrode of the third structural element being connected to the third electrode of the fourth structural element, and said external terminals being respectively connected to the control and second electrodes of the second and fifth structural elements, the second electrode of the fourth structural element, a joint of the second electrode of the first structural element, the third electrodes of the second and fourth structural elements and the control electrode of the fourth structural element, a joint of the control and third electrodes of the first and third structural elements, and a joint of the second electrode of the third structural element and the third electrode of the fourth structural element.

3. A circuit arrangement, in accordance with Claim 2, in which the control and third electrodes of the second and fifth structural elements are supplied with an input signal through the external terminals, the control and third electrodes of the first and third structural elements are supplied with a source voltage through the external terminal, the second electrode of the fourth structural element is grounded, and a joint of the second electrode of the first structural element, the third electrodes of the second and fifth structural elements and the control electrode of the fourth structural element and a joint of the second electrode of the third structural

element and the third electrode of the fourth structural element are led out through the external terminals as output terminals, to provide circuit functions of an exclusive logic gate and an inverter.

4. A circuit arrangement, in accordance with Claim 3, in which the circuit is constituted by two symmetrical circuits, the external terminals being used in the same way for each circuit, and a joint point of the second electrode of the first structural element, the third electrodes of the second and fifth structural elements and the control electrode of the fourth structural element in the circuit is connected through the external terminals to a joint in the other circuit corresponding to the first joint, to provide the circuit functions of an exclusive logic gate and an inverter.

5. A semiconductor integrated circuit arrangement, in accordance with Claim 4, in which the circuit is constituted of two symmetrical circuits, in one of which the control electrode of the second structural element and the second electrode of the fifth structural element are connected through the external terminals to be supplied with an input signal a_1 , the second electrode of the second structural element and the control electrode of the fifth structural element are connected through the external terminals to be supplied with an input signal a_2 , the structural elements for input in the other circuit are also connected in the same way to constitute two input signal supplying portions, one of them is supplied with a third input F_c through the external terminal, a joint of the second electrode of the first structural element, the third electrodes of the second and fifth structural elements, and the control electrode of the fourth structural element is connected to the other input signal supplying portion through the external terminal M_1 , and the third electrode of the structural element in the other circuit which is in a symmetric relation to the second structural element is used as an output terminal through the external terminal, to provide a circuit function of a three input (a_1 , a_2 and F_c) pure binary adder.

6. A semiconductor arrangement, in accordance with Claim 2, in which a joint of the second electrode of the first structural element, the third electrodes of the second and fifth structural elements and the control electrode of the fourth structural element, a joint of the second electrode of the third structural element and the third electrode of the fourth structural element and the control electrodes of the second and fifth structural elements are supplied with input signals, a joint of the control and third electrodes of the first and third structural elements and the second electrodes of the second and fifth structural elements are grounded, the external terminal connected to the second



electrode of the fourth structural element is used as an output terminal and a voltage is applied through said external terminal, to provide a circuit function of a logic gate.

5 7. A semiconductor arrangement, in accordance with Claim 1, in which said circuit constitution comprises a plurality of sets of circuits including at least three structural elements, the control electrode of the first structural element is connected to the third electrode of said element, the second electrode of said element is connected to the third electrode of the second structural element, the control electrode of the second structural element is connected to the third electrode of the third structural element, joints of the control and third electrodes of the first structural elements of the respective sets are connected in common, the second electrodes of the second structural elements of the respective sets are connected in common, and the control electrodes of the third structural elements of the respective sets are connected in common, and the external terminals are connected respectively to joints of the control and third electrodes of the first structural elements of the respective sets, joints of the second electrodes of the first structural elements of the respective sets, the second electrodes of the second structural elements and the control electrodes of the third structural elements of the respective sets.

8. A semiconductor arrangement, in accordance with Claim 7, in which a source voltage is applied through the external terminal to the control and third electrodes of the first structural element, the second electrode of the second structural element is grounded through the external terminal, an input signal is supplied to the second electrode of the third structural element, a synchronizing signal is supplied through the external terminal to the control electrode of the third structural element, a joint of the second electrode of the first structural element and the third electrode of the second structural element is connected through the external terminals to the second electrode of the third structural element in the next set having the same circuit configuration and another synchronizing signal having different phase is supplied through the external terminal to the control electrode of the third structural element of said set, to provide a circuit function of a synchronous dynamic memory.

9. A semiconductor arrangement, in accordance with Claim 7, in which two integrated blocks provided with at least two sets of circuit constitution including at least three structural elements are provided; in the first block, a voltage is applied through the external terminal to a joint of the control and third electrodes of the first structural element and the control electrode of the third structural element of two sets, the second

electrode of the second structural element is grounded, a joint of the second electrode of the first structural element and the third electrode of the second structural element of the first set is connected to the second electrode of the third structural element of the second set and a joint of the second electrode of the first structural element and the third electrode of the second structural element of the second set is connected to the second electrode of the third structural element of the first set; and, in the second block, a joint of the control and third electrodes of the first structural element and the second electrode of the second structural element of each set are grounded through the external terminals, a synchronizing signal is applied to the control electrode of the third structural element, joints of the second electrodes of the first structural elements and the third electrodes of the second structural elements of the first and second sets are connected to the second electrodes of the third structural elements of the respective corresponding sets in the first block and the respective second electrodes of the third structural elements of the respective sets are used as input signal supplying terminals through the external terminals, to provide a circuit function of a synchronous static memory.

10. A semiconductor arrangement, in accordance with Claim 7, in which a voltage is supplied through the external terminals to a joint of the control and third electrodes of the first structural element and the control electrode of the third structural element, the second electrode of the second structural element is grounded, the second electrode of the third structural element is used as an input terminal through the external terminal, and a joint of the second electrode of the first structural element and the third electrode of the second structural element is used as an output terminal through the external terminal, to provide a circuit function of an inverter.

11. A semiconductor arrangement, in accordance with Claim 7, in which a joint of the second electrode of the first structural element and the third electrode of the second structural element and the second electrode of the second structural element are grounded through the external terminals, a time selecting signal is supplied through the external terminal to the control electrode of the third structural element, an input driving pulse signal is supplied to the second electrode thereof and a joint of the second electrode of the first structural element and the third electrode of the second structural element is connected through the external terminals to the indication elements of a display tube, to provide a circuit function of a display tube driving circuit.

12. A semiconductor arrangement, in accordance with Claim 7, in which a voltage



is supplied through the external terminal to the control electrode of the third structural element, a joint of the second electrode of the first structural element and the third electrode of the second structural element and the second electrode of the third structural element are used as input terminals through the external terminals and the second electrode element is used as an output terminal, to provide a circuit function of a logic gate.

13. A semiconductor arrangement, in accordance with Claim 1, in which said circuit constitution comprises a plurality of sets of circuits including at least three structural elements, the control electrode of the first structural element in one set is connected to the third electrode of the third structural element, the second electrode of the first structural element is connected to the third electrode of the second structural element, the control and second electrodes of the second structural element and the control electrode of the third structural element are connected, a joint of the control and second electrodes of the second structural element and the control electrode of the third structural element of each set are connected in common and the third electrode of the first structural element of each of two sets out of a plurality of sets are connected in common, and the external terminals are connected respectively to a joint of the third electrodes of the first structural elements of the respective sets, a joint of the second electrode of the first structural element and the third electrode of the second structural element, a joint of the control and second electrodes of the second structural element and the control electrodes of the third structural element, and the second electrode of the third structural element.

14. A semiconductor arrangement, in accordance with Claim 13, in which a voltage is supplied through the external terminal to a joint of the control second electrodes of the second structural element and the control electrode of the third structural element, the third electrode of the first structural element is grounded, an input signal is supplied through the external terminal to the second electrode of the third structural element, and a joint of the second electrode of the first structural element and the third electrode of the second structural element is used as an output terminal through the external terminal, to provide a circuit function of an inverter.

15. A semiconductor arrangement, in accordance with Claim 13, in which the third electrode of the first structural element is grounded, a timing signal is supplied through the external terminal to a joint of the control

and second electrodes of the second structural element and the control electrode of the third structural element, an input signal is supplied to the second electrode of the third structural element, and a joint of the second electrode of the first structural element and the third electrode of the second structural element is connected as an output terminal through the external terminal to a display tube, to provide a circuit function of a display tube driver.

16. A semiconductor arrangement, in accordance with Claim 13, in which a joint of the control and second electrodes of the second structural element and the control electrode of the third structural element is connected to a source of voltage through the external terminal, an input signal is supplied through the external terminal to the third electrode of the first structural element, a condition input signal is supplied through the external terminal to the second electrode of the third structural element, and a joint of the second electrode of the first structural element and the third electrode of the second structural element is used as an output terminal through the external terminal, to provide a circuit function of a conditional logic gate.

17. A semiconductor arrangement, in accordance with Claim 13, in which at least two adjoining sets of symmetric circuit are provided, a voltage is supplied through the external terminal to the control and second electrodes of the second structural element and the control electrode of the third structural element, in each set, a joint of the second electrode of the first structural element and the third electrode of the second structural element is connected through the external terminals to the second electrode of the third structural element of the other set and is supplied with an input signal a_1 , the second electrode of the third structural element of the first set is connected through the external terminal to a joint of the second electrode of the first structural element and the third electrode of the second structural element of the other set and supplied with an input signal a_2 , and a common joint of the third electrode of the first structural element is used as an output terminal through the external terminal, to provide a circuit function of an exclusive logic gate.

18. A semiconductor integrated circuit substantially as herein before described with reference to Figure 2 of the accompanying drawings.

19. A semiconductor integrated circuit substantially as hereinbefore described with reference to Figure 4 of the accompanying drawings.



20. A semiconductor integrated circuit substantially as hereinbefore described with reference to Figure 6 of the accompanying drawings.

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