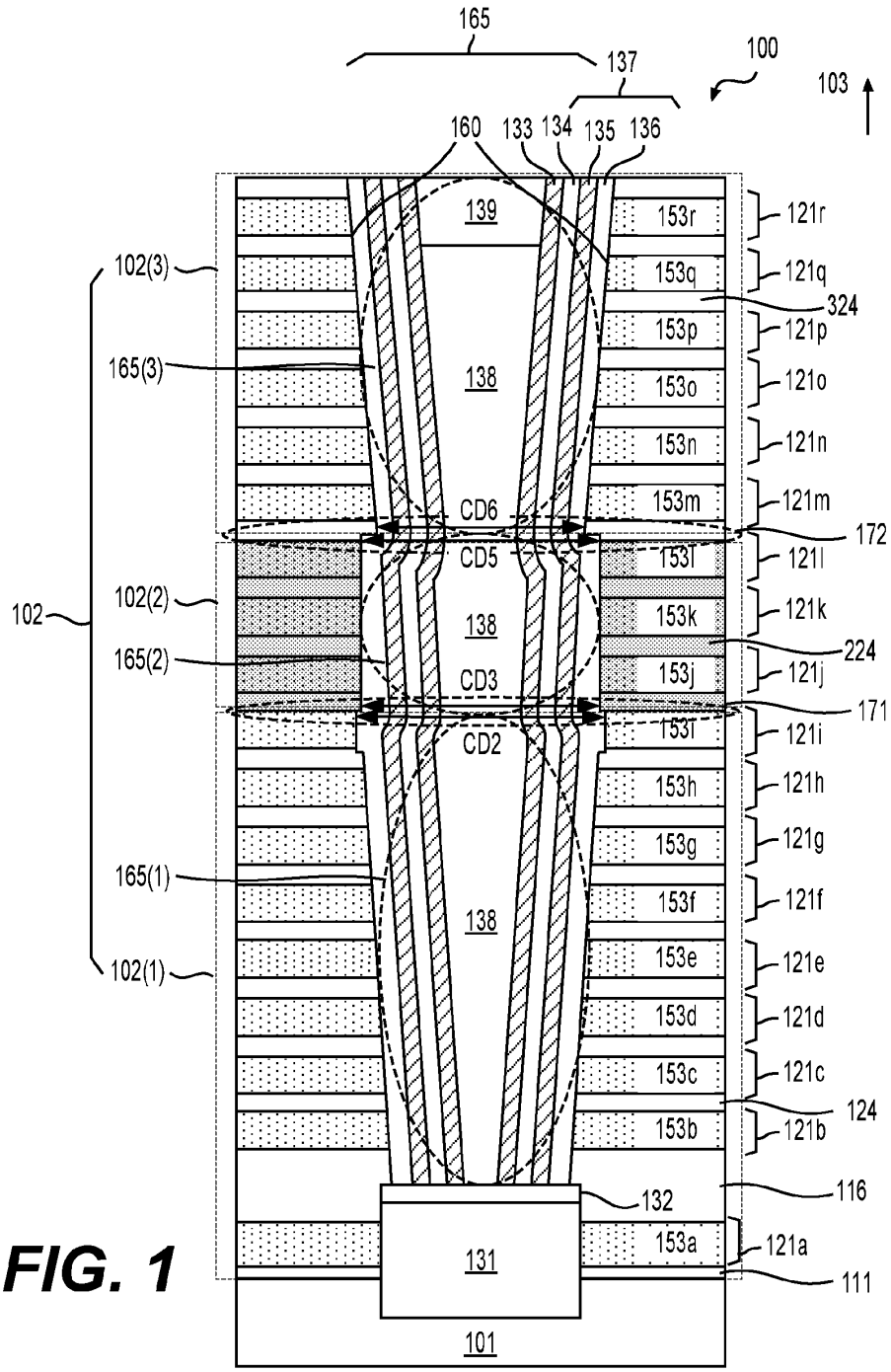

165
137
100
103
160
133
134
135
136
139
153r
121r
102(3)
153q
121q
324
153p
121p
165(3)
138
153o
121o
153n
121n
CD6
153m
121m
172
CD5
153l
121l
102
102(2)
138
153k
121k
224
165(2)
CD3
153j
121j
171
CD2
153i
121i
153h
121h
153g
121g
165(1)
138
153f
121f
153e
121e
102(1)
153d
121d
153c
121c
124
153b
121b
132
116
131
153a
121a
111
101

FIG. 1

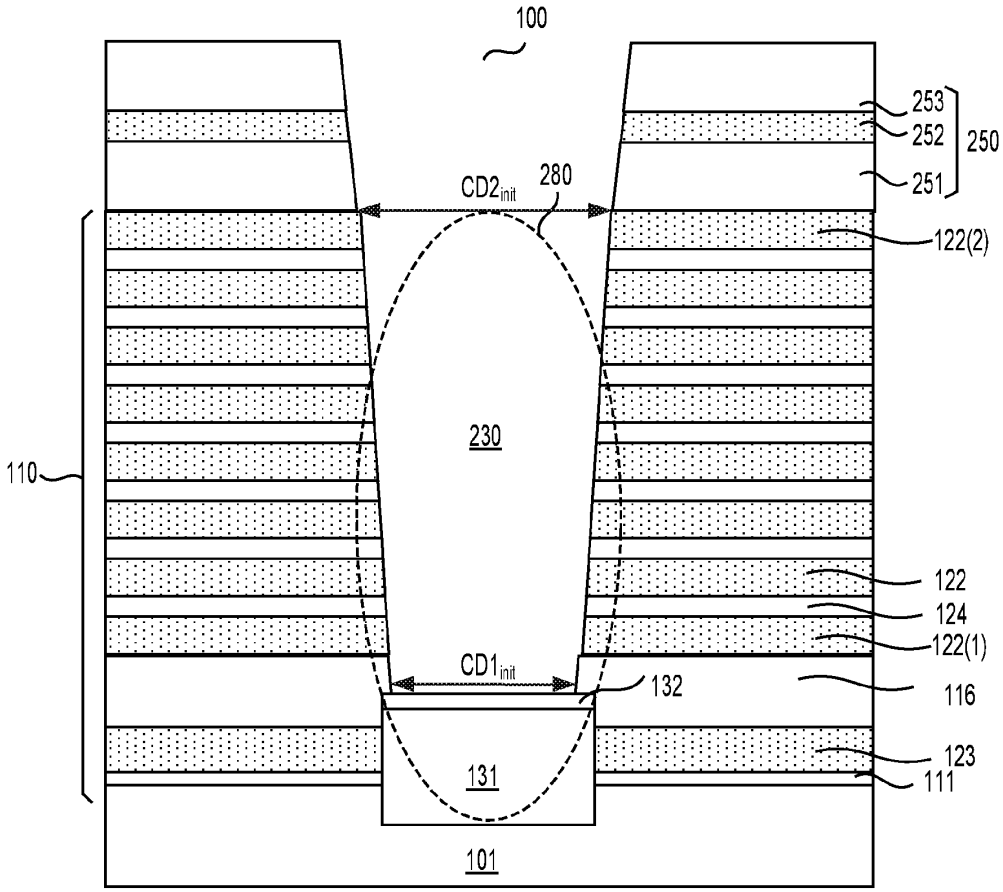

100
253
252
250
251
CD2init
280
122(2)
230
110
122
124
122(1)
CD1init
132
116
123
131
111
101

FIG. 2

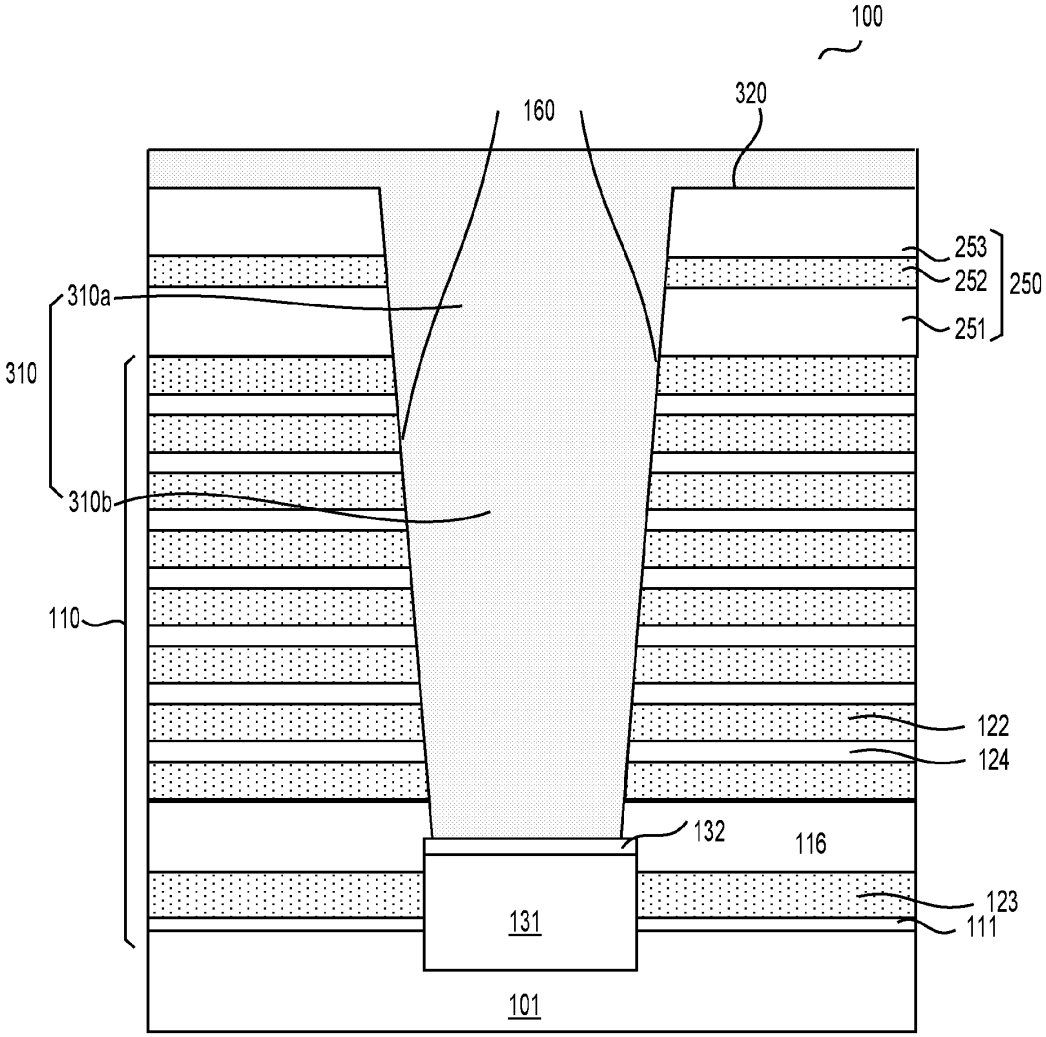

100
160
320
253
252
250
251
310a
310
310b
110
122
124
132
116
123
131
111
101

FIG. 3

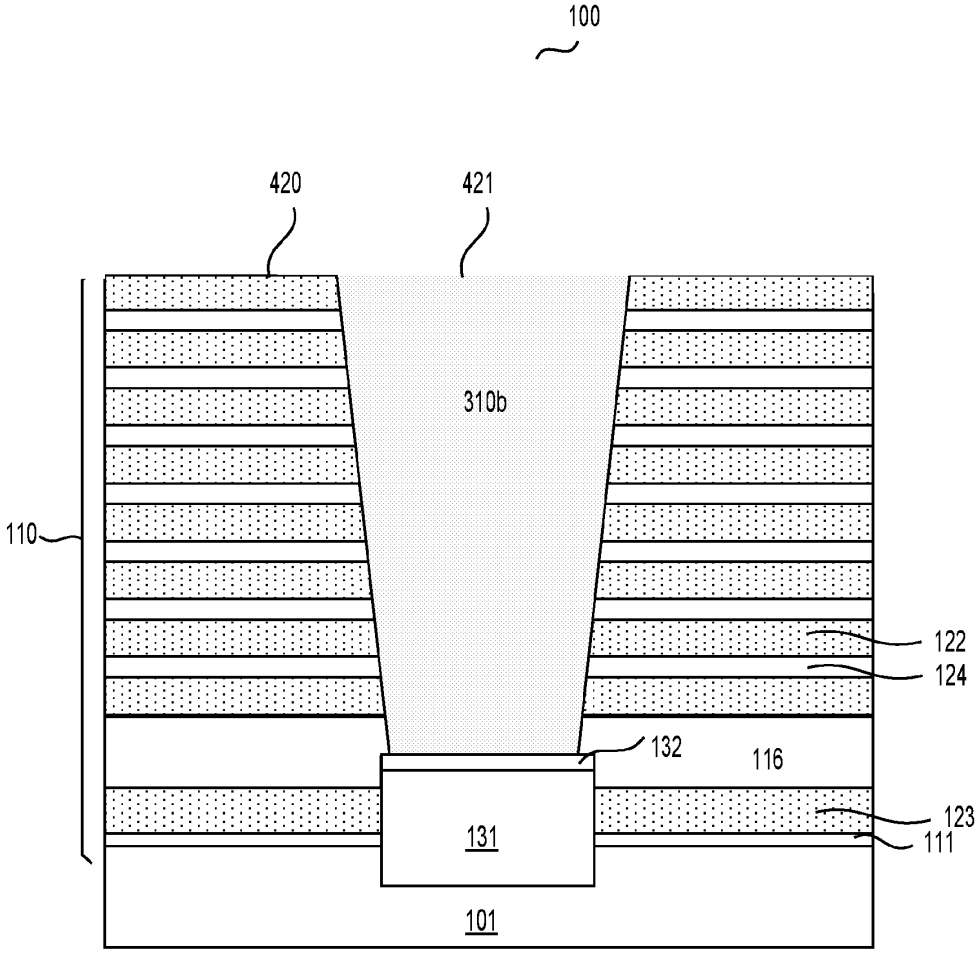


FIG. 4

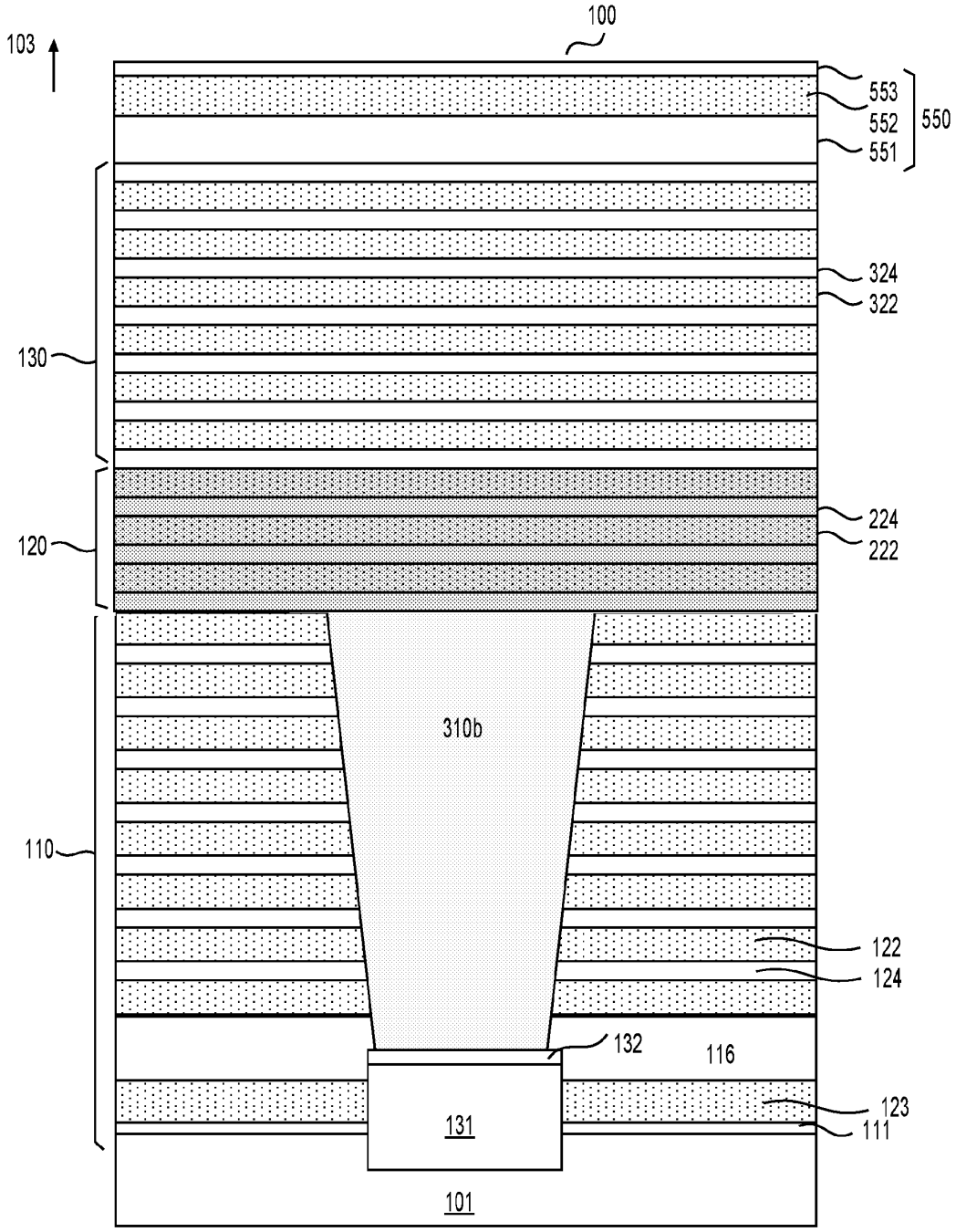

100
103
553
552
551
550
324
322
130
224
222
120
310b
110
122
124
132
116
131
123
111
101

FIG. 5

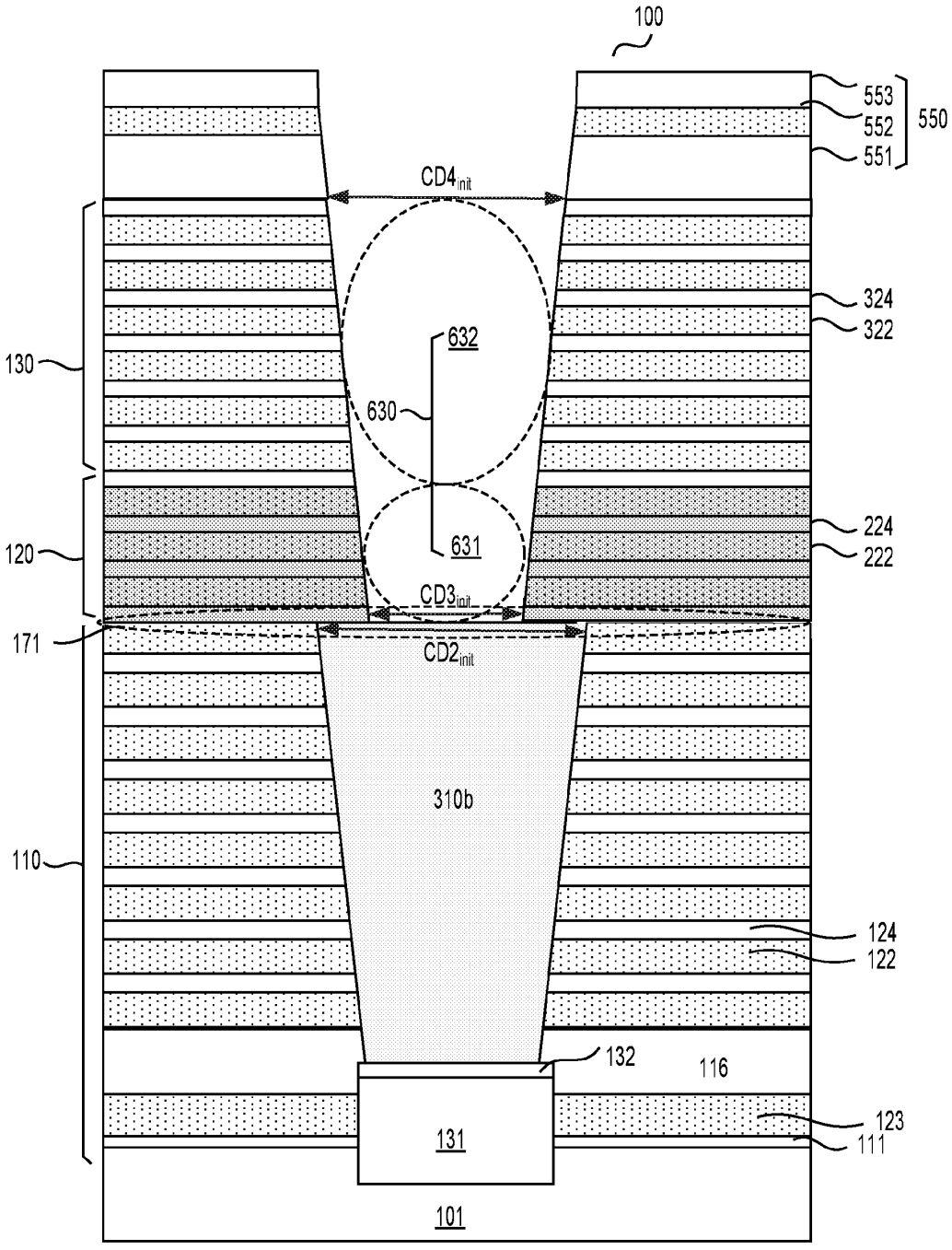

100
553
552
551
550
CD4init
324
322
632
130
630
631
224
222
120
CD3init
171
CD2init
310b
110
124
122
132
116
131
123
111
101

FIG. 6

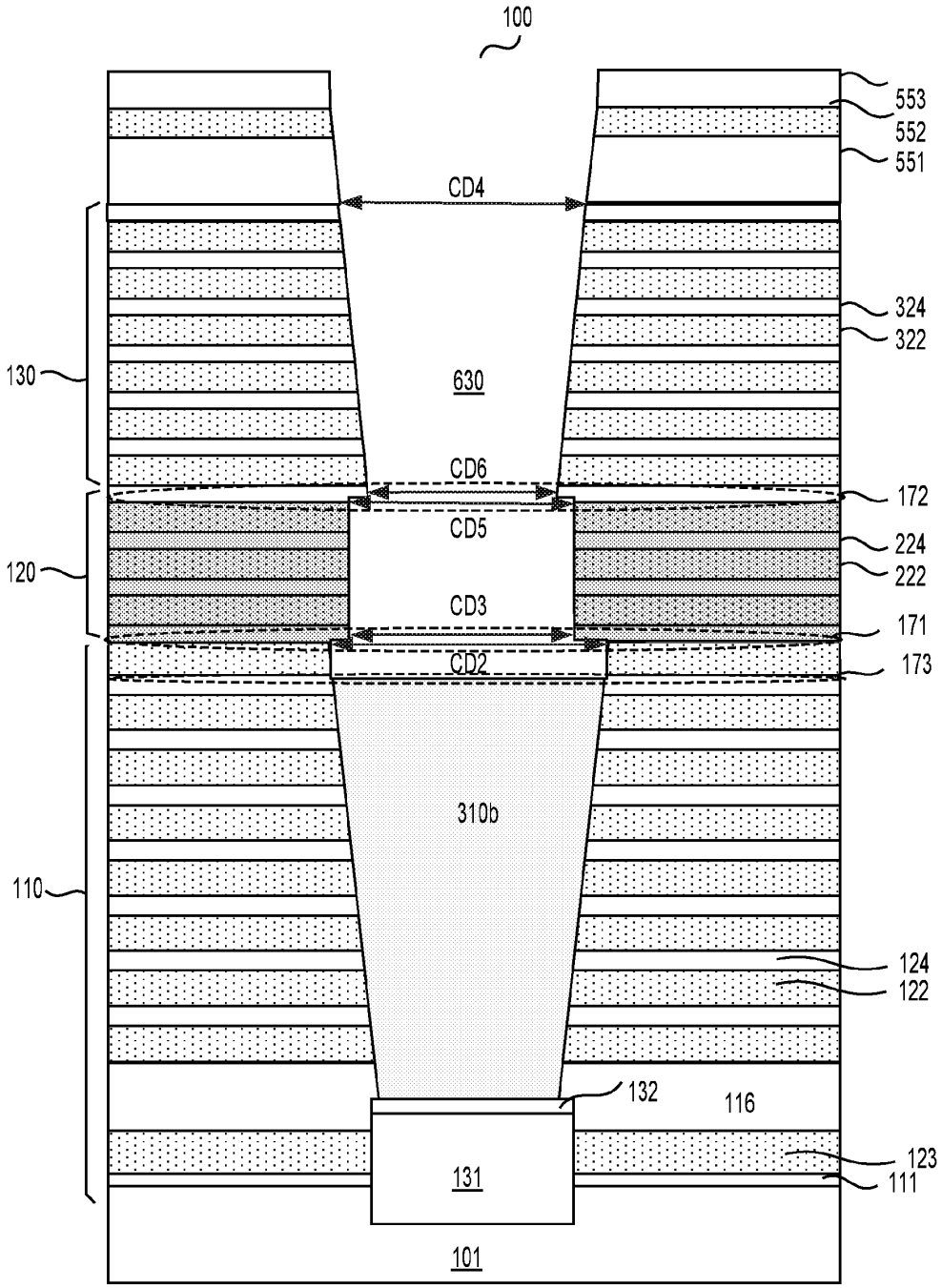

100
553
552
551
CD4
324
322
130
630
CD6
172
CD5
224
120
222
CD3
171
CD2
173
310b
110
124
122
132
116
123
131
111
101

FIG. 7

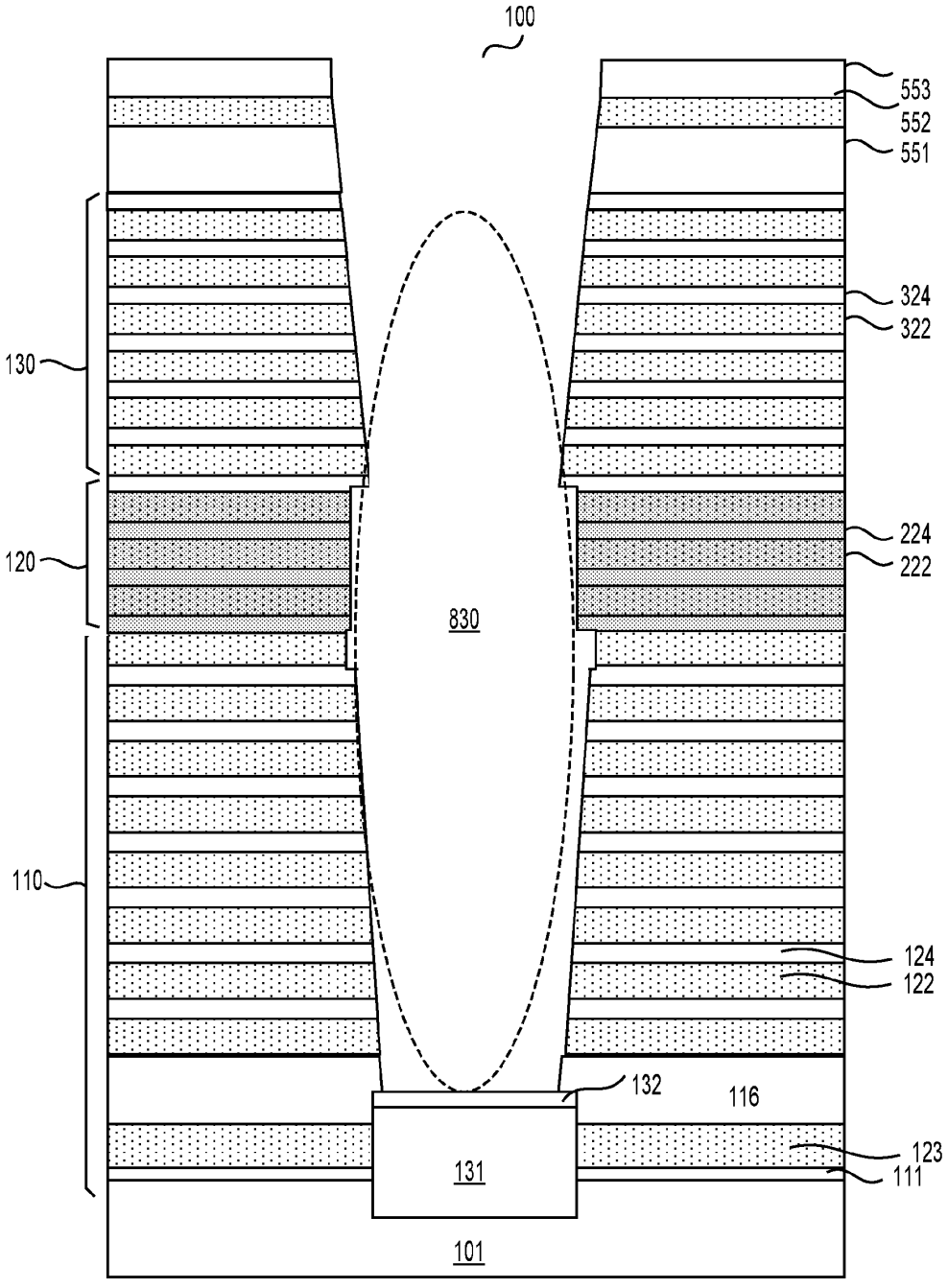

100
553
552
551
324
322
130
224
222
120
830
110
124
122
132
116
123
131
111
101

FIG. 8

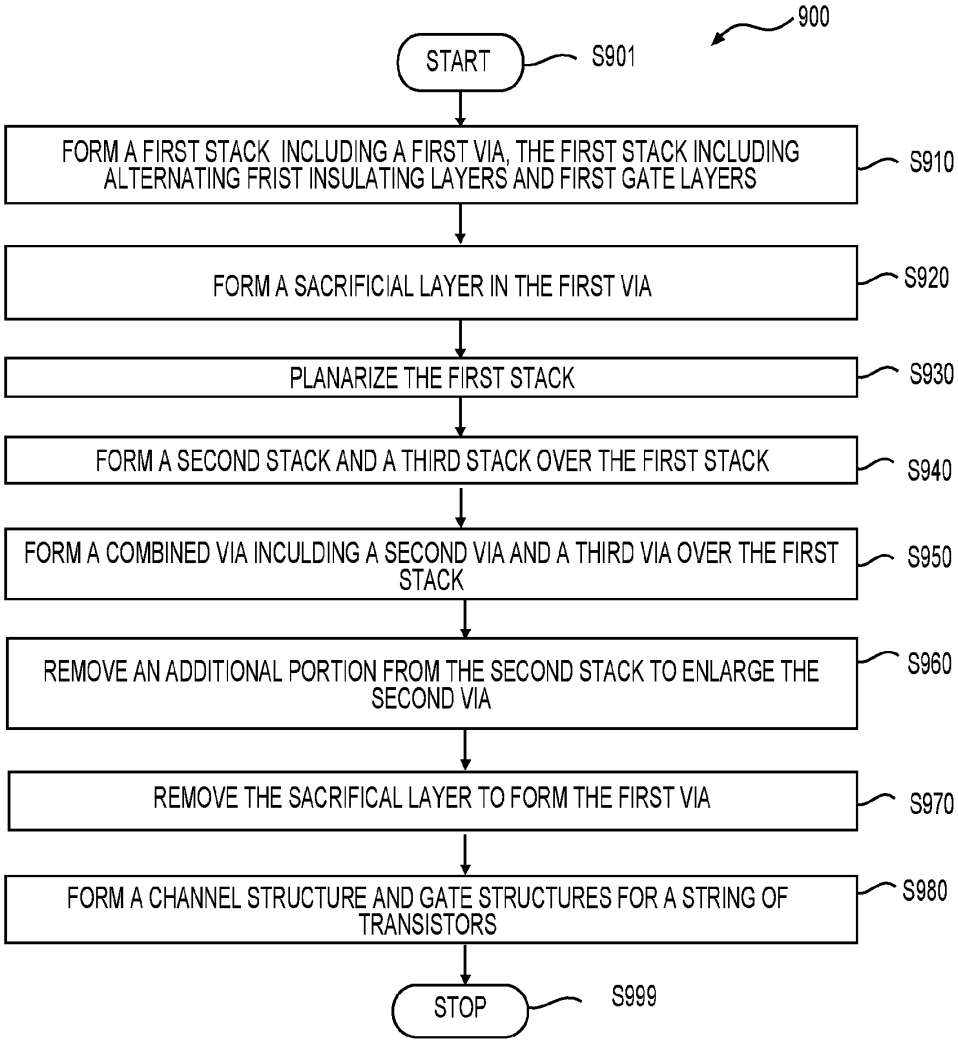

900
START
S901
FORM A FIRST STACK INCLUDING A FIRST VIA, THE FIRST STACK INCLUDING ALTERNATING FRIST INSULATING LAYERS AND FIRST GATE LAYERS
S910
FORM A SACRIFICIAL LAYER IN THE FIRST VIA
S920
PLANARIZE THE FIRST STACK
S930
FORM A SECOND STACK AND A THIRD STACK OVER THE FIRST STACK
S940
FORM A COMBINED VIA INCULDING A SECOND VIA AND A THIRD VIA OVER THE FIRST STACK
S950
REMOVE AN ADDITIONAL PORTION FROM THE SECOND STACK TO ENLARGE THE SECOND VIA
S960
REMOVE THE SACRIFICAL LAYER TO FORM THE FIRST VIA
S970
FORM A CHANNEL STRUCTURE AND GATE STRUCTURES FOR A STRING OF TRANSISTORS
S980
STOP
S999

FIG. 9