

ELECTRONIC CONTROL CIRCUIT FOR AUDIO-SIGNAL LEVEL
~~Circuit arrangement for the electronic level control of a sound signal~~

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The invention relates to a circuit arrangement for the electronic level control of a sound signal, comprising an amplifier circuit which is included in a sound signal path and whose gain can be controlled in dependence on a variable d.c. control voltage, and a voltage control stage for generating the variable d.c. control voltage, the generated variable d.c. control voltage being applied from the output of this voltage control stage to the amplifier circuit in order to control the gain of this amplifier circuit.

Such a circuit arrangement is known, for example from DE-AS 21 36 247. In this known circuit arrangement the amplifier circuit comprises a differential amplifier consisting of two bipolar transistors and the voltage control stage is formed by a variable resistance element connected to a direct voltage source and generating a d.c. control voltage which is applied to the base of a third bipolar transistor of the amplifier circuit, which third transistor forms a current source for the two transistors of the differential amplifier and, in dependence on the direct control voltage applied to its base, controls the current supplied by it to the two transistors of the differential amplifier and thus the signal coupling between these two transistors. In this known circuit arrangement the entire control range of the differential amplifier for controlling or adjusting the level of a sound signal is realised by means of comparatively small variations of the d.c. control voltage, but this results in a comparatively strong dependence of the control characteristic of the differential amplifier on tolerances of the components and voltage values and on thermal influences. Moreover, comparatively high voltages and comparatively large currents are required in order to obtain an optimum control characteristic of the differential amplifier in this known circuit arrangement. In the case that the known circuit arrangement is used for the level control or level adjustment of stereo signals, in which case, as is apparent from DE-AS 21 36 247, such a differential amplifier is provided in each of the two stereo channels, another problem is that owing to the afore-mentioned tolerance and temperature dependence, the same level control or adjustment action for both stereo channels throughout the control range can only be achieved with great difficulty.

It is the object of the invention to preclude the afore-mentioned problems and to construct a circuit arrangement of the type defined in the opening paragraph in such a manner that it has both a simple circuit configuration and a comparatively large control range and that the entire control range obtained by means of the amplifier circuit
5 is realised by means of a comparatively large variation of the d.c. control voltage and an optimum control characteristic of the amplifier circuit is obtained with comparatively small supply voltages and small currents. To this end, the invention is characterised in that the amplifier circuit is formed by a CMOS inverter having a signal input, a signal output and a supply voltage terminal, which signal input is preceded by a series resistor
10 via which the sound signal whose level is to be controlled is applied to the signal input of the CMOS inverter, on which signal output the level-controlled sound signal is available, and to which supply voltage terminal the variable d.c. control voltage generated by means of the voltage control stage is applied as supply voltage for the CMOS inverter, the CMOS inverter being operated, in dependence on the d.c. control
15 voltage applied to the supply voltage terminal, below the knee voltage in its starting region, in which the gain of the CMOS inverter decreases and, in addition, the dynamic output resistance of the CMOS inverter increases as the d.c. control voltage decreases.

By means of the circuit arrangement in accordance with the invention it is achieved that, in dependence on the variable d.c. control voltage applied as supply
20 voltage to the CMOS inverter used as amplifier circuit, both the gain of the CMOS inverter and the dynamic output resistance of the CMOS inverter can be varied, in such a manner that the gain decreases and the dynamic output impedance increases as the d.c. control voltage decreases. Together with a load impedance connected to the output of the CMOS inverter the dynamic output resistance of the CMOS inverter forms a
25 voltage divider for the level-controlled sound signal, which supplies a sound signal whose level decreases with increasing dynamic output impedance as a result of the changing voltage divider ratio. Moreover, since the gain decreases as the d.c. control voltage decreases the CMOS inverter also supplies a sound signal whose level decreases as the d.c. control voltage decreases. Thus, for controlling or adjusting the level of a
30 sound signal the circuit arrangement in accordance with the invention utilises two effects which augment one another, *i.e.* the variation of the gain of the CMOS inverter, which is directly proportional to the variation of the d.c. control voltage applied to the CMOS inverter, and the variation in the dynamic output resistance of the CMOS inverter,

which is inversely proportional to the variation of the d.c. control voltage applied to the CMOS inverter. Thus, a comparatively large control range is obtained for the electronic control or adjustment of the level of a sound signal with the aid of particularly simple means, *i.e.* by means of only a single CMOS inverter operated below the knee voltage in its starting region. Since a CMOS inverter is used it is possible to vary the d.c. control voltage over a comparatively wide range for the level control of a sound signal owing to the characteristics of this inverter in its starting region, which is advantageous for a minimal influence of tolerances and thermal effects on the control characteristic. Operating the CMOS inverter below the knee voltage in its starting region further has the advantage that the desired result is obtained with low d.c. control voltages, which are applied to the CMOS inverter as its supply voltage, and only very small currents occur. Another advantage of using a CMOS inverter operated below the knee voltage in its starting region is that a linear variation of the d.c. control voltage results in a logarithmic variation of the output signal of the CMOS inverter, *i.e.* of the level-controlled sound signal, as is required for a correct volume control adapted to the logarithmic auditory sensitivity of the ear. Moreover, due to the low tolerance and temperature dependence of such CMOS inverters, the same control characteristic for both stereo channels is obtained throughout the control range, *i.e.* a satisfactory tracking, if the circuit arrangement in accordance with the invention is used for the electronic level control or adjustment of stereo signals, in which case such a CMOS inverter is provided in each of the two stereo channels.

For a maximal control range it has proved to be particularly advantageous if a dynamic resistance, which is essentially formed by two series-connected diodes and whose resistance value is controllable, is coupled to the connection between the series resistor and the signal input of the CMOS inverter, the connection between the series resistor and the signal input of the CMOS inverter being connected to the connection between the two diodes of the dynamic resistance, which together with the series resistor forms a voltage divider for the sound signal whose level is to be controlled and which is applied to the CMOS inverter, and the variable d.c. control voltage generated by means of the voltage control stage is applied to a terminal of a diode of the dynamic resistance formed by the two diodes to control the resistance value of this dynamic resistance, the resistance value of the dynamic resistance formed by the two diodes decreasing as the d.c. control voltage decreases. Thus, it is achieved that, as the d.c.

control voltage decreases, the voltage divider ratio between the series resistor and the dynamic resistance whose resistance value can be controlled and which is formed by the two diodes, varies in such a manner that the level of the sound signal applied to the signal input of the CMOS inverter is reduced. This also provides an additional effect for the level control of a sound signal by very simple further means, *i.e.* in fact by means of two diodes, which effect amplifies the two afore-mentioned effects, *i.e.* the decrease in gain and the increase in dynamic output resistance of the CMOS inverter as the d.c. control voltage decreases, which further extends the control range for electronic level control or adjustment of a sound signal. Providing the two diodes has the additional advantage that it precludes overdriving of the CMOS inverter with decreasing d.c. control voltage, which is applied to the supply voltage terminal of the CMOS inverter as the supply voltage for this inverter. Providing two such series-connected diodes further has the advantage that the dynamic resistance remains substantially constant independently of the signal amplitude of the sound signal across the diodes.

Furthermore, it has proved to be advantageous if the connection between the series resistor and the signal input of the CMOS inverter and the connection between the two diodes of the dynamic resistance are connected *via* a capacitor which together with the series resistor forms a high-pass filter *via* which mid-range and treble signal components of a sound signal whose level is to be controlled are applied to the dynamic resistance to attenuate these signal components. Thus, it is achieved that at low volumes, which are set by reducing the d.c. control voltage to low voltage values, in which case the dynamic resistance has a low resistance value, mid-range and treble signal components are attenuated in relation to bass signal components, which corresponds to a relative boost of the bass signal components, which results in a good physiological loudness control as regards bass signal components.

In this connection it has proved to be particularly advantageous if the series resistor has its terminal which is remote from the signal input of the CMOS inverter connected to a terminal of a further high-pass filter whose other terminal is connected to at least one diode of the dynamic resistance, to the terminal of the diode which is remote from the connection between the two diodes, treble signal components of a sound signal whose level is to be controlled being additionally applied to the signal input of the CMOS inverter, with the series resistor being partly bypassed to boost these treble signal components, *via* the further high-pass filter, the diode of the dynamic

resistance connected to this further high-pass filter, and the capacitor arranged between the connection between the two diodes and the connection between the series resistor and the signal input of the CMOS inverter. Thus, it is achieved that at low volumes, which are set by reducing the d.c. control voltage to small voltage values, the dynamic
5 resistance 34 then having a low resistance value, the treble signal components are also boosted in addition to said boost of the bass signal components, which provides a particularly good physiological loudness control.

The invention will be described in more detail hereinafter with reference to an exemplary embodiment shown in the drawing, to which the invention is not
10 limited. The single Figure shows a circuit arrangement for electronic level control of a stereo sound signal, a circuit arrangement for electronic level control of a sound signal in accordance with the invention being included in each of the two stereo channels.

The Figure shows a circuit arrangement 1 for the electronic level control or adjustment of a stereo sound signal having a first input terminal 2 which receives,
15 for example, the left-channel sound signal whose level is to be controlled from a diagrammatically shown first preamplifier 3, and having a second input terminal 4 which receives, for example, the right-channel sound signal whose level is to be controlled from a diagrammatically shown second preamplifier 5. The circuit arrangement 1 further comprises a first output terminal 6, from which the level-
20 controlled left-channel sound signal is applied to, for example, a diagrammatically shown first output amplifier 7, and a second output terminal 8, from which the level-controlled right-hand sound signal is applied to, for example, a diagrammatically shown second output amplifier 9. Each of the two stereo channels 10 and 11 includes a circuit arrangement, 12 and 13 respectively, for the electronic level control or adjustment of
25 the relevant sound signal. These two circuit arrangements 12 and 13 have a completely identical circuit configuration, for which reason their parts bear the same reference symbols for the sake of simplicity.

The circuit arrangement 12 or 13 for the electronic level control of a sound signal comprises an amplifier circuit 14, which is included in the sound signal
30 path, *i.e.* in the stereo channel 10 or 11, and whose gain can be controlled in dependence on a variable d.c. control voltage. For generating the variable d.c. control voltage a voltage control stage 15 is provided whose output 16 supplies the generated

variable d.c. control voltage to the amplifier circuit 14 in order control the gain of this amplifier circuit.

The voltage control stage 15 has a potentiometer 17 coupled to a supply voltage terminal +V and to a reference potential, *i.e.* earth potential, *via* a resistor 18.

- 5 The wiper of the potentiometer 17 is connected to the output 16 of the voltage control stage 15. The resistor 18 ensures that the d.c. control voltage generated by means of the voltage control stage 15 and appearing on the output 16 cannot drop below a given minimum voltage value. The voltage control stage need not be constructed with a potentiometer as in the circuit arrangement shown. Such a voltage control stage may
- 10 also comprise, for example, a d.c. amplifier constructed as an integrator with a virtually infinite time constant, whose input voltage is variable between a given d.c. potential and a reference potential by means of, for example, two touch controls and which supplies at its output an output voltage corresponding to the set input voltage as the d.c. control voltage. Alternatively, such a voltage control stage may comprise a digital-to-analog
- 15 converter circuit which, in dependence on a digital signal applied to it by means of a remote control device, generates a direct voltage value, which it supplies as the d.c. control voltage.

- In the present case the amplifier circuit 14 is formed in a particularly simple and advantageous manner by a CMOS inverter, which is shown
- 20 diagrammatically in the Figure and which has a signal input 19, a signal output 20 and a supply voltage terminal 21. The CMOS inverter 14 comprises, in known manner, two complementary MOS field effect transistors 22 and 23, shown in the Figure, and protective resistors and protective diodes, not shown. Such a CMOS inverter can be realised, for example, by means of a CMOS inverter chip manufactured by the
- 25 Applicant and commercially available under the type designation PC74HCU04, which comprises six such CMOS inverters.

- The signal output 20 and the signal input 19 of the CMOS inverter 14 are connected to one another *via* a feedback resistor 24, which determines the operating point of the CMOS inverter 14. Together with the feedback resistor 24, a series resistor
- 30 25 preceding the signal input 19 determines the gain of the CMOS inverter 14. The series resistor 25 is connected to the respective input terminal 2 or 4 *via* a capacitor 26 for d.c. isolation. The sound signal whose level is to be controlled is applied to the signal input 19 of the CMOS inverter 14 *via* the series resistor 25. The level-controlled

sound signal is available on the signal output 20 of the CMOS inverter 14. The signal output 20 is connected to a load resistor 28 via a capacitor 27 for d.c. isolation. The voltage drop across the load resistor 28 is applied to the output amplifier 7 or 9 via the respective output terminal 6 or 8.

- 5 The supply voltage terminal 21 of the CMOS inverter 14 receives the variable d.c. control voltage generated by means of the voltage control stage 15 and appearing at its output 16 as the supply voltage for the CMOS inverter 14 via an electrically conductive connection 29. In dependence on the d.c. control voltage applied to the supply voltage terminal 21 the CMOS inverter 14 is operated below the knee
10 voltage in its starting region, in which the gain of the CMOS inverter 14 decreases and, in addition, the dynamic output resistance of the CMOS inverter 14 increases as the d.c. control voltage decreases.

- For the above case, in which the CMOS inverter 14 is implemented with the aid of the CMOS inverter chip PC74HCU04, the following is to be noted with
15 respect to the choice of the value of the supply voltage for this CMOS inverter. The PC74HCU04 chip is intended to be powered with a customary supply voltage of between 2 and 6 V. With such a voltage supply each of the CMOS inverters in this chip is operated in its pinch-off region above the knee voltage. To operate such a CMOS inverter in its starting region below the knee voltage as is required in the present circuit
20 arrangement, the applied supply voltage, which is formed by the d.c. control voltage generated by means of the voltage control stage 15, is selected to be correspondingly lower. In practice, it has then proved to be effective if the maximum d.c. control voltage is approximately 1.7 V. To adjust the level of a sound signal the d.c. control voltage is varied between this value of 1.7 V and a value of approximately 0.8 V with
25 the aid of the potentiometer 17. The resistor 18 ensures that the d.c. control voltage cannot drop below 0.8 V. The use of the resistor 18 thus ensures that the CMOS inverter 14 is receives a given minimum supply voltage, which guarantees that the CMOS inverter 14 operates correctly as an amplifier. If the supply voltage for the CMOS inverter 14, i.e. the d.c. control voltage applied to it, drops below said
30 minimum value of approximately 0.8 volts, normal operation of the CMOS inverter 14 will cease altogether, which is not permissible.

A capacitor 30 is connected to the connection 29 between the output 16 of the voltage control stage 15 and the supply voltage terminal 21 of the CMOS inverter

14. In the present case, where the d.c. control voltage is applied to the supply voltage terminals 21 of two CMOS inverters 14 in the two stereo channels 10 and 11 *via* the connection 29, this capacitor 30 serves to preclude any interaction between the two CMOS inverters 14 connected to one another with their supply voltage terminals 21 *via* the connection 29.

By operating the CMOS inverter 14, which is used as an amplifier circuit, below the knee voltage in its starting region, both the gain of the CMOS inverter 14 and the dynamic output resistance of the CMOS inverter 14 are varied in the present circuit arrangements 12 and 13 for the electronic level control or adjustment of a sound signal in dependence on the variable d.c. control voltage applied to the CMOS inverter 14 as the supply voltage, in such a manner that the gain decreases but the dynamic output resistance increases as the d.c. control voltage decreases. Together with the load resistor 28 connected to the signal output 20 the dynamic output resistance of the CMOS inverter 14 forms a voltage divider for the level-controlled sound signal. Owing to the varying voltage divider ratio this voltage divider supplies a sound signal whose level decreases when the d.c. control voltage decreases and, consequently, the dynamic output resistance increases. The CMOS inverter 14 also supplies a sound signal whose level decreases as the d.c. control voltage decreases, because the gain decreases as the d.c. control voltage decreases. Thus, to control the level of a sound signal two effects are involved which amplify one another, *i.e.* the variation of the gain of the CMOS inverter 14, which is directly proportional to the variation of the d.c. control voltage applied to the CMOS inverter, and the variation of the dynamic output resistance of the CMOS inverter 14, which is inversely proportional to the variation of the d.c. control voltage applied to the CMOS inverter. This provides a comparatively wide control range for the electronic control or adjustment of the level of a sound signal by means of only a single CMOS inverter operated below the knee voltage in its starting region. Owing to the characteristics of a CMOS inverter in its starting region the d.c. control voltage can be varied within a comparatively wide range to control the level of a sound signal, for example when the CMOS inverter chip PC74HCU04 is used, within a range of between approximately 1.7 V and approximately 0.8 V, *i.e.* within a range of approximately 0.9 V, which is advantageous for a small influence of tolerances and thermal effects on the control characteristic. Operating the CMOS inverter below the knee voltage in its starting region further has the advantage that the desired result can

be obtained with low d.c. control voltages applied to the CMOS inverter as supply voltages, and that only very small currents occur. If the CMOS inverter chip PC74HCU04 is used the d.c. control voltage is below approximately 1.7 V and currents of the order of magnitude of only a few up to 100 μ A occur. A further advantage of using a CMOS inverter operated below the knee voltage in its starting region is that a linear variation of the d.c. control voltage results in a logarithmic variation of the output signal of the CMOS inverter, *i.e.* of the level-controlled sound signal, as is desired for a correct loudness control adapted to the logarithmic auditory sensitivity of the ear. Furthermore, as a result of the low tolerance and temperature dependence of such CMOS inverters, the same control characteristic for both stereo channels over the entire control range, *i.e.* a satisfactory tracking, is obtained with the present circuit arrangement for level control or adjustment of a stereo sound signal, which includes such a CMOS inverter in each of the two stereo channels.

A dynamic resistance 34, which is essentially formed by two series-connected diodes 32 and 33 and whose resistance value can be controlled, is connected to the connection 31 between the series resistor 25 and the signal input 19 of the CMOS inverter 14 in the circuit arrangement 12 or 13. In this arrangement the connection 31 between the series resistor 25 and the signal input 19 of the CMOS inverter is connected to the connection 35 between the two diodes 32 and 33 of the dynamic resistance 34. Together with the series resistor 25 the dynamic resistance 34 formed by the two diodes 32 and 33 constitutes a voltage divider for the sound signal whose level is to be controlled and which is applied to the CMOS inverter 14. The diode 32 has its anode connected to the supply voltage terminal +V *via* a series resistor 36 and the other diode 33 has its cathode connected to the output 16 of the voltage control stage 15 *via* the connection 29 by means of a further series resistor 37. In this manner the variable d.c. control voltage generated by means of the voltage control stage 15 is applied, *via* the series resistor 37, to the dynamic resistance 34 formed by the two diodes 32 and 33, to control the resistance value of the dynamic resistance 34 at the cathode of the diode 33, the resistance value of the dynamic resistance 34 decreasing as the d.c. control voltage decreases. Thus, the voltage divider ratio between the series resistor 25 and the controllable dynamic resistance 34 formed by the two diodes 32 and 33, is varied when the d.c. control voltage decreases, thereby reducing the level of the sound signal applied to the signal input 19 of the CMOS inverter 14. Thus, the dynamic

resistance 34 provides an additional effect for controlling the level of a sound signal, which effect amplifies the two afore-mentioned effects, *i.e.* the decrease in gain and the increase in dynamic output resistance of the CMOS inverter 14 when the d.c. control voltage decreases, which provides a further extension of the control range of the

5 electronic control or adjustment of the level of a sound signal. In addition, the use of the dynamic resistance 34 precludes overdriving of the CMOS inverter 14 when the d.c. control voltage, which is applied to the supply voltage terminal of the CMOS inverter as its supply voltage. Using two such series-connected diodes as a dynamic resistance has the advantage that the dynamic resistance remains substantially constant, independently

10 of the signal amplitude of the sound signal across the diodes.

The connection 31 between the series resistor 25 and the signal input 19 of the CMOS inverter 14 and the connection 35 between the two diodes 32 and 33 of the dynamic resistance 34 are interconnected *via* a capacitor 38. Together with the series resistor 25 the capacitor 38 forms a high-pass filter 39 *via* which mid-range and

15 treble components of a sound signal whose level is to be controlled are applied to the dynamic resistance 34 to attenuate these signal components. Here, the cut-off frequency selected for this high-pass filter 39 is approximately 300 Hz. At low volumes, which occur when the d.c. control voltage at the output 16 of the voltage control stage 15 is set to low voltage values, the dynamic resistance 34 then having a low resistance value,

20 the mid-range and treble components by-passed *via* the high-pass filter 39 are drained, *via* the dynamic resistance 34 as a result of its low value, to the supply voltage terminal +V *via* the series resistor 36 and to earth *via* the series resistor 37 and the capacitor 30, which results in the mid-range and treble components being attenuated in comparison with the bass components, which are not by-passed. This corresponds to a

25 boost of the bass components relative to the mid-range and treble components at low volumes. At high volumes, which occur when the d.c. control voltage at the output 16 of the voltage control stage 15 is set to high voltage values, the dynamic resistance 34 then having a high resistance value, virtually no mid-range and treble components are drained *via* the dynamic resistance 34 because of its high resistance value, so that for

30 high volumes the bass components are not boosted relative to the mid-range and treble components. This provides a satisfactory physiological loudness control as regards bass components.

Moreover, the terminal of the series resistor 25 which is remote from the signal input 19 of the CMOS inverter 14, which is connected to the isolating capacitor 26, is connected to a terminal of a further high-pass filter 40, whose other terminal is connected to the cathode of the diode 33 of the dynamic resistance 34. The further high-pass filter 40 comprises a capacitor 41 connected in series with a resistor 42. The cut-off frequency selected for this further high-pass filter 40 is approximately 3 kHz. Treble components of a sound signal whose level is to be controlled are additionally applied to the signal input 19 of the CMOS inverter 14, to boost these treble components, *via* the further high-pass filter 40 and the diode 33 of the dynamic resistance 34, which diode is connected to this further filter, and the capacitor 38 arranged between the connection 35, which connects the two diodes 32 and 33, and the connection 31, which connects the series resistor 25 and the signal input 19 of the CMOS inverter 14. At low volumes, which occur when the d.c. control voltage at the output 16 of the voltage control stage 15 is set to low voltage values, the dynamic resistance 34 then having a low resistance value, treble components are additionally applied to the signal input 19 *via* the high-pass filter 40, the diode 33, which then has a low resistance value, and the capacitor 38, as a result of which these treble components are boosted at low volumes. At high volumes, which occur when the d.c. control voltage at the output 16 of the voltage control stage 15 is set to high voltage values, the dynamic resistance 34 then having a high resistance value, hardly any additional treble components are applied to the signal input 19 of the CMOS inverter 14 owing to the high resistance value of the diode 33, so that the treble components are not boosted at high volumes. Thus, at low volumes the treble components of a sound signal whose level is to be controlled, are also boosted in addition to said boost of the bass components, which yields a particularly good physiological loudness control. It is to be noted that the further high-pass filter 40 may alternatively be connected to the anode of the other diode 32 of the dynamic resistance 34, yielding the same advantageous effect. The further high-pass filter 40 may also be connected to the both diodes 32 and 33 of the dynamic resistance 34 *via* one further resistor each, to the connections of the diodes 32 and 33 which are remote from the connection 35 between these two diodes, which also yields the same advantageous effect.

Claims:

1. A circuit arrangement for the electronic level control of a sound signal, comprising an amplifier circuit (14) which is included in a sound signal path and whose gain can be controlled in dependence on a variable d.c. control voltage, and a voltage control stage (15) for generating the variable d.c. control voltage, the generated variable
5 d.c. control voltage being applied from the output (16) of this voltage control stage to the amplifier circuit (14) in order to control the gain of this amplifier circuit, characterised in that the amplifier circuit (14) is formed by a CMOS inverter (14) having a signal input (19), a signal output (20) and a supply voltage terminal (21), which signal input (19) is preceded by a series resistor (25) *via* which the sound signal
10 whose level is to be controlled is applied to the signal input (19) of the CMOS inverter (14), on which signal output (20) the level-controlled sound signal is available, and to which supply voltage terminal (21) the variable d.c. control voltage generated by means of the voltage control stage (15) is applied as supply voltage for the CMOS inverter (14), the CMOS inverter (14) being operated, in dependence on the d.c. control voltage
15 applied to the supply voltage terminal (21), below the knee voltage in its starting region, in which the gain of the CMOS inverter (14) decreases and, in addition, the dynamic output resistance of the CMOS inverter (14) increases as the d.c. control voltage decreases.
2. A circuit arrangement as claimed in Claim 1, characterised in that a
20 dynamic resistance, which is essentially formed by two series-connected diodes (32, 33) and whose resistance value is controllable, is coupled to the connection between the series resistor (25) and the signal input (19) of the CMOS inverter (14), the connection between the series resistor (25) and the signal input (19) of the CMOS inverter (14) being connected to the connection (35) between the two diodes (32, 33) of the dynamic
25 resistance (34), which together with the series resistor (25) forms a voltage divider for the sound signal whose level is to be controlled and which is applied to the CMOS inverter (14), and in that the variable d.c. control voltage generated by means of the voltage control stage (15) is applied to a terminal of a diode (33) of the dynamic



resistance (34) formed by the two diodes (32, 33) to control the resistance value of this dynamic resistance, the resistance value of the dynamic resistance (34) formed by the two diodes (32, 33) decreasing as the d.c. control voltage decreases.

3. A circuit arrangement as claimed in Claim 2, characterised in that the
5 connection between the series resistor (25) and the signal input (19) of the CMOS inverter (14) and the connection (35) between the two diodes (32, 33) of the dynamic resistance (34) are connected *via* a capacitor (38) which together with the series resistor (25) forms a high-pass filter *via* which mid-range and treble signal components of a sound signal whose level is to be controlled are applied to the dynamic resistance (34)
10 to attenuate these signal components.

4. A circuit arrangement as claimed in Claim 3, characterised in that the series resistor (25) has its terminal which is remote from the signal input (19) of the CMOS inverter connected to a terminal of a further high-pass filter (40) whose other terminal is connected to at least one diode (33) of the dynamic resistance (34), to the
15 terminal of the diode (33) which is remote from the connection (35) between the two diodes (32, 33), treble signal components of a sound signal whose level is to be controlled being additionally applied to the signal input (19) of the CMOS inverter (14), with the series resistor (25) being partly bypassed to boost these treble signal components, *via* the further high-pass filter (40), the diode (33) of the dynamic
20 resistance (34) connected to this further high-pass filter, and the capacitor (38) arranged between the connection (35) between the two diodes (32, 33) and the connection between the series resistor (25) and the signal input (19) of the CMOS inverter (14).