CLAIMS

What is claimed is:

1. An etch apparatus, comprising

a chamber;

a plasma source within or coupled to the chamber; and

an electrostatic chuck within the chamber, the electrostatic chuck comprising:

a conductive pedestal having a plurality of notches at a circumferential edge thereof;

a plurality of lift pins corresponding to ones of the plurality of notches; and

edge insulator ring laterally around the conductive pedestal, the edge insulator ring having a plurality of inner protrusions corresponding to ones of the plurality of notches, each of the plurality of inner protrusions having an opening there through to accommodate corresponding ones of the plurality of lift pins.

2. The etch apparatus of claim 1, wherein the conductive pedestal and surfaces of the plurality of notches are coated with a ceramic material.

3. The etch apparatus of claim 2, wherein the ceramic material comprises alumina.

4. The etch apparatus of claim 1, the electrostatic chuck further comprising:

a bottom insulator ring beneath the conductive pedestal, the bottom insulator ring having a plurality of openings corresponding to ones of the plurality of lift pins.

5. The etch apparatus of claim 1, wherein the plurality of lift pins is located outside of a perimeter of a processing region of the conductive pedestal, the plurality of lift pins arranged for contacting a substrate carrier.

6. The etch apparatus of claim 1, the electrostatic chuck further comprising:

a shadow ring positioned over the plurality of lift pins.

7. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

forming a mask above the semiconductor wafer, the mask comprising a layer covering and protecting the integrated circuits, and the semiconductor wafer supported by a substrate carrier;

patterning the mask with a laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits; and

etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits while the semiconductor wafer is supported by the substrate carrier, and the substrate carrier is supported by an electrostatic chuck comprising a conductive pedestal having a plurality of notches at a circumferential edge thereof; and

an edge insulator ring laterally around the conductive pedestal, the edge insulator ring having a plurality of inner protrusions corresponding to ones of the plurality of notches, each of the plurality of inner protrusions having an opening there through to accommodate corresponding ones of a plurality of lift pins.

8. The method of claim 7, wherein the conductive pedestal and surfaces of the plurality of notches are coated with a ceramic material, and wherein the ceramic material prevents current from leaking from the electrostatic chuck during the etching.

9. The method of claim 7, further comprising:

subsequent to the etching, removing the substrate carrier from the conductive pedestal using the plurality of lift pins corresponding to ones of the plurality of notches of the conductive pedestal.

10. A system for dicing a semiconductor wafer comprising a plurality of integrated circuits, the system comprising:

a factory interface;

a laser scribe apparatus coupled with the factory interface and comprising a laser; and

an etch apparatus coupled with the factory interface, the etch apparatus comprising a chamber, a plasma source within or coupled to the chamber, and an electrostatic chuck within the chamber, the electrostatic chuck comprising a conductive pedestal having a plurality of notches at a circumferential edge thereof, and a plurality of lift pins corresponding to ones of the plurality of notches,

wherein the electrostatic chuck of the etch apparatus further comprises an edge insulator ring laterally around the conductive pedestal, the edge insulator ring having a plurality of inner protrusions corresponding to ones of the plurality of notches, each of the plurality of inner protrusions having an opening there through to accommodate corresponding ones of the plurality of lift pins.

11. The system of claim 10, wherein the laser scribe apparatus is configured to perform laser ablation of streets between integrated circuits of a semiconductor wafer, and wherein the etch apparatus is configured to etch the semiconductor wafer to singulate the integrated circuits subsequent to the laser ablation.

12. The system of claim 10, wherein the etch apparatus is housed on a cluster tool coupled with the factory interface, the cluster tool further comprising:

a deposition chamber configured to form a mask layer above the integrated circuits of the semiconductor wafer.

13. The system of claim 10, wherein the etch apparatus is housed on a cluster tool coupled with the factory interface, the cluster tool further comprising:

a wet/dry station configured to clean the semiconductor wafer subsequent to the laser ablation or the etching.

14. The system of claim 10, wherein the laser scribe apparatus comprises a femtosecond-based laser.

15. The system of claim 14, wherein the femtosecond-based laser has a wavelength of less than or equal to 530 nanometers with a laser pulse width of less than or equal to 400 femtoseconds.

16. The system of claim 10, wherein the conductive pedestal and surfaces of the plurality of notches of the electrostatic chuck of the etch apparatus are coated with a ceramic material.

17. The system of claim 10, wherein the electrostatic chuck of the etch apparatus further comprises a bottom insulator ring beneath the conductive pedestal, the bottom insulator ring having a plurality of openings corresponding to ones of the plurality of lift pins.

18. The system of claim 10, wherein the plurality of lift pins of the electrostatic chuck of the etch apparatus is located outside of a perimeter of a processing region of the conductive pedestal, the plurality of lift pins arranged for contacting a substrate carrier.