BALL GRID ARRAY CHIP PACKAGES HAVING IMPROVED TESTING AND STACKING CHARACTERISTICS

ABSTRACT OF THE DISCLOSURE

A stackable ball grid array (BGA) or fine ball grid array (FBGA) semiconductor package particularly suitable for board-on-chip or chip-on-board applications in which a low profile BGA or FBGA semiconductor package is needed. The present invention provides a semiconductor package which is capable of being burned in and tested in a more efficient and cost effective manner than prior known BGA or FBGA semiconductor packages. A high density, low profile memory module incorporating a plurality of the disclosed BGA or FBGA semiconductor packages in a stacked arrangement is further disclosed.

Exemplary BGA or FBGA semiconductor packages of the present invention generally comprise a substrate having a semiconductor device attached to a selected surface thereof. The semiconductor device has a plurality of bond pads respectively wire bonded to a plurality of bond pads located on the substrate. The substrate is preferably provided with a plurality of circuit traces leading from the substrate bond pads to a plurality of connective elements, such as solder ball contact pads and associated solder balls, arranged in a preselected ball grid array pattern and to a plurality of test pads arranged in a preselected pattern. Burn in and testing of the semiconductor chip may be performed by electrically contacting selected test pads by complementary arranged test probes in lieu of directly contacting and perhaps harming the connective elements. Upon burning in and testing of the semiconductor device, the test pads may be disassociated from the substrate to decrease the foot print of the semiconductor package. In accordance with the present invention the semiconductor device and the connective elements may optionally be provided on the same surface of the substrate to decrease the profile of the stackable BGA or FBGA chip package.

[Figure 5]