

WHAT IS CLAIMED IS:

- 1 1. A substrate comprising:
2 a support structure comprising:
3 a polycrystalline ceramic core;
4 a first adhesion layer coupled to the polycrystalline ceramic core;
5 a conductive layer coupled to the first adhesion layer;
6 a second adhesion layer coupled to the conductive layer; and
7 a barrier layer coupled to the second adhesion layer;
8 a silicon oxide layer coupled to the support structure;
9 a substantially single crystalline silicon layer coupled to the silicon oxide
10 layer;
11 an epitaxial III-V layer coupled to the substantially single crystalline silicon
12 layer.
- 1 2. The substrate of claim 1 wherein the polycrystalline ceramic core
2 comprises aluminum nitride.
- 1 3. The substrate of claim 2 wherein the epitaxial III-V layer comprises an
2 epitaxial gallium nitride layer.
- 1 4. The substrate of claim 3 wherein the epitaxial gallium nitride layer has
2 a thickness of about 5 μm or greater.
- 1 5. The substrate of claim 1 wherein the substantially single crystal silicon
2 layer comprises an exfoliated silicon layer about 0.5 μm in thickness.
- 1 6. The substrate of claim 1 wherein the substantially single crystal silicon
2 layer comprises an exfoliated silicon layer and an epitaxial silicon layer grown on the
3 exfoliated silicon layer, and the substantially single crystal silicon layer has a thickness of
4 about 0.5 μm .
- 1 7. The substrate of claim 2 wherein:
2 the first adhesion layer comprises a first tetraethyl orthosilicate (TEOS) layer
3 encapsulating the polycrystalline ceramic core;
4 the conductive layer comprises a polysilicon layer encapsulating the first
5 TEOS oxide layer;

6 the second adhesion layer comprises a second TEOS layer encapsulating the
7 polysilicon layer; and
8 the barrier layer comprises a silicon nitride layer encapsulating the second
9 TEOS layer.

1 8. The substrate of claim 7 wherein:
2 the first TEOS layer has a thickness of about 1000 Å;
3 the polysilicon layer has a thickness of about 3000 Å;
4 the second TEOS layer has a thickness of about 1000 Å; and
5 the silicon nitride layer has a thickness of about 4000 Å.

1 9. A method of manufacturing a substrate, the method comprising:
2 forming a support structure by:
3 providing a polycrystalline ceramic core;
4 encapsulating the polycrystalline ceramic core in a first adhesion shell;
5 encapsulating the first adhesion shell in a conductive shell;
6 encapsulating the conductive shell in a second adhesion shell; and
7 encapsulating the second adhesion shell in a barrier shell;
8 joining a bonding layer to the support structure;
9 joining a substantially single crystalline silicon layer to the bonding layer;
10 forming an epitaxial silicon layer by epitaxial growth on the substantially
11 single crystalline silicon layer; and
12 forming an epitaxial III-V layer by epitaxial growth on the epitaxial silicon
13 layer.

1 10. The method of claim 9 further comprising forming a plurality of vias
2 passing from the epitaxial III-V layer to the epitaxial silicon layer.

3 11. The method of claim 9 wherein the epitaxial III-V layer comprises
4 gallium nitride.

1 12. The method of claim 9 wherein:
2 the first adhesion shell comprises a tetraethyl orthosilicate (TEOS) shell;
3 the conductive shell comprises a polysilicon shell;
4 the second adhesion shell comprises a second TEOS shell;
5 the barrier material comprises a silicon nitride shell; and
6 the bonding layer comprise silicon oxide.

1 13. The method of claim 12 wherein:
2 the first TEOS shell comprises a single layer of TEOS;
3 the polysilicon layer comprises a single layer of polysilicon;
4 the second TEOS oxide shell comprises a single layer of TEOS; and
5 the silicon nitride shell comprises a single layer of silicon nitride.

1 14. An engineered substrate structure comprising:
2 a support structure comprising:
3 a polycrystalline ceramic core;
4 a first adhesion layer coupled to the polycrystalline ceramic core;
5 a conductive layer coupled to the first adhesion layer;
6 a second adhesion layer coupled to the conductive layer; and
7 a barrier shell coupled to the second adhesion layer;
8 a bonding layer coupled to the support structure;
9 a substantially single crystalline silicon layer coupled to the bonding layer;
10 and
11 an epitaxial single crystal silicon layer coupled to the substantially single
12 crystalline silicon layer.

1 15. The engineered substrate structure of claim 14 wherein:
2 the polycrystalline ceramic core comprises polycrystalline gallium nitride;
3 the first adhesion layer comprises tetraethyl orthosilicate (TEOS);
4 the conductive layer comprises polysilicon;
5 the second adhesion layer comprises TEOS;
6 the barrier shell comprises silicon nitride; and
7 the bonding layer comprise silicon oxide.

1 16. The engineered substrate structure of claim 14 further comprising an
2 epitaxial III-V layer coupled to the epitaxial single crystal silicon layer.

1 17. The engineered substrate structure of claim 16 further comprising a
2 plurality of vias passing from the epitaxial III-V layer to the epitaxial single crystal silicon
3 layer.

1 18. The engineered substrate structure of claim 14 further comprising one
2 or more buffer layers disposed between the substantially single crystalline silicon layer and
3 the epitaxial single crystal silicon layer.

1 19. The engineered substrate structure of claim 14 wherein the epitaxial
2 single crystal silicon layer is strained.

1 20. The engineered substrate structure of claim 14 wherein the epitaxial
2 single crystal silicon layer is characterized by a thickness in the range of 1 μm to 20 μm .

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1 21. A substrate comprising:
2 a polycrystalline ceramic core;
3 a first adhesion layer encapsulating the polycrystalline ceramic core;
4 a conductive layer encapsulating the first adhesion layer;
5 a second adhesion layer encapsulating the conductive layer;
6 a barrier layer encapsulating the second adhesion layer;
7 a bonding layer coupled to the barrier layer; and
8 a substantially single crystalline silicon layer coupled to the bonding lay

1 22. The substrate of claim 21 wherein the polycrystalline ceramic core
2 comprises polycrystalline aluminum nitride.

1 23. The substrate of claim 21 wherein the first adhesion layer comprises
2 tetraethyl orthosilicate (TEOS).

1 24. The substrate of claim 21 wherein the first adhesion layer has a
2 thickness of about 1000 Å.

1 25. The substrate of claim 21 wherein the conductive layer comprises
2 polysilicon.

1 26. The substrate of claim 21 wherein the conductive layer has a thickness
2 of about 3000 Å.

1 27. The substrate of claim 21 wherein the second adhesion layer comprises
2 tetraethyl orthosilicate (TEOS).

- 1 28. The substrate of claim 21 wherein the second adhesion layer has a
2 thickness of about 1000 Å.
- 1 29. The substrate of claim 21 wherein the barrier layer comprises silicon
2 nitride.
- 1 30. The substrate of claim 21 wherein the barrier layer has a thickness of
2 about 4000 Å.
- 1 31. The substrate of claim 21 wherein the substantially single crystalline
2 silicon layer comprises an exfoliated silicon layer.
- 1 32. The substrate of claim 21 wherein the substantially single crystalline
2 silicon layer has a thickness of about 0.5 μm.
- 1 33. A method of fabricating a substrate, the method comprising:
2 providing a polycrystalline ceramic core;
3 encapsulating the polycrystalline ceramic core in a first adhesion shell;
4 encapsulating the first adhesion shell in a conductive shell;
5 encapsulating the conductive shell in a second adhesion shell;
6 encapsulating the second adhesion shell in a barrier shell;
7 joining a bonding layer to the barrier shell; and
8 joining a single crystal silicon layer to the bonding layer.
- 1 34. The method of claim 33 wherein the polycrystalline ceramic core
2 comprises polycrystalline aluminum nitride.
- 1 35. The method of claim 33 wherein the first adhesion shell comprises
2 tetraethyl orthosilicate (TEOS).
- 1 36. The method of claim 33 wherein the conductive shell comprises
2 polysilicon.
- 1 37. The method of claim 33 wherein the second adhesion shell comprises
2 tetraethyl orthosilicate (TEOS).
- 1 38. The method of claim 33 wherein the barrier shell comprises silicon
2 nitride.

1 39. The method of claim 33 wherein joining the single crystalline silicon
2 layer comprises performing a layer transfer process from a silicon-on-insulator wafer.

1 40. The method of claim 39 further comprising smoothing the substantially
2 single crystalline silicon layer.