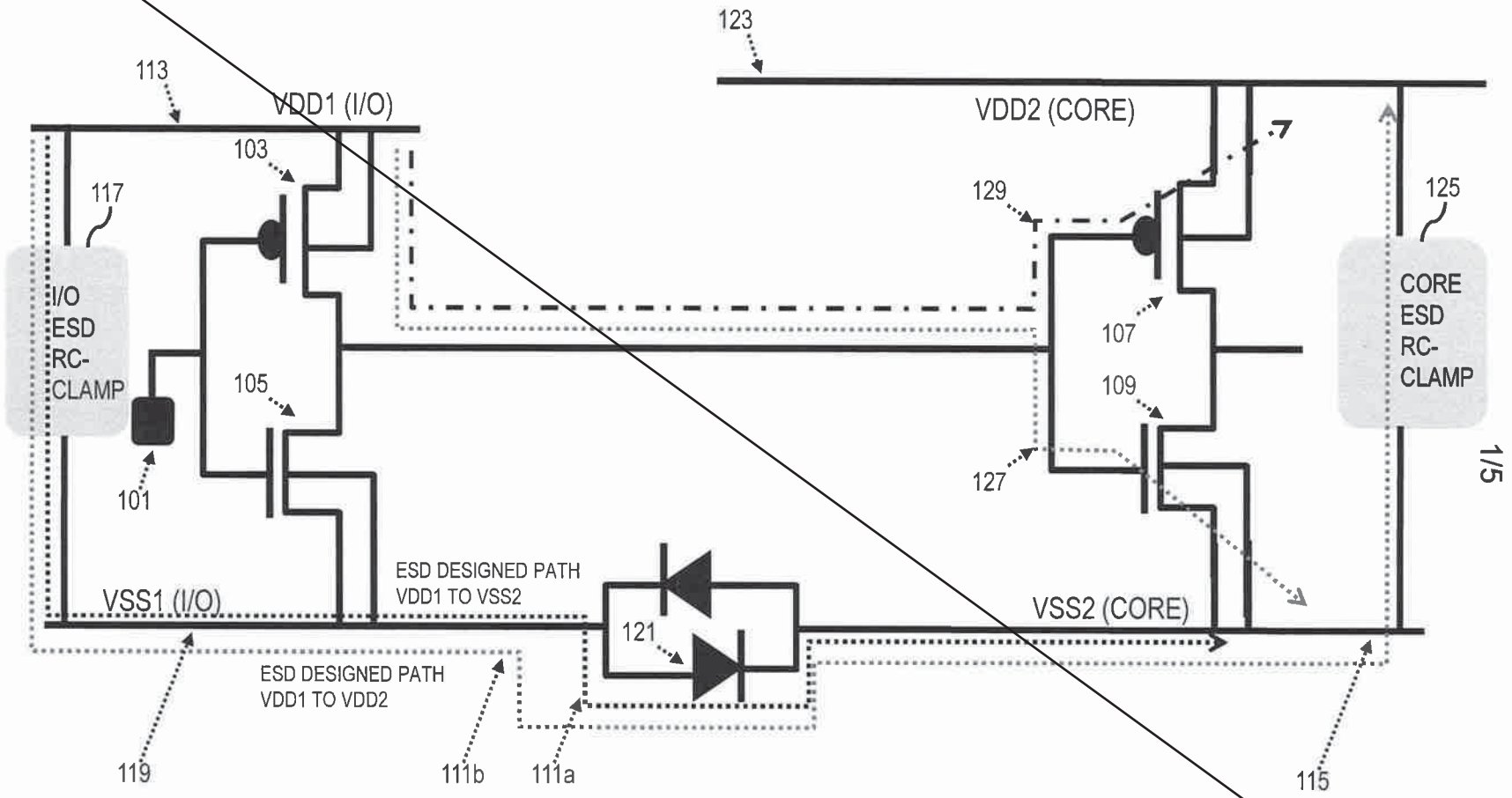
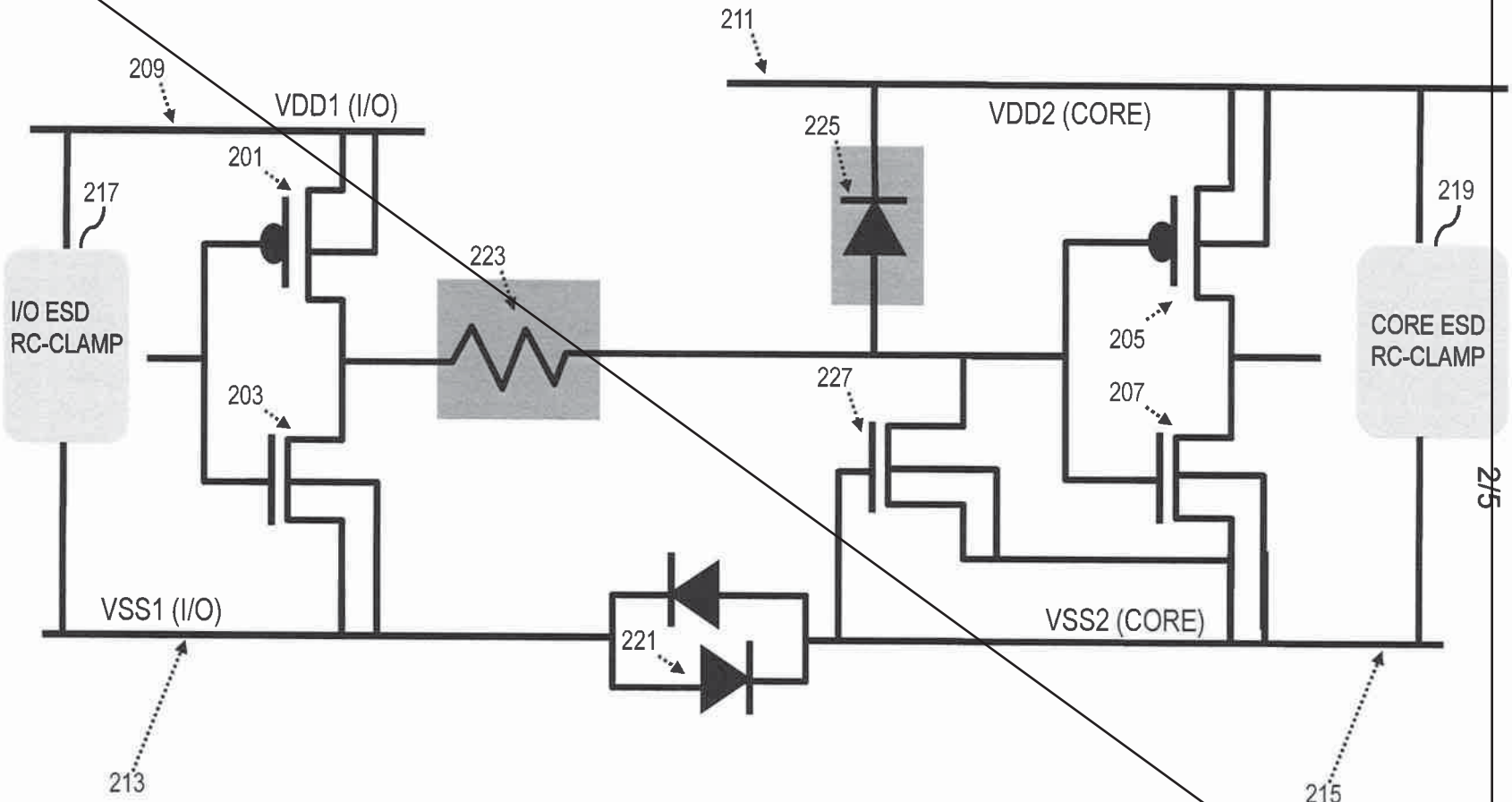
FIG. 1



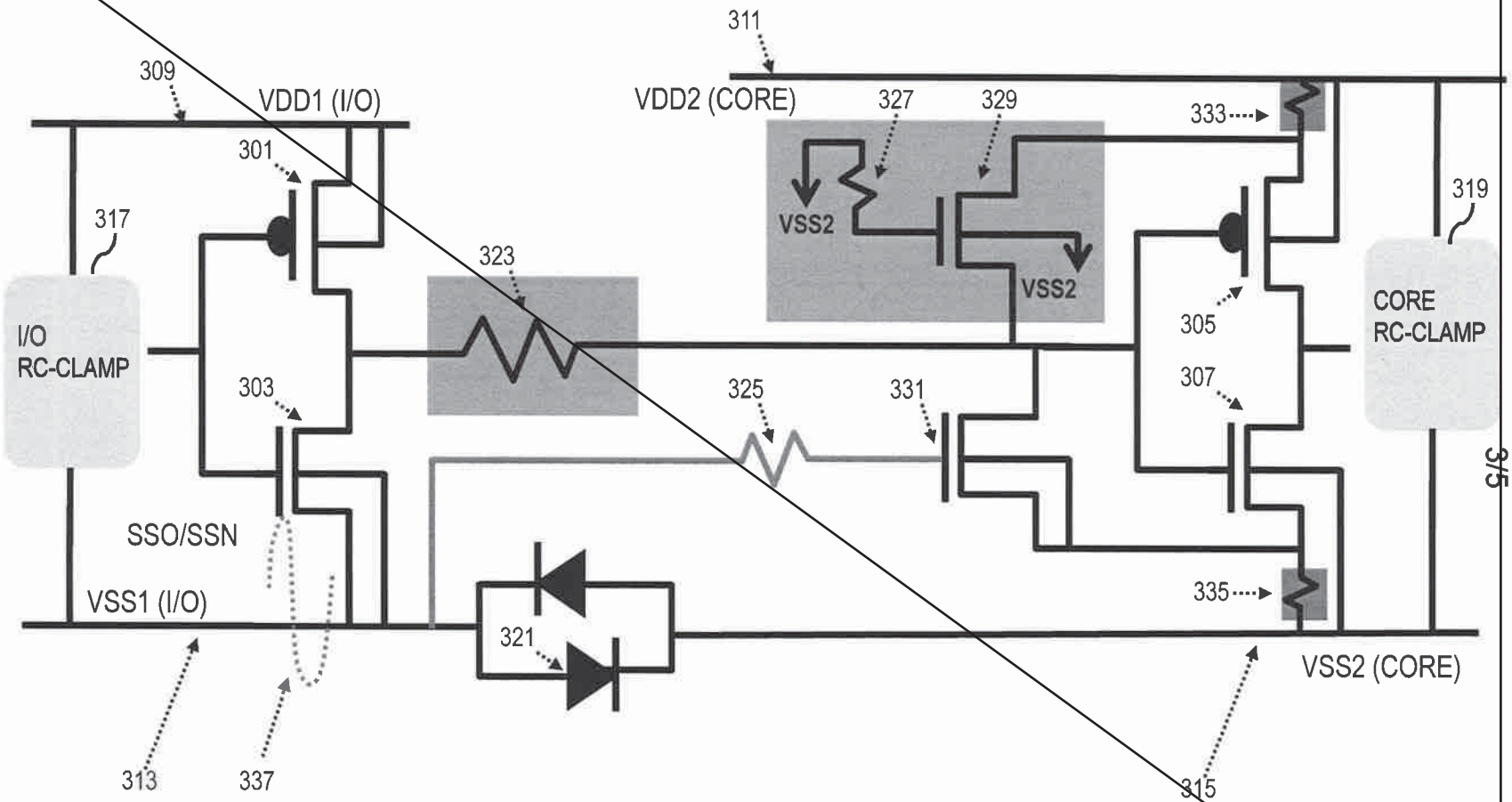
Background Art

FIG. 2



Background Art

FIG. 3



Background Art

FIG. 4A

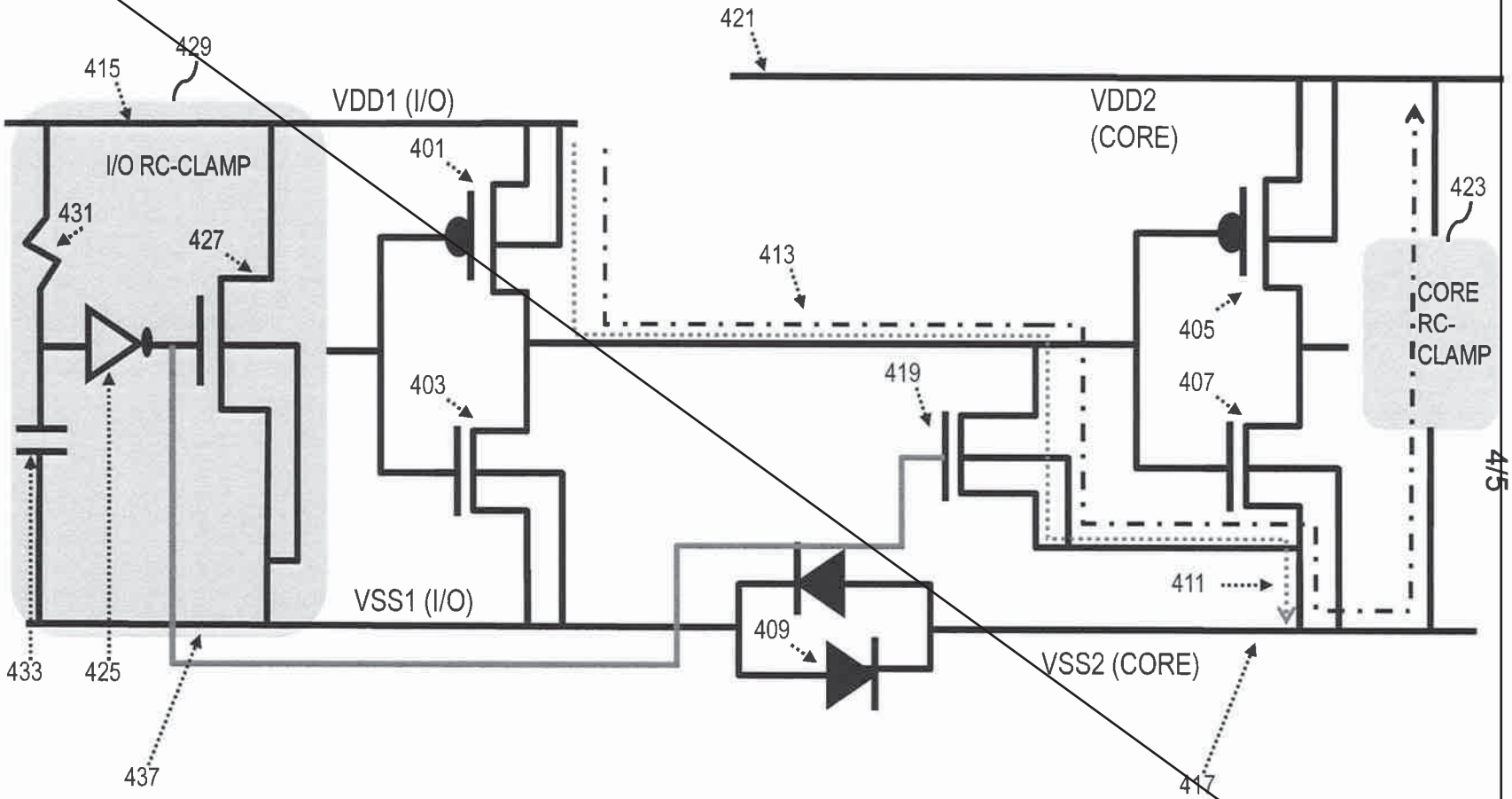
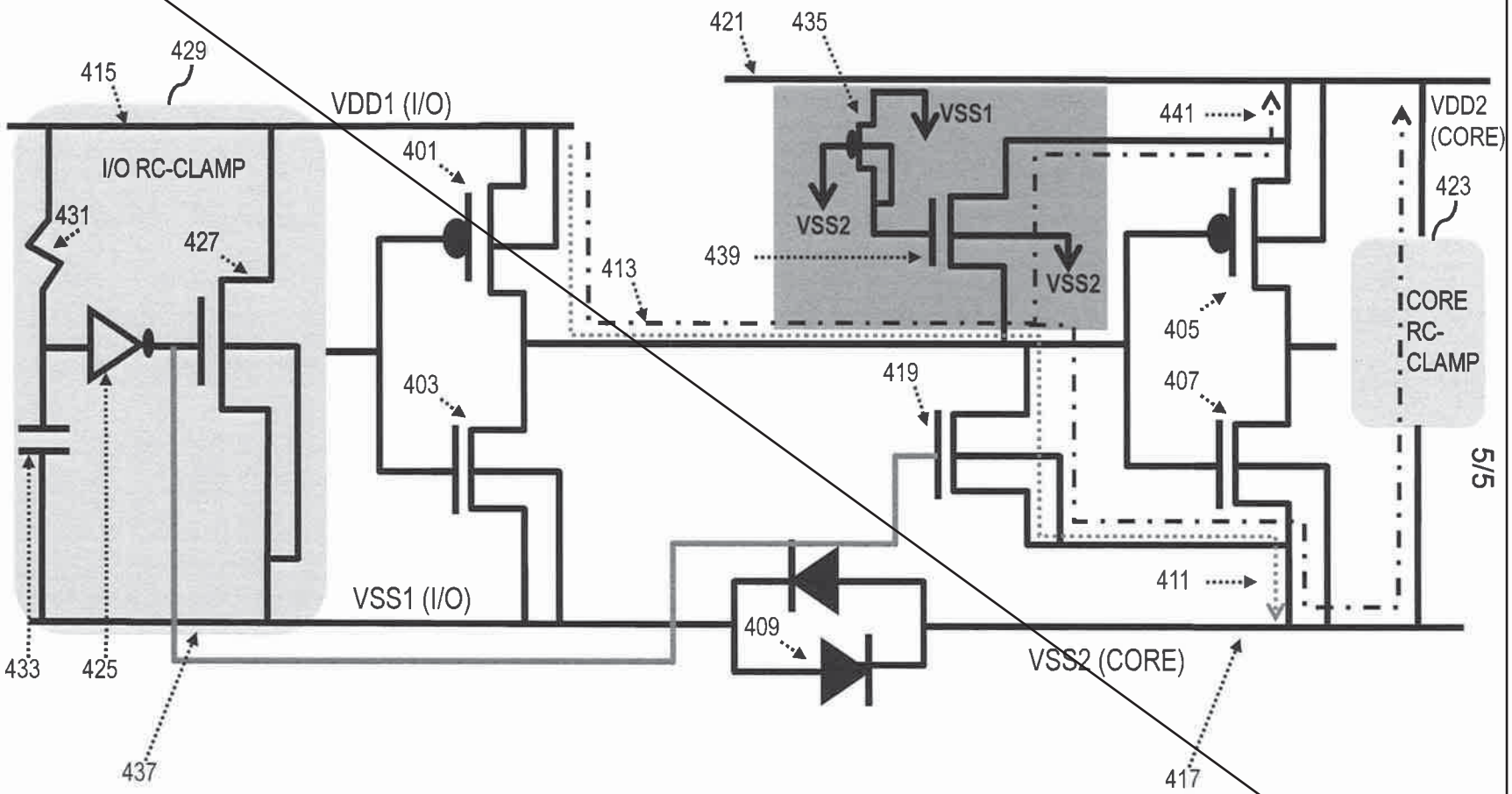

415
429
VDD1 (I/O)
421
VDD2
(CORE)
I/O RC-CLAMP
401
423
431
427
413
CORE
RC-
CLAMP
405
403
419
407
411
VSS1 (I/O)
409
433
425
VSS2 (CORE)
437
417

FIG. 4B


415
429
VDD1 (I/O)
I/O RC-CLAMP
431
427
401
403
413
421
435
VSS1
VSS2
VSS2
439
441
VDD2
(CORE)
423
CORE
RC-
CLAMP
405
407
419
411
VSS1 (I/O)
409
VSS2 (CORE)
433
425
437
417

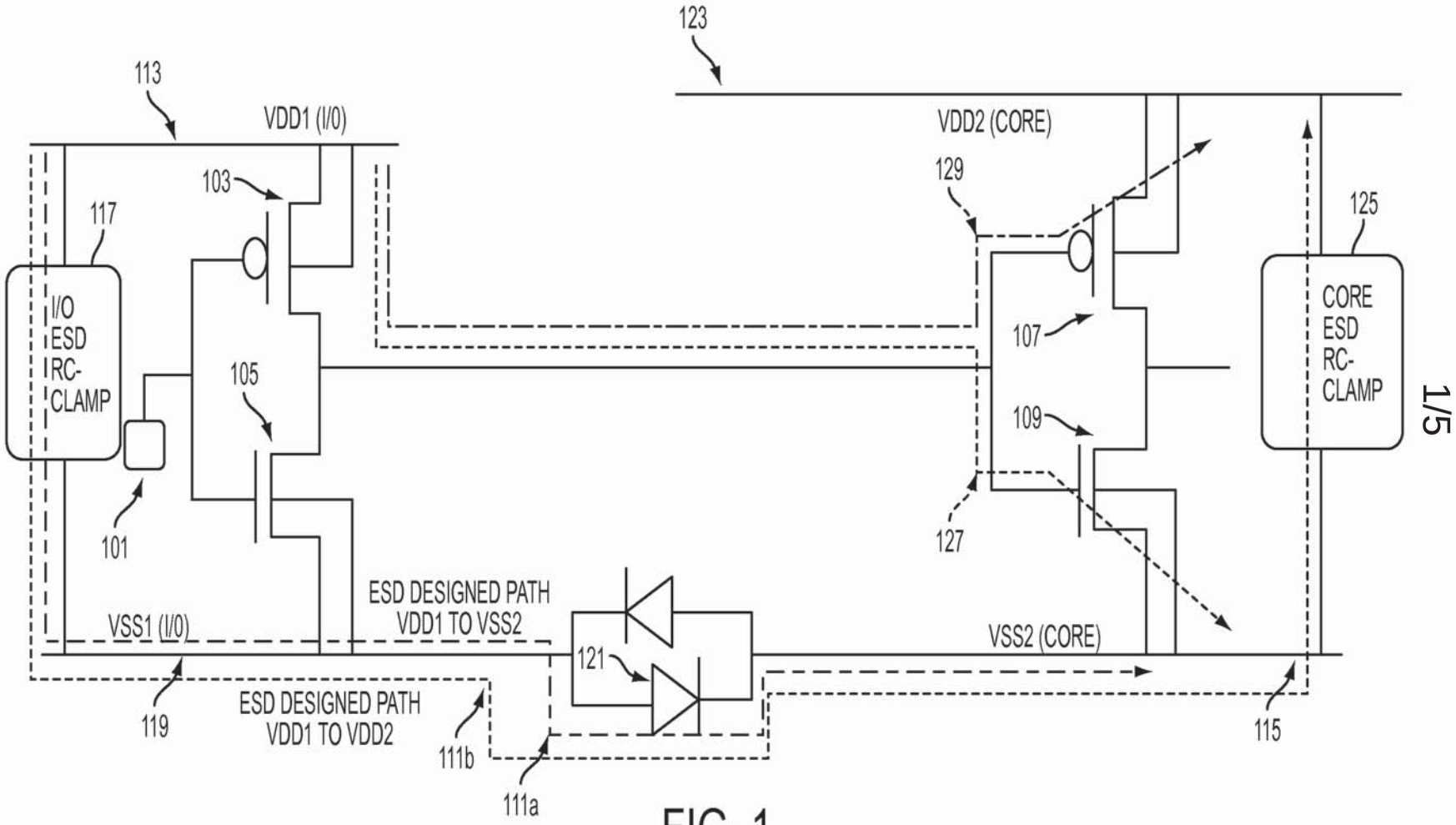


FIG. 1
BACKGROUND ART

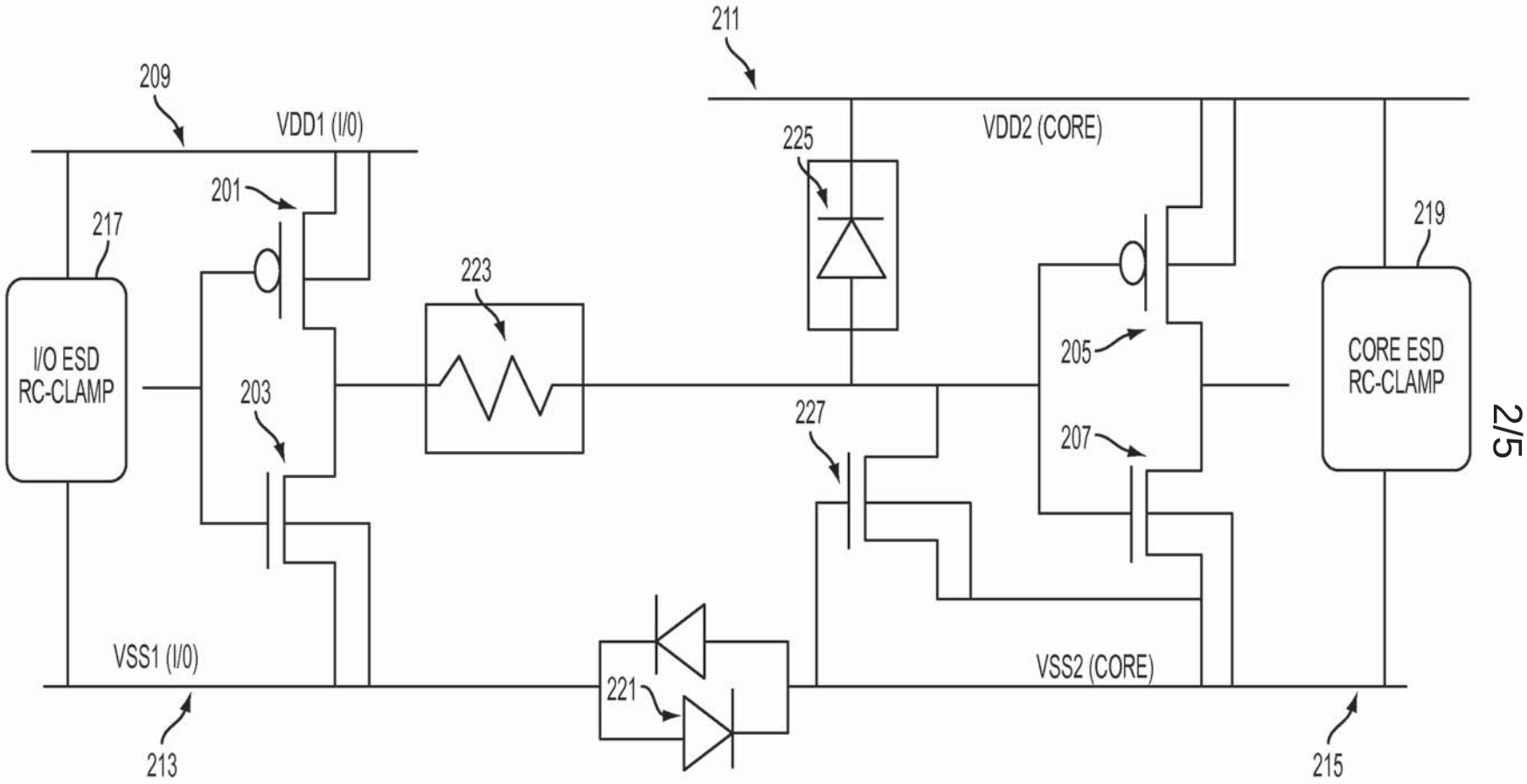


FIG. 2
BACKGROUND ART

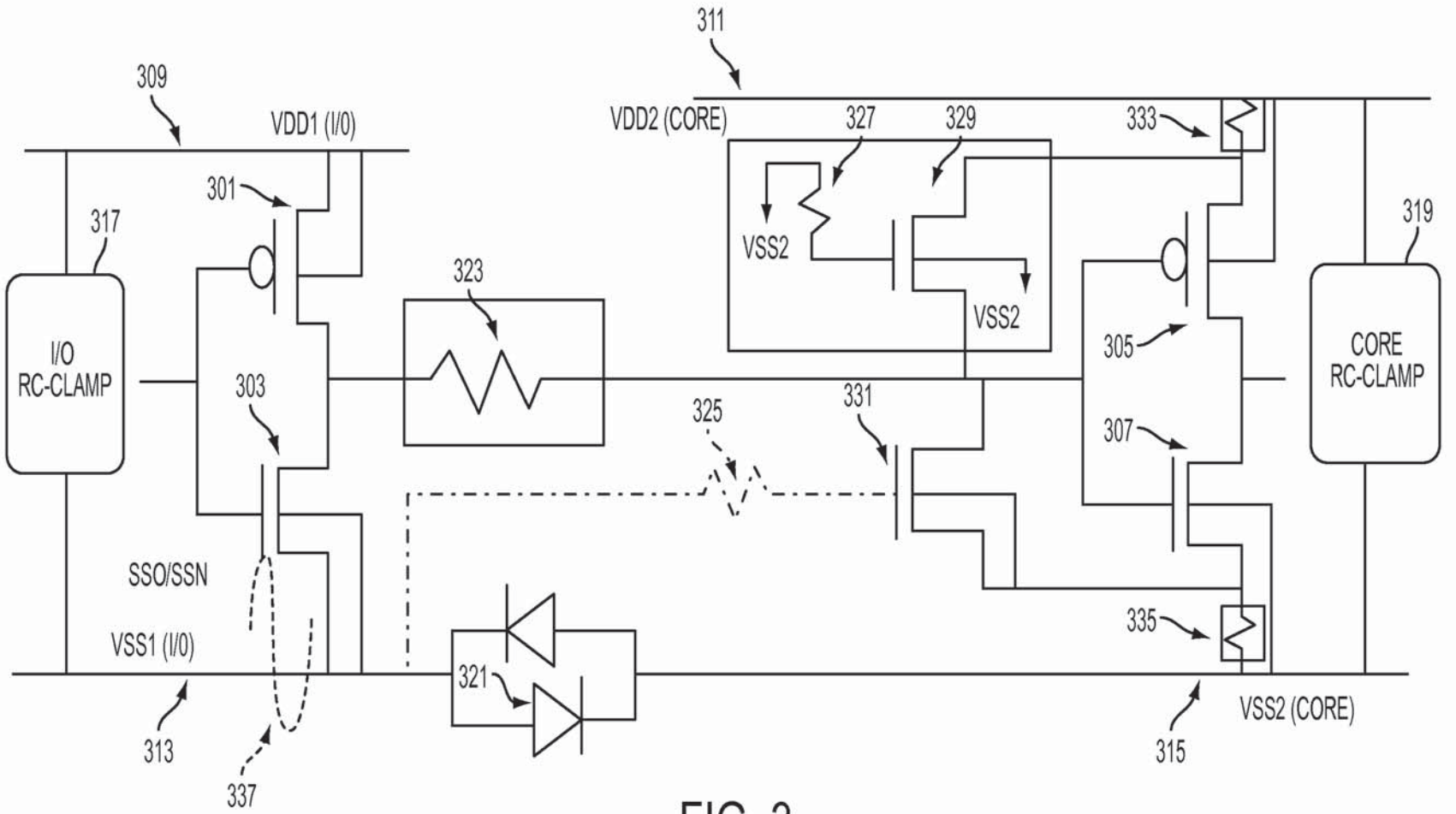


FIG. 3
BACKGROUND ART

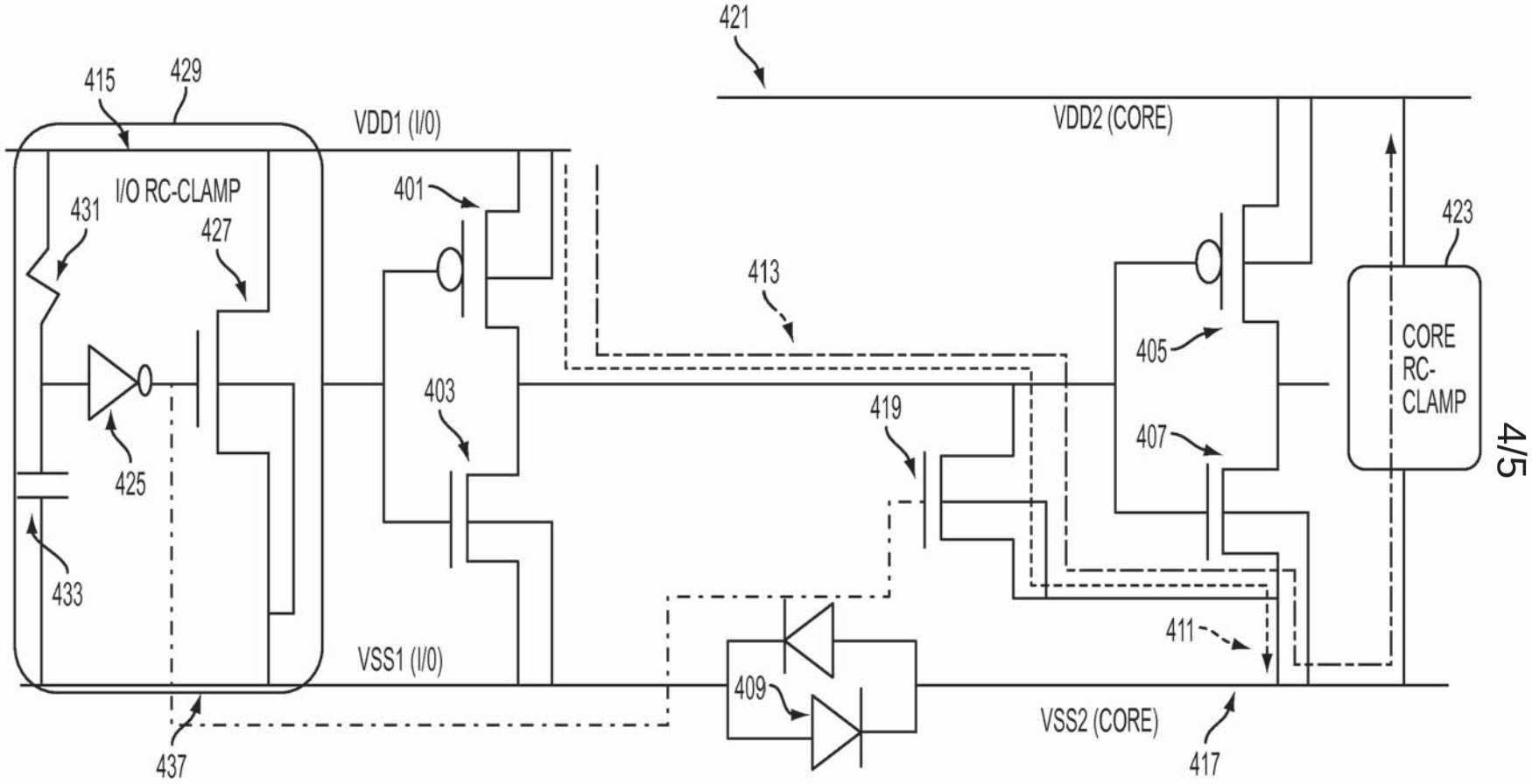

421
415
429
VDD1 (I/O)
VDD2 (CORE)
I/O RC-CLAMP
431
427
401
413
423
CORE
RC-
CLAMP
405
403
419
407
425
433
411
VSS1 (I/O)
409
VSS2 (CORE)
437
417

FIG. 4A

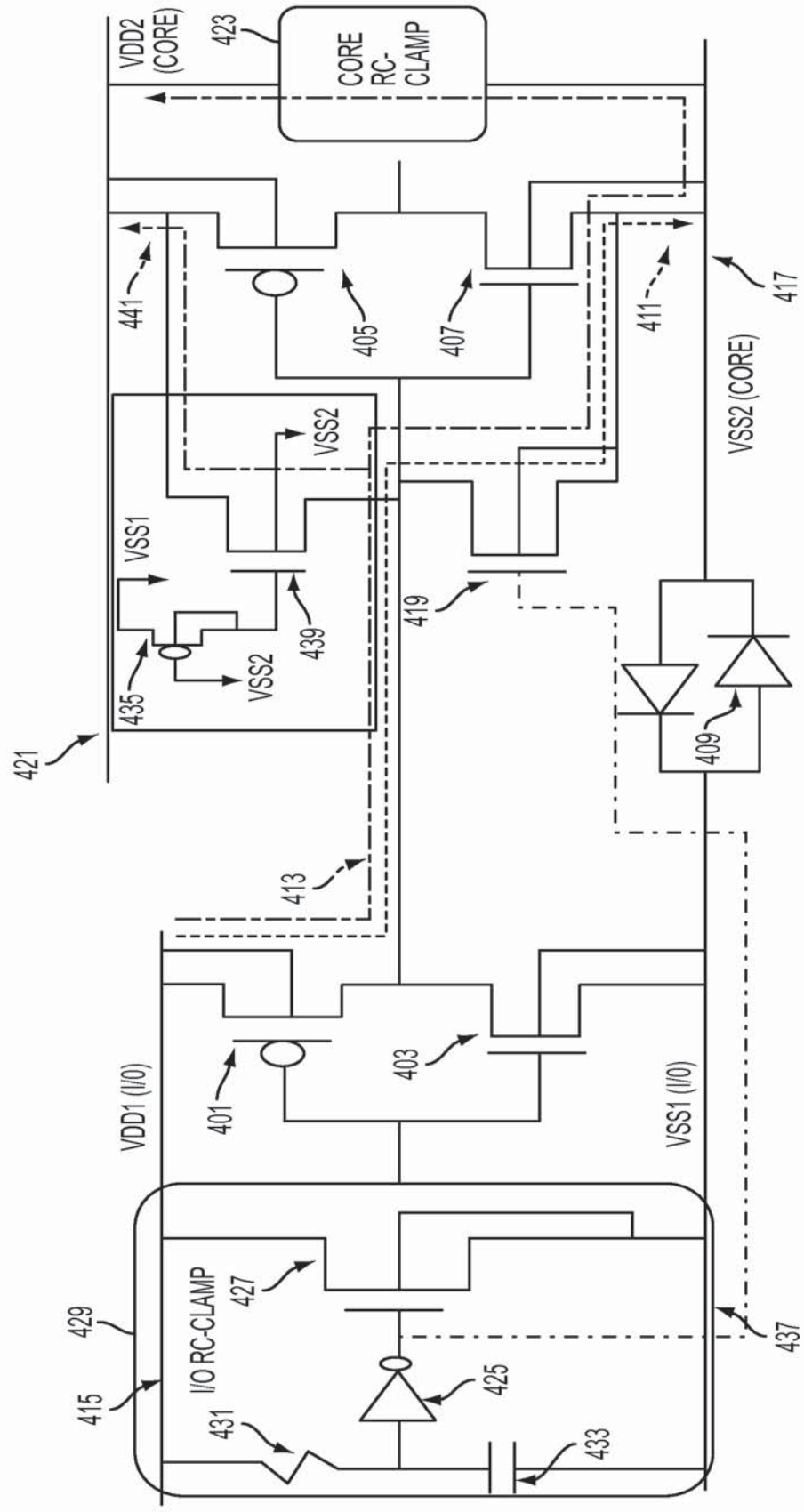

VDD2 (CORE)
423
CORE RC-CLAMP
441
405
407
411
417
VSS2 (CORE)
VSS2
VSS1
435
VSS2
439
419
421
409
413
VDD1 (I/O)
401
403
VSS1 (I/O)
429
I/O RC-CLAMP
427
415
425
431
433
437

FIG. 4B