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ABSTRACT

When a buffer is formed by using transistors having large element characteristic variations, the deviation of the timing between the input clock pulse and the reset pulse is likely to occur. When the deviation of the timing becomes larger, a malfunction is caused to occur, and an operation margin becomes smaller with respect to the variations of the element characteristics. In a timing generation circuit, which is formed on an insulating substrate and which has two TFFs (12, 13), for generating a dot clock DCK and a horizontal clock HCK whose frequencies are different in synchronization with a master clock MCK which is input external to the substrate, separate reset pulses drst and hrst are generated at a pulse generation circuit 15 with respect to the two TFFs (12, 13), and a resetting operation is performed at separate timings. Thus, a large operation margin can be ensured even when each circuit is formed by using TFTs having large element characteristic variations and a rough process rule.