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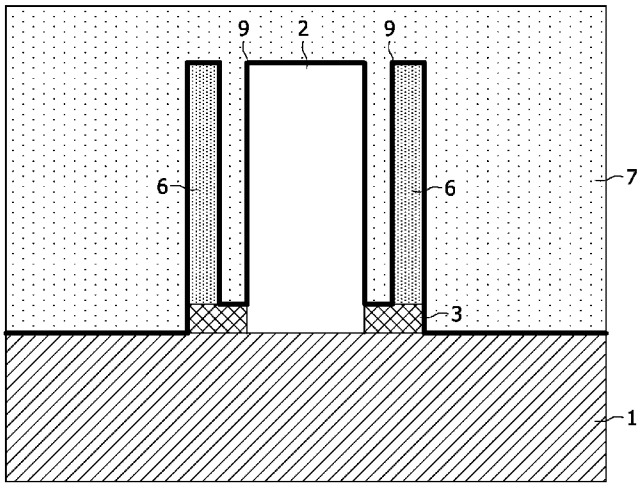
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Declaration under Rule 4.17:
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[Continued on next page]

(54) **Title:** METHOD OF FABRICATING A DUAL-GATE FET



(57) **Abstract:** The invention provides a method of fabricating an extremely short-length dual-gate FET, using conventional semiconductor processing techniques, with extremely small and reproducible fins with a pitch and a width that are both smaller than can be obtained with photolithographic techniques. On a protrusion (2) on a substrate (1), a first layer (3) and a second layer (4) are formed, after which the top surface of the protrusion (2) is exposed. A portion of the first layer (3) is selectively removed relative to the protrusion (2) and the second layer (4), thereby creating a fin (6) and a trench (5). Also a method is presented to form a plurality of fins (6) and trenches (5). The dual-gate FET is created by forming a gate electrode (7) in the trench(es) (5) and a source and drain region. Further a method is presented to fabricate an extremely short- length asymmetric dual-gate FET with two gate electrodes that can be biased separately.

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