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1 Image Encoding Apparatus

BACKGROUND OF THE INVENTIONField of the Invention

5 The present invention relates to an image encoding apparatus and, more particularly, to an image encoding apparatus for quantizing conversion data obtained by converting image information onto a frequency region, and variable-length coding the quantized conversion
10 data.

Related Background Art

In recent years, as an encoding method of a color image signal, an adaptive DCT (discrete cosine transformation) encoding method has been receiving a
15 lot of attention. An encoding method in the JPEG (Joint Photographic Expert Group) organized as an international standard organization of encoding methods of this type employs the DCT encoding method.

A basic system of an encoding method of this
20 system will be briefly described below.

Fig. 2 is a schematic block diagram for explaining an arrangement of a conventional encoding method using DCT conversion, and Figs. 3 to 6 are views for explaining processing of the encoding method shown in
25 Fig. 2. An input terminal 2 receives a digital image signal to be encoded, which signal is obtained by raster scanning. The image signal input to the



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1 terminal 2 is input to an 8×8 blocking circuit 4, and
is two-dimensionally divided into pixel blocks each
consisting of (8×8) pixels. The image signal is
output to the next circuit in units of pixel blocks.

5 A DCT conversion circuit 6 DCT-converts the image
signal from the blocking circuit 4, and outputs an (8×8)
data matrix for a frequency region. More
specifically, a pixel block consisting of image data D_{11}
to D_{88} , as shown in Fig. 3, is converted into a data
10 matrix including X_{11} to X_{88} , as shown in Fig. 4, by the
circuit 6.

Note that X_{11} represents a DC component in the
horizontal and vertical directions of the pixel block,
i.e., an average value of this pixel block. If X_{11} to
15 X_{88} are generally represented by X_{ij} , a component
represented by X_{ij} has a higher frequency in the
vertical direction as i is larger, and has a higher
frequency in the horizontal direction as j is larger.

20 The data matrix output from the DCT conversion
circuit 6 is input to a linear quantization circuit 8.
A quantization matrix generation circuit 18 generates a
quantization matrix (W_{11} to W_{88} ; Fig. 5) indicating
weighting coefficients of quantization step sizes for
DCT coefficients X_{11} to X_{88} , and a coefficient generation
25 circuit 16 generates a coefficient C . The quantization
matrix (W_{11} to W_{88}), and the coefficient C are input to a
multiplication circuit 20. The multiplication circuit



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1 20 calculates ($W_{1j} \times C$), and quantization steps of the
linear quantization circuit 8 are determined by outputs
2 Q_{11} to Q_{88} from the multiplication circuit 20. Note that
the coefficient C has a positive value, and controls
5 the image quality and generation data amount.

In practice, the linear quantization circuit 8
calculates X_{1j}/Q_{1j} , and outputs the calculation results.
Assume that the outputs from the linear quantization
circuit 8 are represented by G_{11} to G_{88} . The quantized
10 conversion data G_{11} to G_{88} are output from a zigzag
scanning circuit 10 sequentially from DC components.
More specifically, the zigzag scanning circuit 10
outputs, to a variable length coding circuit (VLC) 12,
the data G_{11} to G_{88} in the order of G_{11} , G_{12} , G_{21} , G_{31} , G_{22} ,
15 G_{13} , G_{14} , G_{23} , G_{32} , G_{41} , ..., G_{85} , G_{86} , G_{77} , G_{68} , G_{78} , G_{87} , and
 G_{88} .

The VLC 12 calculates a predicted value for, e.g.,
a DC component G_{11} among adjacent pixel blocks, and
Huffman-encodes a predicted error from the predicted
20 value. Alternatively, the VLC 12 performs equal-length
coding of only this DC component. On the other hand,
the VLC encodes AC components G_{12} to G_{88} other than the
DC component G_{11} while zigzag-scanning quantization
25 outputs from low-frequency components to high-frequency
components. The VLC classifies significant
coefficients, which do not correspond to a quantization
output = 0, into groups according to their values, and



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1 Huffman-encodes a set of a group identification number,
and a run length of the number of insignificant
coefficients which correspond to a quantization output
= 0, and are sandwiched between the immediately
5 preceding significant coefficient and a current
significant coefficient. The VLC then adds an
equal-length code indicating the position of a value in
a group.

In general, since high-frequency components in an
10 oblique direction of an image have a low probability of
generation, it can be expected that the latter half
portion of G_{1j} after zigzag scanning often becomes 0.
Therefore, variable length codes obtained in this
manner can be expected to have a very high compression
15 ratio. Assuming a compression ratio between 1/2 to 1/9
as an average, an image almost free from image quality
degradation can be decoded.

On the other hand, a transmission path generally
has a predetermined transmission capacity per unit
20 time. When one frame must be transmitted during each
predetermined period like in a case wherein motion
pictures are to be transmitted, it is desired that a
code to be output has a fixed number of bits in units
of frames or in units of pixel blocks.

25 If the above-mentioned coefficient C is increased,
a probability that G_{1j} becomes 0 is increased, and a
total bit count NB of encoded data is decreased. The



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1 relationship between the coefficient C and the total
bit count NB is expressed by a monotonous decrease
function although it varies depending on images, and it
is known that this relationship is represented by a
5 logarithmic curve shown in Fig. 6 for an average image.

The above-mentioned JPEG, and the like propose a
method of predicting a coefficient C0 for obtaining a
desired total bit count NB0. More specifically, a
given coefficient C1 is encoded, and a total bit count
10 nbl of the obtained code is calculated. A predicted
value C2 of C0 is calculated based on nbl and C1. This
calculation can be predicted since the logarithmic
curve shown in Fig. 6 passes (C1, nbl).

Upon several repetitions of this operation, an
15 encoding amount including several % of an error from
the desired total bit count NB0 can be obtained.

However, processing for repetitively performing
encoding to determine the value of the coefficient C0
is time-consuming, and is not suitable for an encoding
20 apparatus, which must transmit one frame during a
predetermined period of time like in transmission of
motion pictures. In particular, when an image signal
having a very high bit rate such as a high-definition
television signal is to be processed, such processing
25 is impossible.

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1 SUMMARY OF THE INVENTION

 The present invention has been made in consideration of the above situation, and has as its object to provide an image encoding apparatus for
5 quantizing conversion data obtained by converting image information onto a frequency region, and encoding the quantized conversion data, wherein the image encoding apparatus can perform high-speed processing, and can set a data amount in units of frames to be a desired
10 data amount.

 For this purpose, according to one preferred aspect of the present invention, an image encoding apparatus comprises conversion means for converting image information into data on a frequency region,
15 parallel output means for parallelly outputting the converted data to output the converted data of a plurality of channels, quantization means for respectively quantizing the converted data of the plurality of channels output from the parallel output means; operation means for calculating a data amount to
20 be obtained when one of the converted data of the plurality of channels output from the quantization means is encoded, coefficient generation means for generating a quantization coefficient for controlling a
25 quantization step of converted data of other channels of the quantization means, and encoding means for encoding at least one of the converted data of the

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1 plurality of channels output from the quantization means.

Other objects and advantages of the present invention will become apparent from the detailed
5 description to follow taken in conjunction with the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an arrangement of an image encoding apparatus according to the first
10 embodiment of the present invention;

Fig. 2 is a schematic block diagram for explaining an arrangement of a conventional encoding method using DCT conversion;

Fig. 3 is a view showing a pixel block consisting of (8 x 8) image data;
15

Fig. 4 is a view showing a DCT-converted data matrix;

Fig. 5 is a view showing a quantization matrix indicating weighting coefficients of quantization step
20 sizes;

Fig. 6 is a graph showing the relationship between a control coefficient C and a total bit count;

Fig. 7 is a block diagram showing an arrangement of an image encoding apparatus according to the second
25 embodiment of the present invention;

Figs. 8A and 8B are views for explaining a convergence state of the control coefficient C;



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1 Fig. 9 is a block diagram showing an arrangement of an image encoding apparatus according to the third embodiment of the present invention;

5 Fig. 10 is a chart for explaining a control operation of a data transmission order in the apparatus shown in Fig. 9;

 Fig. 11 is a chart for explaining a control operation of a data transmission order of DC and AC components, which are simultaneously obtained;

10 Fig. 12 is a block diagram showing an arrangement of an image encoding apparatus according to the fourth embodiment of the present invention; and

 Fig. 13 is a block diagram showing an arrangement of an image encoding apparatus according to the fifth embodiment of the present invention.

15 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

 The preferred embodiments of the present invention will be described in detail hereinafter with reference to the accompanying drawings.

20 Fig. 1 is a block diagram showing an arrangement of an encoding apparatus according to the first embodiment of the present invention wherein the present invention is applied to a transmission apparatus for transmitting a television signal.

25 In Fig. 1, an input terminal 20 receives a television signal. The television signal input from the terminal 20 is converted into 8-bit digital data by



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1 an A/D converter 22, and is divided into (8 x 8) pixel
blocks by an (8 x 8) blocking circuit 26 for performing
the same operation as that in the blocking circuit
shown in Fig. 2. The television signal is supplied to
5 a DCT conversion circuit 28 in units of blocks.

Pixel data D_{11} to D_{88} of each block are converted by
the DCT conversion circuit 28 into a data matrix (X_{11} to
 X_{88}) for a frequency region in the same manner as in
Fig. 2, and the data matrix is supplied to a zigzag
10 scanning circuit 30. The zigzag scanning circuit 30
performs the same operation as the zigzag scanning
circuit 10 shown in Fig. 2, and outputs the
DCT-converted data matrix (X_{11} to X_{88}) in the order of
 X_{11} , X_{12} , X_{21} , X_{31} , X_{22} , X_{13} , X_{14} , X_{23} , X_{32} , X_{41} , ..., X_{85} , X_{86} ,
15 X_{77} , X_{68} , X_{78} , X_{87} , and X_{88} .

A quantization matrix generation circuit 36
generates the above-mentioned quantization matrix (W_{11}
to W_{88}). In this embodiment, since already
zigzag-scanned data are input to quantization circuits
20 32a to 32e, quantization matrix data W_{11} to W_{88} are
generated in the order corresponding to the zigzag
scanning, and are supplied to multiplication circuits
38a to 38e.

25 The multiplication circuit 38a receives an initial
coefficient $C1$ as the above-mentioned coefficient
(control coefficient) C from an initial coefficient
generation circuit. In this embodiment, the initial



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1 coefficient C1 is set to be "1". When the initial
coefficient C1 is set to be "1", since $W_{1j} = Q_{1j}$, the
multiplication circuit 38a can be omitted, and the
quantization matrix data W_{11} to W_{88} can be directly input
5 to the quantization circuit 32a.

In this manner, the quantization circuit 32a
obtains quantization codes G_{11} to G_{88} based on the
control coefficient C1. These quantized conversion
codes G_{11} to G_{88} are input to a VLC 40a.

10 In this embodiment, VLCs 40a to 40d do not output
actual encoded data, but output only pieces of total
bit count information nb1 to nb4 in units of frames
obtained upon execution of the same processing as in
the VLC 12 in Fig. 2. The total bit count information
15 nb1 output from the VLC 40a is input to a coefficient
operation circuit 44a. Coefficient operation circuits
44a to 44d predict a control coefficient C0
corresponding to a desired total bit count NB0 using
the pieces of total bit count information nb1 to nb4
20 from the VLCs 40a to 40d, the initial coefficient C1,
and outputs C2 to C4 from the coefficient operation
circuits 44a to 44c, and respectively output control
coefficients C2 to C5. The coefficient operation
circuits 44a to 44d output the control coefficients C2
25 to C5, obtained based on conversion data for one frame
input to the quantization circuits 32a to 32d, at the



1 input timing of conversion data for the next frame to
the quantization circuits 32a to 32d.

On the other hand, circuits (1FDLs) 34a to 34d
delay the outputs from the zigzag scanning circuit 30
5 by one frame period. Therefore, the control
coefficient C2 output from the coefficient operation
circuit 44a is input to the multiplication circuit 38b
at the input timing of conversion data for one frame,
which are used for obtaining the control coefficient

10 C2, to the quantization circuit 32b. The
multiplication circuit 38b calculates $(W_{1j} \times C)$, and
inputs the result to the quantization circuit 32b.
More specifically, the quantization circuit 32b
performs the second quantization for a given frame, and
15 obtains quantization codes $G2_{11}$ to $G2_{22}$ based on the
control coefficient C2. The quantized conversion codes
 $G2_{11}$ to $G2_{22}$ are input to the VLC 40b.

The operations of coefficient operation circuits
44b to 44d, the multiplication circuits 38c to 38e, the
20 1FDLs 34b to 34d, the VLCs 40b to 40d, and the
quantization circuits 32c to 32e are respectively the
same as those of the coefficient operation circuit 44a,
the multiplication circuit 38b, the 1FDL 34a, the VLC
40a, and the quantization circuit 32b. These circuits
25 sequentially update the predicted value of a desired
control coefficient for a given frame.



1 Thus, the predicted value C5 of the control
coefficient obtained from the coefficient operation
circuit 44d can be caused to converge to a value very
close to the control coefficient C0 corresponding to
5 the desired total bit count NB0. In this embodiment,
the control coefficient C5 is supplied to the
multiplication circuit 38e as a final control
coefficient C. The output from the multiplication
circuit 38e is supplied to the quantization circuit
10 32e. The quantization circuit 32e quantizes the output
from the 1FDL 34d, i.e., conversion data, which are
delayed by a total of four frame periods, and supplies
the quantized data to a VLC 40e.

 The VLC 40e actually performs encoding that was
15 described earlier with reference to Fig. 2, and outputs
encoded data (DATA). The encoded data are output from
an entry buffer 46 at a predetermined bit rate, and are
multiplexed with the final control coefficient C by a
multiplexer 48. The multiplexed data are then output
20 from a terminal 50 onto a transmission path.

 The second embodiment of the present invention
will be described below.

 Fig. 7 is a block diagram showing an arrangement
of an encoding apparatus according to the second
25 embodiment of the present invention wherein the present
invention is applied to a transmission apparatus for
transmitting a television signal.



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1 Note that the same reference numerals in Fig. 7
denote the same parts as in Fig. 1, and a detailed
description thereof will be omitted.

 In this embodiment, a coefficient operation
5 circuit 41 supplies a predicted initial coefficient as
the above-mentioned quantization coefficient (control
coefficient) C1 to a multiplication circuit 38a. Note
that the predicted initial coefficient will be
described later. The coefficient operation circuit 41
10 predicts a control coefficient C0 corresponding to a
desired total bit count NB0 using pieces of total bit
count information nb1 to nb4 from VLCs 40a to 40d, the
initial coefficient C1, and outputs C2 to C4 of this
operation circuit 41, and outputs control coefficients
15 C2 to C5. The coefficient operation circuit 41 outputs
the control coefficients C2 to C5, obtained based on
conversion data for one frame input to quantization
circuits 32a to 32d, at the input timing of conversion
data for the next frame to the quantization circuits
20 32a to 32d.

 The arrangement and operations of the second
embodiment are the same as those of the encoding
apparatus of the first embodiment, except for the
above-mentioned arrangement and operations.

25 The predicted initial coefficient will now be
described.



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1 In general, motion pictures have a high
correlation among frames. For this reason, when
adaptive DCT encoding is performed to set a control
coefficient (quantization coefficient) so as to
5 maintain a constant total data amount for one picture
(one frame), the control coefficients become almost the
same among frames.

In this embodiment, by utilizing the high correlation among frames, a value obtained in the immediately preceding frame is used as a control coefficient to be input to the multiplication circuit 38a. Thus, a convergence time of the control coefficients C2 to C5 until an optimum control coefficient is obtained can be shortened, and a more accurate control coefficient can be obtained.

A further detailed explanation will be made below with reference to Figs. 8A and 8B.

Fig. 8A shows values C1 to C5 when a control coefficient of a given frame is obtained. As can be seen from Fig. 8A, the control coefficient converges to a target optimum control coefficient value while oscillating.

Fig. 8B shows values C1 to C5 when a control coefficient of a frame next to the given frame is obtained. The initially input value C1 is the control coefficient C2 of the immediately preceding frame, i.e., the value C2 (this value will be referred to as a

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1 predicted initial coefficient) shown in Fig. 8A. It
can be regarded that an optimum control coefficient of
this frame is almost the same as that of the
immediately preceding frame. Thus, since the value C1
5 becomes closer to the optimum control coefficient, the
convergence time can be shortened, and a value closer
to the optimum control coefficient can be obtained.

As the correlation among frames is higher, images
having higher image quality can be obtained upon
10 repetition of this operation.

The third embodiment of the present invention will
be described below.

Fig. 9 is a block diagram showing an arrangement
of an encoding apparatus according to the third
15 embodiment of the present invention wherein the present
invention is applied to a transmission apparatus for
transmitting a television signal.

Note that the same reference numerals in Fig. 9
denote the same parts as in Fig. 1, and a detailed
20 description thereof will be omitted.

In Fig. 9, VLCs 40a to 40d of this embodiment
calculate total data amounts of only AC components
after encoding, and output pieces of total bit count
information nb1 to nb4 in units of frames. On the
25 other hand, DC components are equal-length coded.

The operations up to a multiplication circuit 38e,
except for the above-mentioned processing operations of



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1 the VLCs 40a to 40d, are the same as those in the first
embodiment. The processing operations after the
multiplication circuit 38e will be described in detail
below.

5 The output from the multiplication circuit 38e is
supplied to a quantization circuit 32e. The
quantization circuit 32e quantizes outputs from a 1FDL
34d, i.e., at least AC components of conversion data
delayed by a total of four frame periods, and supplies
10 quantized data $G5_{12}$ to $G5_{88}$ to a VLC 40e.

The VLC 40e actually performs encoding that was
described above with reference to Fig. 2, on AC components
 $G5_{12}$ to $G5_{88}$, and outputs encoded data (DATA).

On the other hand, DC components are separated
15 from the outputs from a 1FDL 34c by a DC extraction
circuit 51, and are input to a quantization circuit 52.
The quantization circuit 52 quantizes a DC component X_{11}
by a predetermined quantization step independently of
the above-mentioned coefficient C, and inputs the
20 quantized component to a coding circuit 54.

The coding circuit 54 equal-length codes the
above-mentioned DC component by, e.g., predicted
differential encoding. DC component data equal-length
coded by the coding circuit 54, and AC component data
25 variable-length coded by the VLC 40e, as described
above, are respectively input to buffer memories 56 and
46.



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1 The read operations of encoded data from the
memories 46 and 56 are controlled by a buffer control
circuit 58. In this case, control is made as follows.
That is, as for encoded data for a given frame, all the
5 DC component encoded data of the frame are read out
first, and then, AC component encoded data of the same
frame are read out.

 The relationship between read and write timings of
data stored in the memories 46 and 56 will be described
10 below.

 Fig. 10 is a chart showing the data write timings
to the memory 46, i.e., the write timings of AC
component encoded data (AC), the data write timings to
memory 56, i.e., the write timings of DC component
15 encoded data (DC), and the data read timings from these
two memories.

 Since DC component encoded data (DATA-2) is
quantized by the constant quantization step
independently of the above-mentioned coefficient C,
20 quantization can be performed before determination of
the final coefficient C in the coefficient operation
circuit 44d.

 For this reason, in Fig. 9, DC component data are
separated and extracted by the DC extraction circuit 51
25 at the input side of the 1FDL 34d at the final stage,
and are quantized by the quantization circuit 52.



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1 Thus, during a period for which AC component
encoded data (AC) of a frame of interest are written in
the memory 46, DC component encoded data (DC) of the
same frame already stored in the memory 56 can be read
5 out prior to the AC component encoded data (AC).

On the other hand, Fig. 11 is a chart showing the
relationship between read and write timings of data
corresponding to AC component encoded data (AC) and DC
component encoded data (DC) when the AC and DC
10 component data are quantized and encoded during a
single frame period without using the DC extraction
circuit 51.

In this case, since read access is performed to be
delayed by one frame from write access to change the
15 transmission order of data, a capacity for two frames
is required for a memory of AC component data.

As can be understood from the above description, a
memory capacity required when the transmission order of
data is changed in units of frames corresponds to two
20 frames according to the conventional arrangement.
However, in this embodiment, a memory having a capacity
for one frame need only be arranged for AC component
encoded data (AC) so as to change the data transmission
order.

25 Needless to say, the memories 46 and 56 also have
a buffer function for reading out data at a
predetermined bit rate.



1 At this time, the buffer control circuit 58
controls to slightly delay the data read start timing
of each frame from the write start timing, so that the
read addresses of data from the memory 46 do not
5 overtake write addresses.

The AC component encoded data (AC) and the DC
component encoded data (DC) read out from the memories 46
and 56, as described above, are multiplexed by a
multiplexer 48 together with the final coefficient C,
10 and the multiplexed data are output from a terminal 60
onto a transmission path at a predetermined bit rate.

The fourth embodiment of the present invention
will be described below.

Fig. 12 is a block diagram showing an arrangement
15 of an encoding apparatus according to the fourth
embodiment of the present invention wherein the present
invention is applied to a transmission apparatus for
transmitting a television signal.

Note that the same reference numerals in Fig. 12
20 denote the same parts as in Fig. 1, and a detailed
description thereof will be omitted.

This embodiment assumes an apparatus, which does
not permit that the total bit count of each frame after
variable-length coding exceeds a desired total bit
25 count NBO even slightly.

Therefore, unlike in the first to third
embodiments, a predicted control coefficient is not



1 directly used. This embodiment selects, from control
coefficients for a given frame, a control coefficient
corresponding to a total bit count after
variable-length coding, which is less than and closest
5 to the desired total bit count NB0.

The arrangement and operations except for those
associated with this selection are the same as those of
the first embodiment.

The operation associated with the above-mentioned
10 selection will be described below.

In Fig. 12, a four-frame period delay circuit
(4FDL) 55a, a three-frame period delay circuit (3FDL)
55b, a two-frame period delay circuit (2FDL) 55c, and a
one-frame period delay circuit (1FDL) 55d respectively
15 delay control coefficients C1, C2, C3, and C4. With
these circuits, the control coefficients C1, C2, C3,
and C4 input to a coefficient selector 53 become those
for an image of a single frame. These coefficients C1
to C4 are input to the coefficient selector 53 at the
20 input timing of an image of the corresponding frame to
a quantization circuit 32e through a 1FDL 34d.

The timings of pieces of total bit count
information nb1 to nb4 obtained when quantization and
encoding are performed using these control coefficients
25 C1 to C4 are adjusted to each other by a 3FDL 57a, a
2FDL 57b, and a 1FDL 57c. More specifically, the
pieces of total bit count (data mount) information nb1



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1 to nb4 corresponding to the control coefficients C1 to
C4 input to the coefficient selector 53 are input to a
coefficient decision circuit 59 immediately before a
period for which these control coefficients C1 to C4
5 are input to the coefficient selector 53.

The coefficient decision circuit 59 detects
information corresponding to a total bit count, which
is less than and closest to the desired total bit count
NB0, and supplies 2-bit control information to the
10 coefficient selector 53 according to the detection
result.

Therefore, the coefficient selector 53 selects a
control coefficient corresponding to a total bit count,
which is less than and closest to the desired total bit
count NB0 upon variable-length coding, from the control
15 coefficients C1 to C4, and outputs the selected
coefficient.

In this embodiment, the control coefficient output
from the coefficient selector 53 is determined as a
20 final control coefficient C, and is supplied to a
multiplication circuit 38e. The output from the
multiplication circuit 38e is supplied to the
quantization circuit 32e. The quantization circuit 32e
quantizes outputs from the 1FDL 34d, i.e., conversion
25 data delayed by a total of four frame periods, and
supplies the quantized data to a VLC 40e.



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1 The VLC 40e actually performs encoding that was
described above with reference to Fig. 2, and outputs
encoded data (DATA). The encoded data are output from
an entry buffer 46 at a predetermined bit rate, and are
5 multiplexed with the final control coefficient C by a
multiplexer 48. The multiplexed data are then output
from a terminal 50 onto a transmission path.

The fifth embodiment of the present invention will
be described below.

10 Fig. 13 is a block diagram showing an arrangement
of an encoding apparatus according to the fifth
embodiment of the present invention wherein the present
invention is applied to a transmission apparatus for
transmitting a television signal.

15 Note that the same reference numerals in Fig. 13
denote the same parts as in Fig. 1, and a detailed
description thereof will be omitted.

 This embodiment assumes an apparatus, which does
not permit that the total bit count of each frame after
20 variable-length coding exceeds a desired total bit
count NB0 even slightly, like in the above-mentioned
fourth embodiment.

 The arrangement and operations except for those to
be described below are the same as those in the first
25 embodiment.



1 In Fig. 13, VLCs 40a to 40d of this embodiment
output pieces of total bit count information in units
of frames, and actually encoded codes.

5 Pieces of total bit count information nb1 to nb5
calculated by the VLCs 40a to 40e are input to a rate
fixer 43. The rate fixer 43 discriminates, from nb1 to
nb5 for a single frame, total bit count information
corresponding to a total bit count, which is equal to
or smaller than and closest to NB0, and determines a
10 control coefficient giving the total bit count and
encoded codes as a final control coefficient and
encoded codes.

 Data buffers 45a to 45j are used for supplying
encoded codes d1 to d4, output from the VLCs 40a to 40d
15 for the same frame as a frame corresponding to an
encoded code d5 output from a VLC 40e, to a data
selection switch 47 at the same timing as the encoded
code d5. The data buffers 45a to 45j delay (buffer)
control coefficients C1 to C4 giving the four encoded
20 codes d1 to d4 for a single frame, so that these
control coefficients are supplied to the data selection
switch at the same timing as the encoded codes d1 to
d4.

 The rate fixer 43 controls the data selection
25 switch 47 to output one of the encoded code d5 output
from the VLC 40e, and the encoded codes d1, d2, d3, and
d4 output from the data buffers 45d, 45g, 45i, and 45j



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1 as a final encoded code DATA. In addition to the final
encoded code, the data selection switch 47 outputs one
of the control coefficient C5 output from a coefficient
operation circuit 44d, and the control coefficients C1,
5 C2, C3, and C4 output from the data buffers 45d, 45g,
45i, and 45j as a final control coefficient F.

The encoded code DATA and the control coefficient
F are multiplexed by a multiplexer 48, and are output
from a terminal 50 onto a transmission path.

10 According to the arrangement of each of the above
embodiments, since the control coefficient C is not fed
back at all, a period required for processing for one
frame can become the same as that of processing using a
constant control coefficient C although a calculation
15 of the control coefficient C for a single frame is
performed five times. Thus, very high-speed processing
can be realized.

In the third embodiment, the data transmission
order can be changed, i.e., DC component encoded data
20 (DC) can be output prior to AC component data using a
small memory capacity.

Note that various modifications of the present
invention may be made without departing from the spirit
and the principal features of the invention.

25 For example, in order to realize very high-speed
processing, the control coefficient F is determined in
units of frames. However, if there is a margin for a

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1 processing time, a unit (period) for determining the
value of the control coefficient F can be decreased
(shortened).

5 In each of the above embodiments, the coefficient
operation circuits 44b to 44d predict the desired
control coefficient C0 using the coefficients C2 to C4
output from the coefficient operation circuits 44a to
44c, and the pieces of total bit count information nb2
10 to nb4 obtained when quantization and variable-length
coding are performed according to the coefficients C2
to C4. These circuits can more accurately predict the
control coefficient using coefficients and total bit
count information at the immediately preceding stages
in addition to the above-mentioned coefficients and
15 information. For example, if the coefficient operation
circuit 44b uses the coefficients C1 and C2 and the
pieces of total bit count information nb1 and nb2 so as
to calculate the coefficient C3, the coefficient C0 can
be predicted more accurately.

20 In each of the above embodiments, in order to
parallelly output DCT-converted data X having a time
difference of one frame period, the 1FDLs 34a to 34d
are series-connected at the output side of the DCT
conversion circuit 28 and the zigzag scanning circuit
25 30. When the number of bits of the DCT-converted data
X must be increased, a plurality of 1FDLs may be
connected in series at the output side of the (8 x 8)



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1 blocking circuit 26 so as to save the memory capacity
of the 1FDLs, and the outputs of the 1FDLs may be
connected to the DCT conversion circuit and the zigzag
scanning circuit.

5 In the fifth embodiment, the encoded code output
from the VLCs 40a to 40e for a single frame can be
output. In practice, the same effect can be obtained
in such a manner that the encoded codes from only the
VLCs 40d and 40d can be output, or the encoded codes
10 output from the VLCs 40c to 40e can be selectively
output. In this case, the capacity of each data buffer
can be decreased as compared to the embodiment shown in
Fig. 13, and an increase in hardware size can be
suppressed.

15 Therefore, the above-mentioned embodiments are
merely examples in all respects, and must not be
construed to limit the invention.

The scope of the present invention is defined by
the scope of the appended claims, and is not limited at
20 all by the specific descriptions of this specification.
Furthermore, all the modifications and changes
belonging to equivalents of the claims are considered
to fall within the scope of the present invention.

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1 WHAT IS CLAIMED IS:

1. An image encoding apparatus comprising:

a) conversion means for converting image
information into data on a frequency region;

5 b) parallel output means for parallelly
outputting the converted data to output the converted
data of a plurality of channels;

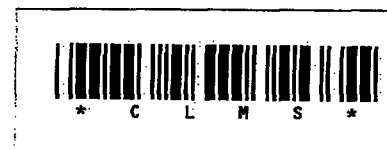
c) quantization means for respectively quantizing
the converted data of the plurality of channels output
10 from said parallel output means;

d) operation means for calculating a data amount
to be obtained when one of the converted data of the
plurality of channels output from said quantization
means is encoded;

15 e) coefficient generation means for generating a
quantization coefficient for controlling a quantization
step of converted data of other channels of said
quantization means according to an output from said
operation means; and

20 f) encoding means for encoding at least one of
the converted data of the plurality of channels output
from said quantization means.

2. An apparatus according to claim 1, wherein
25 said conversion means performs DCT (Discrete Cosine
Transform) conversion.



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1 3. An apparatus according to claim 1, wherein
said encoding means encodes only one of the converted
data of the plurality of channels quantized by said
quantization means.

5

 4. An apparatus according to claim 3, further
comprising multiplexing means for multiplexing encoded
data output from said encoding means, and the
quantization coefficient for obtaining the encoded
10 data.

 5. An apparatus according to claim 1, wherein the
converted data of the plurality of channels output from
said parallel output means have a time difference of a
15 predetermined period therebetween.

 6. An apparatus according to claim 5, wherein
said operation means calculates a data amount, which is
to be obtained when one of the converted data of the
20 plurality of channels is encoded, in units of
predetermined periods.

 7. An apparatus according to claim 5, wherein
said coefficient generation means updates the
25 quantization coefficient in units of predetermined
periods.



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1 8. An apparatus according to claim 5, wherein the
predetermined period is one frame period.

 9. An image processing apparatus comprising:

5 a) conversion means for converting image
information into data on a frequency region;

 b) parallel output means for parallelly
outputting the converted data to output the converted
data of a plurality of channels;

10 c) a plurality of quantization means for
respectively quantizing the converted data of the
plurality of channels output from said parallel output
means;

 d) operation means for calculating a data amount
15 to be obtained when one of the converted data output
from said plurality of quantization means is encoded;

 e) coefficient generation means for generating a
quantization coefficient for controlling a quantization
step of another one of said plurality of quantization
20 means according to an output from said operation means;
and

 f) coefficient supply means for supplying, as a
quantization coefficient used in one quantization
means, a quantization coefficient used in quantization
25 of another quantization means.



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1 10. An apparatus according to claim 9, further
comprising encoding means for encoding one of the
converted data of the plurality of channels quantized
by said plurality of quantization means.

5

11. An apparatus according to claim 9, wherein the
converted data of the plurality of channels output from
said parallel output means have a time difference of a
predetermined period therebetween.

10

12. An apparatus according to claim 11, wherein
said operation means calculates a data amount, which is
to be obtained when the converted data quantized by one
of said plurality of quantization means is encoded, in
15 units of predetermined periods.

13. An apparatus according to claim 11, wherein
said coefficient generation means updates the
quantization coefficient in units of predetermined
20 periods.

14. An apparatus according to claim 11, wherein
the predetermined period is one frame period.

25 15. An image encoding apparatus comprising:
a) conversion means for converting image
information into data on a frequency region;



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- 1 b) parallel output means for parallelly
outputting the converted data to output the converted
data of a plurality of channels;
- c) quantization means for respectively quantizing
5 the converted data of the plurality of channels output
from said parallel output means;
- d) operation means for calculating a data amount
to be obtained when at least an AC component of one of
the converted data of the plurality of channels output
10 from said quantization means is encoded;
- e) coefficient generation means for generating a
quantization coefficient for controlling a quantization
step of converted data of other channels of said
quantization means according to an output from said
15 operation means;
- f) first encoding means for encoding at least the
AC component of one of the converted data of the
plurality of channels output from said quantization
means;
- 20 g) second encoding means for encoding at least a
DC component of the one of the converted data of the
plurality of channels; and
- h) multiplexing means for multiplexing outputs
from said first and second encoding means.

25

16. An apparatus according to claim 15, wherein
the converted data of the plurality of channels output



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1 from said parallel output means have a time difference
of a predetermined period therebetween.

5 17. An apparatus according to claim 16, wherein
said operation means calculates a data amount, which is
to be obtained when the AC component of one of the
converted data of the plurality of channels is encoded,
in units of predetermined periods.

10 18. An apparatus according to claim 16, wherein
said coefficient generation means updates the
quantization coefficient in units of predetermined
periods.

15 19. An apparatus according to claim 16, wherein
said second encoding means encodes the converted data
delayed by the predetermined period from the converted
data encoded by said first encoding means.

20 20. An apparatus according to claim 15, wherein
said multiplexing means multiplexes the outputs from
said first and second encoding means, so that the
output from said second encoding means advances from
the output from said first encoding means.

25

21. An image encoding apparatus comprising:



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- 1 a) conversion means for converting image
information into data on a frequency region;
- b) parallel output means for parallelly
outputting the converted data to output the converted
5 data of a plurality of channels;
- c) quantization means for respectively quantizing
the converted data of the plurality of channels output
from said parallel output means;
- d) operation means for calculating a plurality of
10 data amounts to be obtained when the converted data of
the plurality of channels output from said quantization
means are encoded;
- e) coefficient generation means for generating a
plurality of quantization coefficients for controlling
15 a quantization step of said quantization means
according to an output from said operation means;
- f) selection means for selecting one of the
plurality of quantization coefficients; and
- g) encoding means for encoding the quantized
20 converted data using the quantization coefficient
output from said selection means.

22. An apparatus according to claim 21, wherein
the converted data of the plurality of channels output
25 from said parallel output means have a time difference
of a predetermined period therebetween.



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1 23. An apparatus according to claim 21, wherein
said selection means selects a quantization coefficient
for obtaining a data amount smaller than and closest to
a desired data amount from the plurality of data
5 amounts.

24. An apparatus according to claim 21, further
comprising multiplexing means for multiplexing the
encoded data output from said encoding means, and the
10 quantization coefficient for obtaining the encoded
data.

25. An apparatus according to claim 22, wherein
said selection means comprises a circuit for
15 compensating for a time difference in the plurality of
quantization coefficients output from said coefficient
generation means.

26. An apparatus according to claim 22, wherein
20 said operation means calculates data amounts, which are
to be obtained when the converted data quantized by
said quantization means are encoded, in units of
predetermined periods.

25 27. An apparatus according to claim 22, wherein
said coefficient generation means updates the



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1 quantization coefficient in units of predetermined
periods.

28. An image encoding apparatus comprising:

- 5 a) conversion means for converting image
information into data on a frequency region;
- b) parallel output means for parallelly
outputting the converted data to output the converted
data of a plurality of channels;
- 10 c) quantization means for respectively quantizing
the converted data of the plurality of channels output
from said parallel output means;
- d) operation means for calculating a data amount
to be obtained when one of the converted data of the
15 plurality of channels output from said quantization
means are encoded;
- e) control means for controlling said
quantization means according to an output from said
operation means;
- 20 f) a plurality of encoding means for respectively
encoding at least two of the converted data of the
plurality of channels quantized by said quantization
means; and
- g) selection means for selectively outputting
25 encoded codes output from said plurality of encoding
means.



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1 29. An apparatus according to claim 28, wherein
the converted data of the plurality of channels output
from said parallel output means have a time difference
of a predetermined period therebetween.

5

 30. An apparatus according to claim 28, wherein
said selection means selects an encoded code smaller
than and closest to a desired data amount from the
encoded codes output from said plurality of encoding
10 means.

 31. An apparatus according to claim 28, further
comprising multiplexing means for multiplexing the
encoded code output from said selection means, and a
15 quantization coefficient associated with a quantization
step for obtaining the encoded code.

 32. An apparatus according to claim 29, wherein
said selection means comprises a circuit for
20 compensating for a time difference in said control
means.

 33. An apparatus according to claim 29, wherein
said operation means calculates a data amount, which is
25 to be obtained when the converted data quantized by
said quantization means are encoded, in units of
predetermined periods.



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34. An apparatus according to claim 29, wherein said control means updates a control state of said quantization means in units of predetermined periods.

5 35. A transform image encoder including a quantizer and in which there is provided an ordering circuit for ranking the transform coefficients in sequence of their frequency content, characterised in that the ordering circuit ranks the coefficients prior to
10 quantization thereof.

36. A discrete cosine transform encoder in which transform coefficients are quantized by a quantizer with a variable scale, characterised in that the scale
15 of the quantizer is derived using image data from preceding image frames.

37. A method of transform encoding a video signal, comprising the step of predicting a quantizer step
20 value to match a desired amount of video image data, characterised in that the prediction is performed from image data of at least one preceding frame.



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38. An adaptive transform encoder including a controllable quantizer, in which the quantizer step size is initially set equal to its value on the preceding frame, and the step size value is then
5 adjusted to adjust the amount of image data that would be generated for the current frame towards a predetermined constant amount.



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