

ABSTRACT

(Figure 4)

COMPUTER SYSTEM AND METHOD FOR MAINTAINING MEMORY
CONSISTENCY IN A PIPELINED, NON-BLOCKING CACHING
BUS REQUEST QUEUE

A computer system, and a method performed by it, having a mechanism for ensuring consistency of data among various level(s) of caching in a multi-level hierarchical memory system. The cache consistency
5 mechanism includes an external bus request queue which and associated mechanism, which cooperate to monitor and control the issuance of data requests, such as read requests and write requests, onto an external bus. The computer system includes one or more CPUs each having this consistency mechanism.