

## ACCUMULATOR CIRCUIT AND METHOD OF USE THEREOF

## Related Inventions

5       The present invention is related to the following invention which is assigned to the same assignee as the present invention:

      (1) "Computer Processor Utilizing Logarithmic Conversion and Method of Use Thereof", having Serial No.  
10   08/403,158, filed on March 13, 1995.

      The subject matter of the above-identified related invention is hereby incorporated by reference into the disclosure of this invention.

15                                   Technical Field

      The present invention relates generally to accumulators for summing numbers and, in particular, to an accumulator which is programmable to selectively sum  
20   numbers represented by input signals.

## Background of the Invention

25       An accumulator is an electronic circuit which is used to sum numerical data represented by signals. Typically, an accumulator receives two or more signals and then adds the signals together to form a sum. Accumulator circuits are used in a wide variety of applications. For instance, almost every computer ever built includes an accumulator.

30       Conventional accumulators include two different types of accumulators: serial accumulators and parallel accumulators. Both the serial and parallel accumulator provide the same basic function, that is, they both produce a sum by adding together a plurality of input signals.  
35   However, the serial and parallel accumulators differ in

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their structure and performance speed. The serial accumulator sums a sequence of input signals which are received over a period of time; whereas the parallel accumulator sums a plurality of input signal which are received simultaneously. In regard to circuit structure, the serial accumulator comprises an adder connected to a register; whereas the parallel accumulator comprises an adder tree connected to a register. The adder is a circuit which adds two signals together to produce a sum. The adder tree is a circuit which adds three or more signals together to produce a sum. The register is a memory circuit which stores the sum.

FIG. 1 shows a prior art serial accumulator circuit. The serial accumulator includes an adder 11 and a register 12. The serial accumulator receives a sequence of input signals, over time, on a first input 10. Also, the adder 11 receives a signal representing the sum stored in the register 12 on a feedback path 13. The adder 11 sums the signals received on the first input 10 and the feedback path 13 to produce a result which is then stored in the register 12. After receiving the entire sequence of input signal, the sum stored in the register 12 represent the sum of the input signals. The accumulator provides the contents of the register 12 as a signal on an output 14.

Serial accumulators suffer because they can only sum one input at a time. This negatively impacts the serial accumulator's applicability to many engineering problems. For example, in a computer the serial accumulator will seriously degrade data processing speed if it is used to sum a large number of input signals.

FIG. 2 shows a prior art parallel accumulator circuit. The parallel accumulator circuit comprises an adder tree 16 and a register 17. The adder tree 16 simultaneously receives a plurality of input signals on inputs 15 and in turn produces a sum which is then stored in register 17.

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The sum is represented by a signal on output 18. The adder tree 16 includes a plurality of adders which are connected together in a fashion which allows three or more input signals to be summed concurrently. When using the adder tree topology depicted by FIG. 2,  $N-1$  adders are required to sum  $N$  inputs. For example, as shown in FIG. 2, eight input signals can be received simultaneously, thus, seven adders are required in the adder tree. If one wishes to sum a greater number input signals, then more adders are required. For instance, in order to sum sixty-four input signals, the adder tree would require sixty-three adders.

Although parallel accumulators are much faster than serial accumulators, parallel accumulators are at a disadvantage because they require a large number of adders, and hence, a large amount of space when implemented in an integrated circuit. This fact makes parallel accumulators impractical in many engineering applications.

There is thus a need for an accumulator circuit that is capable of summing concurrent input signals without requiring a large amount of area on an integrated circuit and without incurring a large processing delay.

#### Brief Description of the Drawings

The invention is pointed out with particularity in the appended claims. However, other features of the invention will become more apparent and the invention will be best understood by referring to the following detailed description in conjunction with the accompanying drawings in which:

FIG. 1 shows a prior art serial accumulator circuit.

FIG. 2 shows a prior art parallel accumulator circuit.

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FIG. 3 illustrates a conceptual diagram of an accumulator which is in accordance with a preferred embodiment of the present invention.

5 FIG. 4 illustrates a conceptual diagram of an accumulator which is in accordance with another embodiment of the present invention.

FIG. 5 illustrates a block diagram of a preferred summing circuit utilized by various embodiments of the present invention.

10 FIG. 6 illustrates a block diagram of another summing circuit utilized by various embodiments of the present invention.

15 FIG. 7 illustrates a flow chart diagram of a method of using an accumulator, such as those depicted in FIGS. 3 and 4, in accordance with an embodiment of the present invention.

20 FIG. 8 illustrates a block diagram of a computer which incorporates the various embodiments of the present invention.

#### Detailed Description of the Preferred Embodiments

25 It is an advantage of the present invention to provide an accumulator circuit which is capable of summing a large number of input signals, and yet requires substantially less space on an integrated circuit and less time to accumulate values than a conventional accumulator  
30 performing a similar function. A further advantage of the present invention is to provide an accumulator circuit which can be easily programmed to selectively accumulate any combination of input signals from different sources. Yet another advantage of the present invention is to  
35 provide an accumulator circuit that has a reduced input capacitance.

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Generally, the present invention provides a method and accumulator for summing a plurality of input signals. The input signals may be construed as binary words representing numerical values. The accumulator itself comprises a plurality of summing circuits, a plurality of switches for regulating the transmission of data between the summing circuits, and a control unit for configuring the switches. The accumulator provided by the present invention can be more fully understood with reference to FIGS. 3-6.

FIG. 3 illustrates a conceptual diagram of an accumulator which is in accordance with a preferred embodiment of the present invention. The accumulator comprises a bus 26, a plurality of summing circuits 24a-h, a plurality of switches 32b-h, and a control unit 20 which is connected to each of the summing circuits by a control bus 22.

A significant advantage of the accumulator is that it can function as either a parallel accumulator or a plurality of serial accumulators. The actual function of the accumulator depends upon a sequence of control signals issued by the control unit 20.

The summing circuits 24a-h are adjacently coupled to the bus 26. Each of the summing circuits 24a-h has a bi-directional port 30a-h and an input port 28a-h connected to the bus 26. In addition, each summing circuit has an output port 34a-h. The summing circuits 24a-h receive a plurality of input signals on the input ports 28a-h and then sum the input signals to generate a plurality of intermediate signals. Each summing circuit 24a-h can generate an intermediate signal on either its corresponding output port 34a-h or bi-directional port 30a-h, depending on how the summing circuit is configured by the control unit 20.

The plurality of switches 32b-h are for regulating the transmission of signals on the bus 26. Each switch is

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located on the bus 26 between the input port and the bi-directional port of a respective one of the summing circuits. In addition, each of the switches 32b-h can be independently placed in either an open position or a closed position. In an open position, a switch will prevent signals from passing through to the remainder of the bus 26. In a closed position, a switch will allow signals to pass along the bus 26. For example, if an input signal is received on the input port 28c of the third summation circuit 24c while the first switch 32b is closed and the second switch 32c is open, then the input signal will be distributed across the bus 26 to the bi-directional ports 30a-b of the first and second summing circuits 24a-b and to the input ports 28b-c of the second and third summing circuits 24b-c. The position of each switch is determined by a respective control signal issued by the control unit 20 and distributed across the control bus 22. In an integrated circuit, each switch can be implemented using a MOS (metal oxide semiconductor) pass transistor.

In addition to configuring each of the switches 32b-h, the control unit 20 configures the bi-directional port 30a-h of each of the summing circuits 24a-h to either receive or transmit data. At least one control signal for independently regulating the bi-directional port of each summing circuit is provided by the control unit 20 over the control bus 22. Each summing circuit includes a transceiver, which is responsive to the control signal, for setting the data flow direction of the bi-directional port. The details of the summing circuits are further described herein with reference to FIGS. 5 and 6.

By asserting various control signals at different times, the control unit 20 routes the intermediate signals to be either transmitted as output signals on the output ports 34a-h or across the bus 26 to be received as input by another one of the of summing circuits 24a-h. For

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instance, to sum intermediate signals generated by the first summing circuit 24a and the third summing circuit 24c, the control unit 20 first issues a control signal that opens the first and fourth switches 32b,d and closes the second switch 32c. Then, the control unit 20 issues another control signal that causes the first and third summing circuits 24a,c to place their intermediate signals on their respective bi-directional ports 30a,c. The second summing circuit then receives the intermediate sum of the first summing circuit 24a on its input port 28b and the intermediate sum of the third summing circuit 24c on its bi-directional port 30b.

There are many approaches to realizing the control unit 20. In a digital system, the control unit 20 could be implemented as either a hard-wired control sequencer or a microprogrammable control unit. Generally, a hard-wired control sequencer is a sequential circuit realization of a finite state machine. A microprogrammable control unit, on the other hand, generates control signals by decoding a sequence of instructions that are stored in a memory. For instance, a microprocessor may be used to implement a microprogrammable control unit.

Although the accumulator of FIG. 3 is shown having a topology which includes eight summing circuits, one of ordinary skill in the art will realize that the accumulator may have any number of summing circuits, and yet still embody the concept and spirit of the present invention.

#### Operational Example of the Accumulator of FIG. 3

Two operational examples will be given for the accumulator: (1) parallel accumulation mode and (2) serial accumulation mode. Although only two modes of operations are presented here, many others are possible, as the

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control unit 20 can configure the accumulator to sum any combination of input signals.

The example for parallel accumulation demonstrates the accumulation of eight input signals into a single output sum. During parallel accumulation, the control unit 20 initially issues a control signal that causes all of the switches 32b-h to open. Then, input signals are received, one on each of the input ports 28a-h. During the first addition cycle, the control unit 20 issues a control signal that causes every other summing circuit to generate an intermediate sum from the input signals. In other words, the first summing circuit 24a sums the input signals received on the first pair of input ports 28a-b; the third summing circuit 24c sums the input signals received on the second pair of input ports 28c-d; the fifth summing circuit 24e sums the input signals received on the third pair of input ports 28e-f; and the seventh summing circuit 24g sums the input signals received on the fourth pair of input ports 28g-h.

Next, during the second addition cycle, the four intermediate sums are added together to generate two further intermediate sums. The intermediate sums from the first and third summing circuits 24a,c are summed by the second summing circuit 24b to generate another intermediate sum. To accomplish this, the control unit 20 issues a control signal that opens the first and third switches 32b,d and closes the second switch 32c. The control unit 20 then causes the first and third summing circuits 24a,c to transmit their intermediate sums on their respective bi-directional ports 30a,c. Near this time, the control unit 20 also issues a control signal to cause the second summing circuit to receive signals on its bi-directional port 30b.

A like procedure as described above for the second addition cycle is also performed to sum the intermediate sums produced by the fifth and seventh summing circuits

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24e,g. In this case, the control unit 20 opens the fifth switch 32f and closes the sixth switch 32g. The intermediate sums from the fifth and seventh summing circuits 24e,g are then transmitted across the bus 26 to the input port 28f and the bi-directional port 30f, respectively, of the sixth summing circuit 24f. As a result, the sixth summing circuit 34f generates a further intermediate sum.

During the third addition cycle, the intermediate sums generated by the second and sixth summing circuits 24b,f are summed to produce a final output sum. The control unit 20 asserts a control signal which opens the second switch 32c and closes the third, fourth, and fifth switches 32d-f. The control unit 20 then causes the intermediate sums of the second and sixth summing circuit 24b,f to be transferred across the bus 26 to the input port 28c and the bi-directional port 30c, respectively, of the third summing circuit 24c. The third summing circuit 34c sums these values and provides the result on its output port 34c. The value on the output port 34c is the final output sum generated by the accumulator.

When a summing circuit is inactive, i.e., it is not being used during an addition cycle, it's bi-directional port is held in a high impedance state, and further, it does not otherwise respond to signals traveling along the bus 26.

The example for serial accumulation demonstrates the accumulation of eight sequences of input signals into eight separate output sums. During serial accumulation, the control unit 20 initially issues a control signal that causes all switches 32b-h to remain open and all bi-directional ports 30a-h to assume a high impedance state. The sequences of input signals are received, one on each of the input ports 28a-h. Over time, each summing circuit sums it's respective input sequence to generate an output

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sum on it's corresponding output port 34a-h. These output sums form the output of the accumulator.

FIG. 4 illustrates a conceptual diagram of an accumulator which is accordance with another embodiment of the present invention. The advantage of this version of the accumulator is that it can function as a parallel accumulator, but with significantly fewer adders than a conventional parallel accumulator. In the example shown in FIG. 4, the accumulator requires only four adders (one in each of the summing circuits 54a-d) to accumulate eight input signals; whereas, a conventional parallel accumulator would require seven adders for a like number of inputs. The accumulator can also function as a plurality of serial accumulators or a plurality of two-input adders.

The accumulator comprises a control unit 21, a plurality of switches 60a-b, a first center switch 62, a second center switch 64, and a plurality of summing circuits 54a-d. The summing circuits 54a-d are adjacently arranged into a first symmetrical group 50 and a second symmetrical group 52. Each of the symmetrical groups has a respective center summing circuit 54b-c.

In a diagrammatic sense, the symmetrical groups are mirror-images of one another. The first symmetrical groups includes a first center summing circuit 54b, while the second symmetrical group 52 includes a second center summing circuit 54c. The center summing circuits 54b-c are distinguished from others because they have their bi-directional ports 58b-c connected with the first center switch 62.

Each of the summing circuits 54a-d has an input port 56a-d and a bi-directional port 58a-d. In addition, each summing circuit has an output port 52a-d. The summing circuits 54a-d receive a plurality of input signals on both the input ports 56a-d and the bi-directional ports 58a-d and then sum the input signals to generate a plurality of

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intermediate signals. Each summing circuit 54a-d can generate an intermediate signal on either its corresponding output port 52a-d or bi-directional port 58a-d, depending on how the summing circuit is configured by the control unit 21.

The plurality of switches 60a-b are for regulating the transmission of signals between summing circuits within the same symmetrical group. Each of the plurality of switches 60a-b is connected between the bi-directional port and the input port of an adjacent summing circuits within a symmetrical group.

The first center switch 62 connects the bi-directional ports 58b-c of the center summing circuits 52b-c. The first center 62 switch allows intermediate signals to pass between the center summing circuits 54b-c.

The second center switch 64 can be located between the bi-directional and output ports of either the first or second center summing circuit. In the example shown, the second center switch 64 is connected between the bi-directional port 58c and the input port 56c of the second center summing circuit 54c. The purpose of the second center switch 64 is to allow intermediate signals produced on the bi-directional port 58b of the first center summing circuit 54b to reach the input port 56c of the second center summing circuit 54c.

Each of the switches can be independently placed in either an open position or a closed position. In an open position, a switch will prevent a signal from passing. In a closed position, a switch will allow a signal to pass. The position of each switch is determined by a respective control signal issued by the control unit 21 and distributed across the control bus 23. In an integrated circuit, each switch can be implemented using a MOS (metal oxide semiconductor) pass transistor.

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In addition to configuring each of the switches, the control unit 21 configures the bi-directional port 58a-d of each of the summing circuits 54a-d to either receive or transmit signals. At least one control signal for  
5 independently regulating the bi-directional port of each summing circuit is provided by the control unit 21 over the control bus 23. Each summing circuit includes a transceiver, which is responsive to the control signal, for setting the data flow direction of the bi-directional  
10 port. The details of the summing circuits are further described herein with reference to FIGS. 5 and 6.

By asserting various control signals at different times, the control unit 21 routes the intermediate signals to be either transmitted as output signals on the output  
15 ports 52a-d or to other summing circuits 54a-d. For instance, to sum intermediate signals generated by the first summing circuit 54a and the first center summing circuit 54b, the control unit 21 first issues a control signal that opens the first center switch 62 and closes the  
20 switch 60a between the two summing circuits 54a-b. Then, the control unit 21 issues another control signal that causes the first summing circuit 54a to generate its intermediate signal on its bi-directional port 58a. The first center summing circuit 54b then receives the  
25 intermediate sum on its input port 56b and adds it to its own intermediate sum. The resultant sum generated by the first center summing circuit 54b can be output on either the bi-directional port 58b or the output port 52b.

In a digital system, the control unit 21 could be  
30 implemented as either a hard-wired control sequencer or a microprogrammable control unit.

Although the accumulator of FIG. 4 is shown having a topology which includes four summing circuits, one of ordinary skill in the art will realize that the accumulator

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may be have any number of summing circuits, and yet still embody the concept and spirit of the present invention.

FIG. 5 illustrates a conceptual diagram of a preferred summing circuit 70 utilized by various embodiments of the present invention. The summing circuit 70 comprises an adder 76, a register 72, and a transceiver 74. The adder 76 has an input 71 connected to the input port 73 of the summing circuit 70 and another input 78 connected to the transceiver 74 and register 72. In response to receiving signals on its inputs, the adder 76 generates a sum, represented by an intermediate signal, which is provided to the register 72 and the output port 86. The register 72 stores and then provides the intermediate sum to the adder input 78 or the transceiver 74 at a later time. The register 72 performs its function according to control signals received on a control bus 77. The transceiver 74 either receives signals from the bi-directional port 75 or transmits the intermediate sum stored in the register 72 on the bi-directional port 75. Control signals received on the control bus 77 determine the action of the transceiver 74. In order to avoid indeterminate signals on the adder input 78, the register 72 and the transceiver 74 can have their respective outputs placed in a high-impedance state. In addition, the transceiver 74 can place its connection to the bi-directional port 75 in a high-impedance state.

FIG. 6 illustrates a conceptual diagram of another summing circuit utilized by various embodiments of the present invention. The summing circuit 80 comprises an adder 76, a multiplexer 90, a register 92, and a transceiver 94. The adder 76 has an input 71 connected to the input port 73 of the summing circuit 80 and another input 78 connected to the multiplexer 90. In response to receiving signals on its inputs, the adder 76 generates an intermediate sum, represented by an intermediate signal, which is provided to the register 92 and the output port

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86. The register 92 stores and then provides the intermediate sum to the multiplexer 90 or the transceiver 94 at a later time. The transceiver 94 either receives signals from the bi-directional port 75 or transmits the intermediate sum stored in the register 92 to the bi-directional port 75. In addition, the transceiver 94 can place its connection to the bi-directional port 75 in a high-impedance state. Control signals received on the control bus 77 determine the action of the transceiver 94. The multiplexer 90 selectively provides either the register 92 output or the input signals from the bi-directional port 75 to the adder input 78. The output of the multiplexer 90 is selected by a control signal received on the control bus 77.

FIG. 7 illustrates a flow chart diagram of a method of using an accumulator, such as those depicted in FIGS. 1 and 2, in accordance with an embodiment of the present invention. In box 100, a plurality of input signals are distributed to the plurality of summing circuits. Next, in box 102, the summing circuits add together the input signals to produce a plurality of intermediate sums.

In box 104, a routing path is determined for each of the intermediate sums. The routing path indicates the flow of an intermediate signal, which represents the intermediate sum, through the accumulator. When combined together, the routing paths form a control sequence, which when executed by the control unit causes the accumulator to add together various ones of the intermediate sums to generate an output sum. The control unit can be programmed with routing path information to enable, at predetermined times, selected ones of the summing circuits and the switches. As a result of executing the control sequence, the control unit generates control signals which enable the switches and summing circuits so that the intermediate sums are accumulated as desired. Box 106 depicts the routing of

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at least one of the intermediate sums to an input of one of the summing circuits. The intermediate sums are routed by first enabling selected ones of the summing circuits to transmit, at specific times, an intermediate sum on their bi-directional port. Then, by setting the switches, the intermediate sums are transmitted to at least one other summing circuit. In box 108, the summing circuits sum signals received their inputs to produce an output signal which represents an output sum.

10 In reference to box 100, when the input signals are received on a common bus, such as in the accumulator depicted in FIG. 1, they are first matched to a corresponding summing circuit and then the switches are set accordingly so that the inputs remain isolated on different portions of the bus.

In reference to box 104, the control sequence is determined as follows. First, input signals to be included in the output sum are selected. Next, the summing circuits that produce intermediate sums from the input signals are designated. Then, final summing circuits which produce the output signals are designated. In the preferred embodiment of the present invention, the final summing circuits are selected so that the intermediate sums are transferable across a bus which connects the plurality of summing circuits. Finally, the times at which various switches and summing circuits are to be enabled are determined. The control sequence can be implemented using either microcode or a digital logic circuit.

FIG. 8 illustrates a conceptual diagram of a computer which incorporates an embodiment of the present invention. The computer can generate at least one output sum on its output bus 140. The computer comprises a plurality of processors 120 and an accumulator 150. The accumulator 150 comprises a plurality of adder groups 122a-d, a secondary adder 124, a final summing circuit 126, a control unit 127,

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and a multiplexer 128. Although the plurality of processors may include any number of processors, they are represented by the sixteen depicted in FIG. 8. As a result of performing computations, the processors 120 generate a plurality of numerical values, which are represented by data signals. The adder groups 120a-d, in turn, sum the data signals to produce a plurality of primary sums, represented by primary signals. These primary signals are provided as input to both the secondary adder 124 and the multiplexer 128. Each adder group has a plurality of output ports; and although an adder group may have any number of output ports, in the example shown each adder group has four output ports. All of the output ports are connected to the multiplexer 128, while only one output port from each adder group is connected to the secondary adder 124. The secondary adder sums primary signals from each of the adder groups 122a-d to generate at least one secondary sum. The secondary sums are then provided to the final summing circuit 126 and the multiplexer 128. The final summing circuit 126 sums, over time, a sequence of secondary sums to produce a final sum. The final sum is provided to the multiplexer 128. The control unit 127 provides control signals to the adder groups 122a-d, the secondary adder 124, the final summing circuit 126, and the multiplexer 128 over a control bus 123. By issuing various control signals at different times, the control unit 127 can route, at a minimum, at least one secondary sum to the output bus 140 and configure each of the adder groups 122a-d to generate the at least one primary sum.

In one version of the computer, each of the adder groups 122a-d includes an accumulator based on the accumulator described herein with reference to FIG. 3. Because there are only sixteen processors depicted in FIG. 8, the accumulator shown in FIG. 3 would require only four summing circuits to be operable in one of the adder groups.

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122a-d. Using the accumulator of FIG. 3 as shown, having a total of eight summing circuits, would allow the computer to incorporate thirty-two processors rather than sixteen.

In the same version of the computer, the secondary adder 124 includes an accumulator based on the accumulator described herein with reference to FIG. 4. To be operable in the secondary adder 124, the accumulator shown in FIG. 4 would require only two summing circuits. The final summing circuit 126 includes a serial accumulator as described herein with reference to FIG. 1.

The multiplexer 128 selects outputs from the adder groups 122a-d, secondary adder 124 or final summing circuit 126 to be provided on the computer output bus 140. The signals presented on the computer output bus 140 are determined according to a control sequence which is executed by the control unit 127.

The control unit 127 can configure the computer to accumulate any combination of the processors' 120 outputs. For example, the computer can be configured to individually accumulate the outputs of each of the processors 120 to generate a plurality of individual processor sums. These sums can then be sequentially provided on the computer output bus 140. This is accomplished by setting the adder groups 122a-d to function as a plurality of serial accumulators. The multiplexer 128 then sequential selects each of output of the adder groups 122a-d to be provided on the computer output 140. Another possible configuration allows all outputs of the processors 120 to be accumulated, over a period of time, into a single sum. This can be accomplished by the adder groups 122a-d summing the their respective inputs to generate primary sums. The primary sums are then summed by the secondary adder 124 to produce a secondary sum which represents the total of the processor outputs for a given addition cycle. The secondary sums for a plurality of addition cycle can then be accumulated, over

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time, by the final summing circuit 126 to generate the single sum. The output of the final summing circuit 126 is selected by the multiplexer to be provided on the computer output bus 140.

5        Thus, in summary, there has been described herein a concept, as well as several embodiments, including a preferred embodiment, of an accumulator which utilizes a plurality of switches and summing circuits to add input signals, thus allowing the accumulator to sum inputs at  
10        dramatically greater speeds while reducing the size and complexity of the accumulator in an integrated circuit.

      Because the various embodiments of the present invention provide an accumulator circuit which includes a control unit, they can be easily programmed to selectively  
15        accumulate any combination of input signals from different sources. Additionally, because the various embodiments of the present invention provide a plurality of switches which can be open to isolate input signals, these embodiments enjoy a reduced input capacitance.

20        While specific embodiments of the present invention have been shown and described, it will be apparent to those skilled in the art that the disclosed invention may be modified in numerous ways and may assume many embodiments other than the preferred form specifically set out and  
25        described above.

      Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

30        What is claimed is:



## CLAIMS

1. An accumulator, which comprises:
  - 5 a plurality of summing circuits for generating a plurality of intermediate signals, each of the plurality of summing circuits having a port for transferring signals;
  - a plurality of switches, connected between ports of the plurality of summing circuits, for regulating
  - 10 transmission of the signals, each of the plurality of switches having an open position and a closed position; and
  - a control unit for configuring each of the plurality of switches in either the open position or the closed position and for configuring the port of each of the
  - 15 plurality of summing circuits to either receive or transmit data;
- wherein a plurality of input signals is summable by the plurality of summing circuits to generate the plurality of intermediate signals, and the control unit routes ones
- 20 of the plurality of intermediate signals to be transmitted as output signals or to at least one of the plurality of summing circuits by configuring the plurality of switches and the port of each of the plurality of summing circuits.



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2. The accumulator of claim 1, wherein each of the plurality of summing circuits includes a bi-directional port and an input port.

5        3. The accumulator of claim 2, wherein each of the plurality of summing circuits comprises:

an adder for generating an intermediate signal, the adder having a first input responsive to the input port and a second input;

10       a register for storing the intermediate signal and providing the intermediate signal as a register output thereof;

15       a transceiver for receiving input data from the bi-directional port and transmitting the register output to the bi-directional port; and

a multiplexer for selectively providing either the register output or the input data to the second input of the adder.

20       4. The accumulator of claim 1, wherein each of the summing circuits includes an output port for transmitting at least one output signal.

25       5. The accumulator of claim 1, wherein the control unit is programmable to configure selected ones of the summing circuits and selected ones of the switches at predetermined times.



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6. An accumulator, which comprises:

a bus;

a plurality of summing circuits, adjacently coupled to the bus, for generating a plurality of intermediate

5 signals, each of the plurality of summing circuits having a bi-directional port and an input port connected to the bus;

a plurality of switches for regulating the transmission of data on the bus, each of the plurality of switches having an open position and a closed position and  
10 being located on the bus between the input port and the bi-directional port of a corresponding one of the plurality of summing circuits; and

a control unit for configuring each of the plurality of switches in either the open position or the closed  
15 position and for configuring the bi-directional port of each of the plurality of summing circuits to either receive or transmit data;

wherein a plurality of input signals is summable by the plurality of summing circuits to generate the plurality  
20 of intermediate signals, and the control unit routes ones of the plurality of intermediate signals to be either transmitted as output signals or across the bus to at least one of the plurality of summing circuits by configuring the plurality of switches and the bi-directional port of each  
25 of the plurality of summing circuits.



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7. An accumulator, which comprises:

a plurality of summing circuits adjacently arranged into two symmetrical groups, each of the symmetrical groups having a center summing circuit, and each summing circuit  
5 generating an intermediate signal and having an input port and a bi-directional port;

a first center switch connecting the bi-directional port of the center summing circuit of each group;

a second center switch connected between the bi-  
10 directional port and the input port of one of the center summing circuits;

a plurality of switches, each of the plurality of switches connected between the bi-directional port and the input port of adjacent summing circuits; and

15 a control unit for configuring each of the plurality of switches, the first center switch, and the second center switch in either an open position or a closed position and for configuring the bi-directional port of each of the plurality of summing circuits to either receive or transmit  
20 data;

wherein a plurality of input signals is summable by the plurality of summing circuits to generate a plurality of intermediate signals, and the control unit routes ones of the plurality of intermediate signals to be either  
25 transmitted as output signals or to at least one other of the plurality of summing circuits by configuring the plurality of switches, the first center switch, the second center switch, and the bi-directional port of each of the plurality of summing circuits.

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8. An accumulator having an output bus, which comprises:

a plurality of adder groups for generating a plurality of primary sums in response to a plurality of input

5 signals;

a secondary adder, responsive to at least one primary sum from each of the plurality of adder groups, for generating at least one secondary sum; and

10 a control unit for routing the at least one secondary sum to the output bus and for configuring each of the plurality of adder groups to generate the at least one primary sum.



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9. A computer having an output bus, which comprises:  
a plurality of processors for generating a plurality  
of data signals as a result of performing computations;  
a plurality of adder groups, operatively coupled to  
5 the plurality of processors, for summing the plurality of  
data signals to produce a plurality of primary sums;  
a secondary adder, responsive to at least one primary  
sum from each of the plurality of adder groups, for  
generating at least one secondary sum; and  
10 a control unit for routing the at least one secondary  
sum to the output bus and for configuring each of the  
plurality of adder groups to generate the at least one  
primary sum.



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10. In an accumulator which includes a plurality of summing circuits, a method for producing an output signal which represents a sum, which method comprises the steps of:

5        distributing a plurality of input signals to the plurality of summing circuits;

         the plurality of summing circuits summing the plurality of input signals to produce a plurality of intermediate signals;

10       generating a plurality of control signals in order to route at least one of the plurality of intermediate signals to a designated summing circuit; and

         summing signals received by the designated summing circuit to produce the output signal.

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