

# PATENT SPECIFICATION

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DRAWINGS ATTACHED



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## (54) TELEVISION DEFLECTION CIRCUIT

(71) We, RCA CORPORATION, formerly Radio Corporation of America, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electromagnetic cathode ray beam deflection circuits of the type employed in television receivers and, in particular, to transistor vertical deflection circuits including apparatus for substantially improving the vertical linearity of the scanning raster produced on an associated cathode ray tube.

One type of transistor vertical deflection circuit utilizes the principles of the "Miller Integrator" to generate a substantially sawtooth shaped current for application to the vertical deflection winding associated with a cathode ray tube. In such circuits, the vertical deflection winding is traversed by a desired current waveform in response to the generation of a sawtooth voltage waveform across a capacitor, the capacitor being coupled in a negative feedback path associated with a high gain transistor amplifier. A switching device is coupled in circuit with and is utilized to discharge the capacitor at a predetermined time in the deflection cycle to initiate the retrace portion of such cycle. The deflection circuit may be rendered self-oscillating by supplying to the switching device a retrace voltage pulse which is developed when the current supplied to the vertical deflection windings is decreased. The deflection cycles are synchronized by means of vertical synchronizing signals received by the television receiver along with the image representative information.

In such circuits, a finite voltage is required to initiate conduction in the amplifier and thereby to commence production of the

desired sawtooth deflection waveform across the deflection windings. In the absence of means for providing such a voltage immediately at the beginning of vertical trace, the image produced upon the cathode ray tube is noticeably and undesirably cramped at the top.

It has therefore previously been proposed to provide sawtooth waveform generating circuits of the "Miller Integrator" type including passive feedback means for linearising the sawtooth waveform produced and also for producing a rapid turn-on of the circuit at the beginning of the stroke.

Furthermore, the "Miller Integrator" provides an essentially linear output waveform which must be modified when utilized in connection with a cathode ray tube having a wide deflection angle (i.e. "S"-shaping of the deflection waveform is required to produce a linear vertical raster).

In accordance with the present invention there is provided a television vertical deflection circuit including a transistor amplifier arranged during trace portions of the vertical deflection cycle to cause current to flow in vertical deflection windings coupled to the amplifier output, a capacitor coupled to the amplifier input and arranged to be charged from a primary current supply during trace portions of the deflection cycle and to be discharged by way of switching means which is rendered operative during retrace portions of the deflection cycle, wherein an auxiliary transistor has its emitter-collector path arranged in a rapid charging path for said capacitor, said auxiliary transistor being arranged to be conductive to supply charge to said capacitor during an interval between the time when said switching means is rendered inoperative and the time when said transistor amplifier causes trace current to flow.

A preferred embodiment of the invention will now be described in conjunction with the accompanying drawing.

In the drawing, the circuits of a tele-

vision receiver serving to provide signals for energizing an image reproducing device such as a kinescope 10 are represented by a single block 12 labelled "Television Signal Receiver". The receiver unit 12 incorporates the usual elements required to provide video signals at output terminal L for appropriate intensity modulation of the electron beam of kinescope 10, as well as to provide suitable synchronizing pulse information at terminals P<sub>1</sub> and P<sub>2</sub> to synchronize, in respective horizontal and vertical deflection circuits 14 and 16, the energization of the respective horizontal and vertical windings 18 and 20 of a deflection yoke associated with kinescope 10.

In the vertical deflection circuit shown in the drawing, a sawtooth current waveform is caused to pass through the vertical deflection windings 20 of the deflection yoke, the windings 20 being coupled in series with a current sampling resistor 22 across the secondary winding 24b of a vertical deflection output transformer 24. The flow of the desired sawtooth current waveform in the winding 20, which appear essentially resistive during the relatively low frequency trace portion of the television vertical deflection cycle, is produced in response to the development during trace of a sawtooth voltage waveform across the primary winding 24a of output transformer 24. As will be noted below, during the relatively rapid (higher frequency) retrace portion of the vertical cycle, the deflection windings 20 are substantially inductive and the retrace voltage waveform across windings 20 is an approximately triangular pulse. The development of the composite recurring pulse-sawtooth voltage waveform across transformer 24 is accomplished in the illustrated embodiment of the invention through use of a transistorized arrangement employing principles of the "Miller Integrator".

The integrator comprises transistors 26, 28 and 30 which are cascaded to form a high gain amplifier. Negative feedback is established between the amplifier output and amplifier input via a path incorporating a capacitor 32.

Amplifier 26 comprises a N-P-N transistor having a base electrode 26b, a collector electrode 26c and an emitter electrode 26e. The emitter electrode 26e of amplifier 26 is connected to ground potential while the collector electrode 26c is supplied with operating potential from the B+ voltage supply via a resistor 34. The collector electrode 26c is directly connected to the base electrode 28b of amplifier 28 (a P-N-P transistor). The collector electrode 28c of amplifier 28 is coupled to ground by means of a collector load resistor 36 while the emitter electrode 28e is coupled to the junction of resistors 38 and 40 which form a voltage

divider across the B+ voltage supply. The collector electrode 28c is directly coupled to the base electrode 30b of output amplifier 30 (an N-P-N transistor). The emitter electrode 30e of amplifier 30 is coupled to ground by means of a relatively small "starting" resistor 42 while operating voltage is supplied from the B+ supply to collector electrode 30c by means of primary winding 24a and a de-coupling network comprising resistor 44 and capacitor 46.

Capacitor 32 is subject to alternate charging and discharging to produce the desired recurring sawtooth waveform, the main charging occurring during trace via a path comprising the B+ voltage supply (e.g. +65 volts), a resistor 48, a variable resistor height control 50 and current sampling resistor 22, and the discharging occurring during retrace via a vertical oscillator stage 52 and sampling resistor 22. The charging supply may be compensated for changes in image brightness by coupling the junction of resistors 48 and 50 to the brightness control (not shown) provided in the receiver. Furthermore, a stabilized voltage supply comprising the series combination of a resistor 72 and a zener diode 74 coupled across a low voltage source (e.g. +18 volts) is coupled to the junction of resistors 48 and 50 by means of a resistor 76 to prevent image sizes changes in the event the B+ supply voltage is subject to variations.

In accordance with one aspect of the present invention, an auxiliary means for charging capacitor 32 before the commencement of vertical trace comprises a transistor 54 having a base electrode 54b, a collector electrode 54c and an emitter electrode 54e, the emitter 54e and collector 54c being coupled by means of the resistors 34 and 22 in circuit with the B+ voltage supply and the capacitor 32. The voltage divider comprising resistors 40 and 38 provides a bias voltage for the base electrode 54b of transistor 54 and, at the same time, provides the supply voltage for the emitter electrode 28e of amplifier 28.

Furthermore, an S-shaping network comprising a resistor 80, a clipping diode 56, a first R-C integrator 58, a second R-C integrator 60 and a coupling resistor 62 is coupled between deflection winding 20 and the input (base electrode 26b) of amplifier 26.

Three additional feedback paths are provided between output amplifier 30 and oscillator 52 to render the deflection circuit self-oscillating. Specifically, an integrating network 66 is coupled between deflection winding 20 and base electrode 52b by means of a capacitor 70 to provide a trigger impulse to base electrode 52b of oscillator 52 periodically to turn oscillator 52 on to initiate retrace and off to permit the occurrence

of trace. A feedback winding 24c associated with output transformer 24 is coupled via a variable resistor hold control 64 to base electrode 52b to provide, in conjunction with the capacitor 70, a waveform to increase the rate at which the input to base 52b changes near the end of trace, thereby improving the frequency stability and noise immunity of the system. Finally, the voltage produced across resistor 42 (approximately 1 ohm) is coupled via winding 24c and hold control 64 to the base electrode 52b to provide feedback to insure initiation of oscillation when the receiver is first turned on.

The operation of oscillator stage 52 is synchronized with respect to the image-representative portions of the received television signal by means of vertical synchronizing pulses applied from terminal P<sub>2</sub> via resistor 68 and capacitor 70 to base 52b.

A stabilized base bias voltage is provided for oscillator stage 52 from zener diode 74 by means of a resistor 78.

The operation of the vertical deflection circuit now will be described. Vertical oscillator stage 52 is operated on a recurrent basis alternately to alternately charge capacitor 32 from a substantially constant current charging supply and to discharge it.

During the trace portion of each vertical deflection cycle, oscillator stage 52 and transistor 54 are maintained in a nonconductive state while the transistors 26, 28 and 30 in the high gain amplifier are all biased for conduction. A charging circuit for capacitor 32 is established between the B+ terminal (or, more specifically between the compensating supply point at the junction of resistor 48 and height control 50) and ground. The charging circuit comprises the series combination of height control 50, capacitor 32 and current sampling resistor 22 (neglecting the windings 20 and 24b in parallel with resistor 22). The charging circuit provides a substantially constant current at the junction of capacitor 32 and base electrode 26b. That is, the voltage at the junction of resistor 48 and height control 50 remains substantially constant by virtue of the operation of zener diode 74 and the voltage at the base 26b of transistor 26 remains substantially constant (e.g. 0.7 volt) while transistor 26 is conductive. The resultant constant voltage across height control 50 provides the desired constant charging current for producing a linearly increasing voltage during traces across capacitor 32. At the same time, the current sampling resistor 22 provides a reference voltage across capacitor 32, which voltage is representative of the current in deflection windings 20. Neglecting for the moment the S-shaping network 54-62, if the voltage across resistor 22 (and the current in windings 20) varies linearly, the constant current

supply (height control 50) provides the necessary constant current to permit the voltage across capacitor 32 to increase linearly and thereby follow the voltage across resistor 22. However, if the current in windings 20 varies from the desired linear waveform and the voltage across resistor 22 varies in a like manner, the current required for capacitor 32 to follow the voltage across resistor 22 will change. Since a substantially constant current is supplied to the junction of capacitor 32 and base 26b, the difference in the current demanded by capacitor 32 will be supplied to the base electrode 26b of transistor 26. This relatively small "error" current then will be amplified in transistors 26, 28 and 30 to provide the required correction to the current supplied to windings 20 to maintain a linear trace current waveform. The gain (amplification) provided by transistors 26, 28 and 30 is selected sufficiently high so that a relatively small variation from the desired output waveform will produce the necessary correction.

The characteristic of the Miller integrator whereby only a very small variation at the amplifier input is required to effect a significant change at the output is applied advantageously in the operation of the S-shaping network. Specifically, an essentially parabolic current waveform is supplied to the input (base electrode 26b) of the high gain amplifier by means of the components 54-62 to modify the linear current waveform in deflection windings 20. In practice, therefore, the voltage across resistor 22 is S-shaped rather than linear where a wide deflection angle kinescope 10 is employed. The required parabolic current waveform is derived by double integration (in networks 58 and 60) of a portion of the voltage waveform appearing across transformer winding 24b. That waveform, which is made up of an S-shaped trace portion and a relatively large triangular pulse retrace portion, if passed through the networks 58 and 60 would not, because of the presence of the retrace pulse, produce the desired "parabolic" waveform. Therefore, the clipping diode 56 is provided to remove a substantial portion of the undesired retrace pulse.

Near the end of the trace portion of each deflection cycle, the voltage at the base 52b of oscillator stage 52 approaches the required turn-on level. The retrace portion of each deflection cycle is initiated when a vertical synchronizing pulse is applied to oscillator stage 52 to drive stage 52 into conduction. The base 26b of transistor 26 then is driven below the voltage required to maintain conduction in transistor 26 and all of the transistors 26, 28 and 30 are driven to cutoff. The current in deflection windings 20 then begins to decrease and, at the same time, a voltage pulse is produced

across windings 20 as was mentioned above. When oscillator stage 52 conducts, a discharging circuit is completed for capacitor 32 comprising, in series, oscillator stage 52, capacitor 32 and resistor 22. Furthermore, as transistor 26 is driven to cutoff, transistor 54 is driven into conduction and, initially, the emitter-collector current thereof passes through oscillator stage 52. Capacitor 32 discharges relatively rapidly through oscillator stage 52 essentially to zero voltage. The peak voltage pulse produced across deflection windings 20 begins to decline and, at a somewhat later instant determined by the time constant of integrator network 66, the voltage applied to base 52b also declines. Oscillator stage 52 is then driven towards cutoff. At that time, transistor 54, the current from which previously had been passing through oscillator stage 52, supplies charging current to capacitor 32. Capacitor 32 is charged rapidly by this current to a voltage of a polarity to initiate conduction in transistor 26. When the base-emitter voltage of transistor 26 reaches the nominal turn-on voltage (e.g. +0.7 volt), the transistors 26, 28 and 30 all are driven into conduction whereupon transistor 54 is driven to cutoff. The next track cycle then commences.

It should be noted that while it is common practice in television receiver design to provide an adjustable vertical linearity control in a vertical deflection circuit, in the illustrated embodiment of the invention there is no need for such a control. The basic Miller integrator enhanced by the auxiliary charging circuit constructed in accordance with the present invention provides an exceptionally linear deflection.

#### WHAT WE CLAIM IS:—

1. A television vertical deflection circuit including a transistor amplifier arranged during trace portions of the vertical deflection cycle to cause current to flow in vertical deflection windings coupled to the amplifier output, a capacitor coupled to the amplifier input and arranged to be charged from a primary

current supply during trace portions of the deflection cycle and to be discharged by way of switching means which is rendered operative during retrace portions of the deflection cycle, wherein an auxiliary transistor has its emitter-collector path arranged in a rapid charging path for said capacitor, said auxiliary transistor being arranged to be conductive to supply charge to said capacitor during an interval between the time when said switching means is rendered inoperative and the time when said transistor amplifier causes trace current to flow.

2. A vertical deflection circuit according to claim 1 wherein said transistor amplifier comprises at least a first amplifying transistor requiring a predetermined input voltage to initiate conduction therein, and wherein said auxiliary transistor provides sufficient current to charge said capacitor sufficiently to provide said predetermined input voltage at the commencement of the trace portion of each vertical deflection cycle.

3. A vertical deflection circuit according to claim 1, wherein said transistor amplifier comprises at least two amplifying transistors connected in cascade, input signals being applied to the base of the first of said two amplifying transistors, and the collector of said first amplifying transistor being connected to the base of said second amplifying transistor, the emitter of said second amplifying transistor being connected to a point on a voltage divider connected between said primary current supply and a point of reference potential and the base electrode of said auxiliary transistor being connected to the emitter electrode of said second amplifying transistor.

4. A vertical deflection circuit for a television receiver substantially as described with reference to the accompanying drawing.

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