

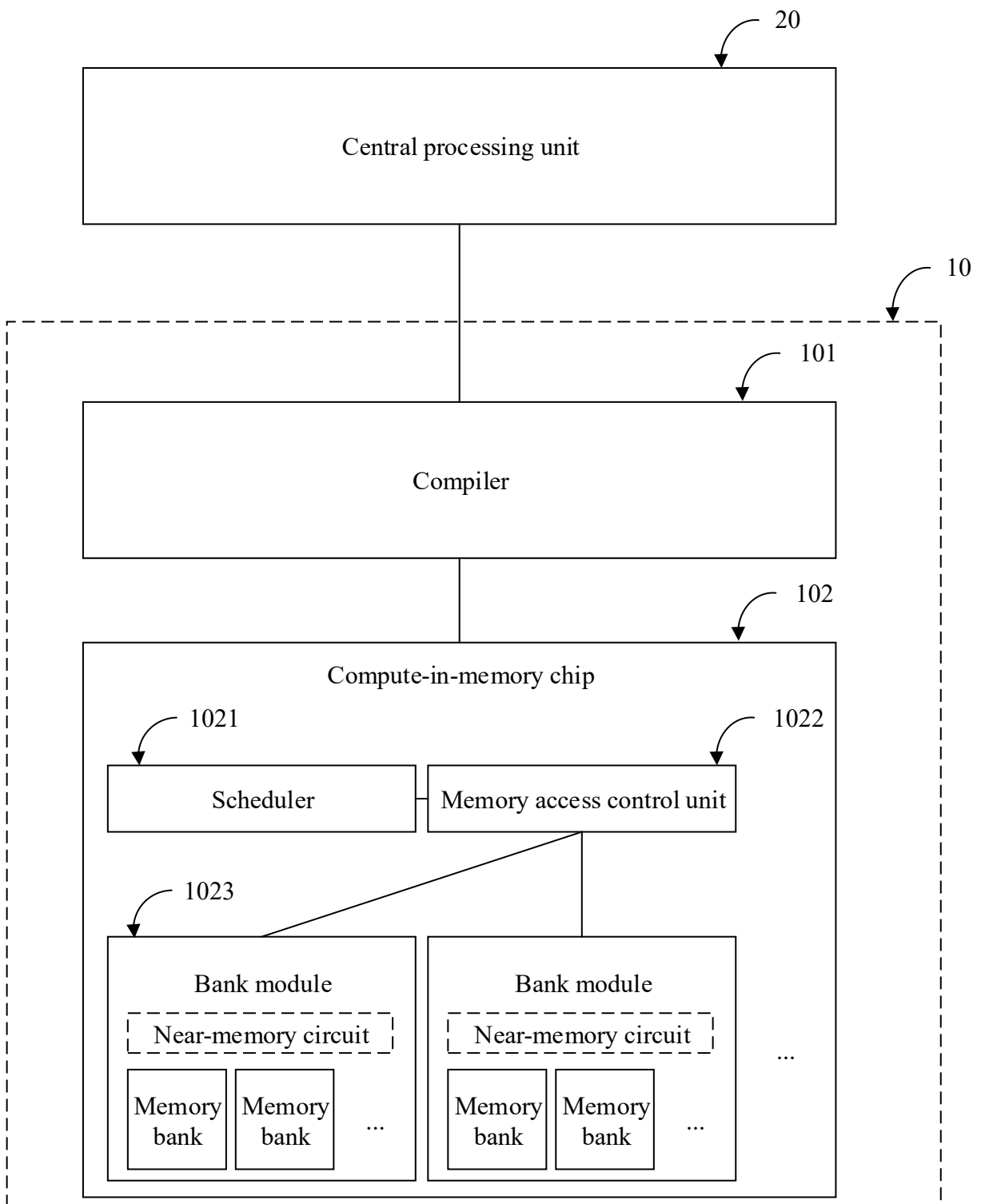


FIG. 1

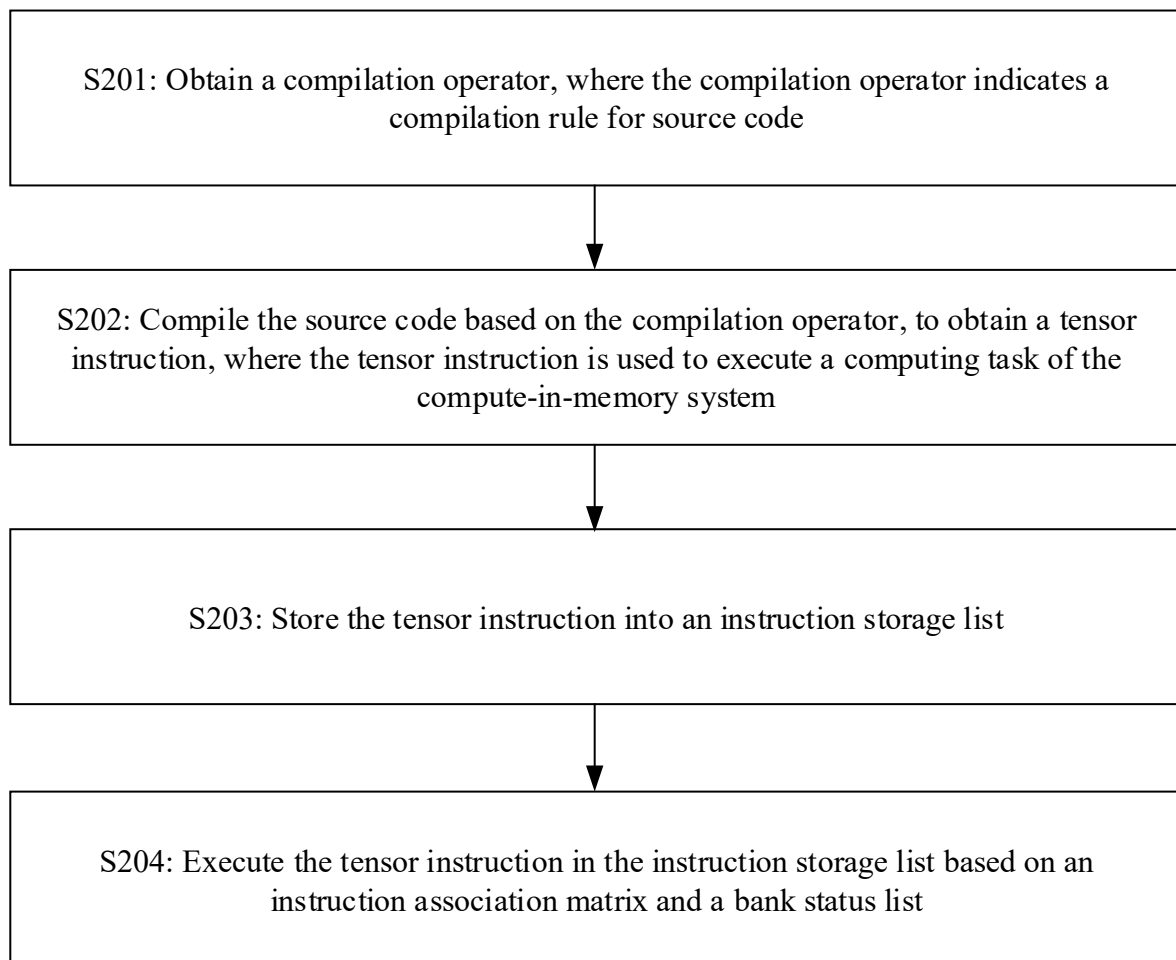


FIG. 2

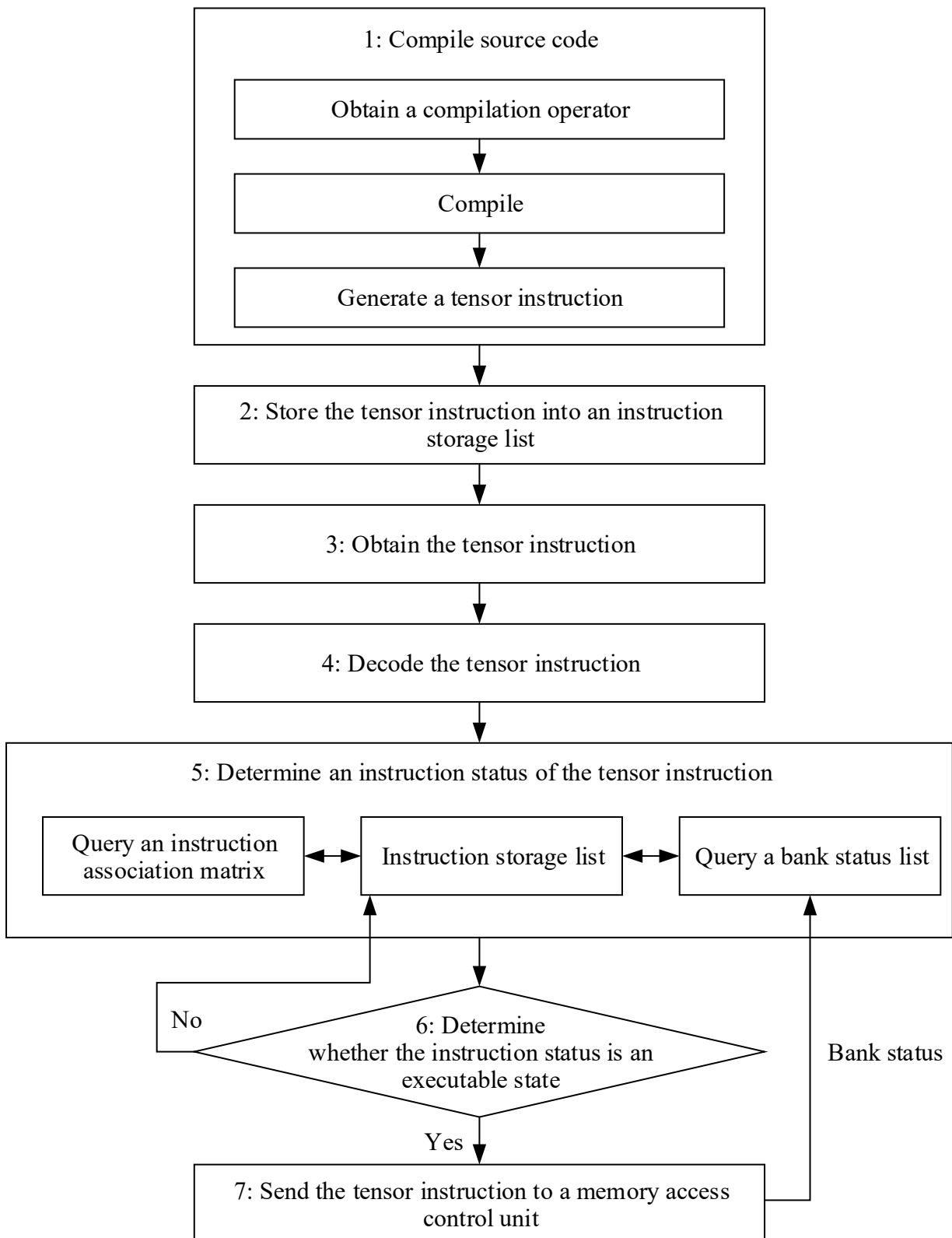


FIG. 3

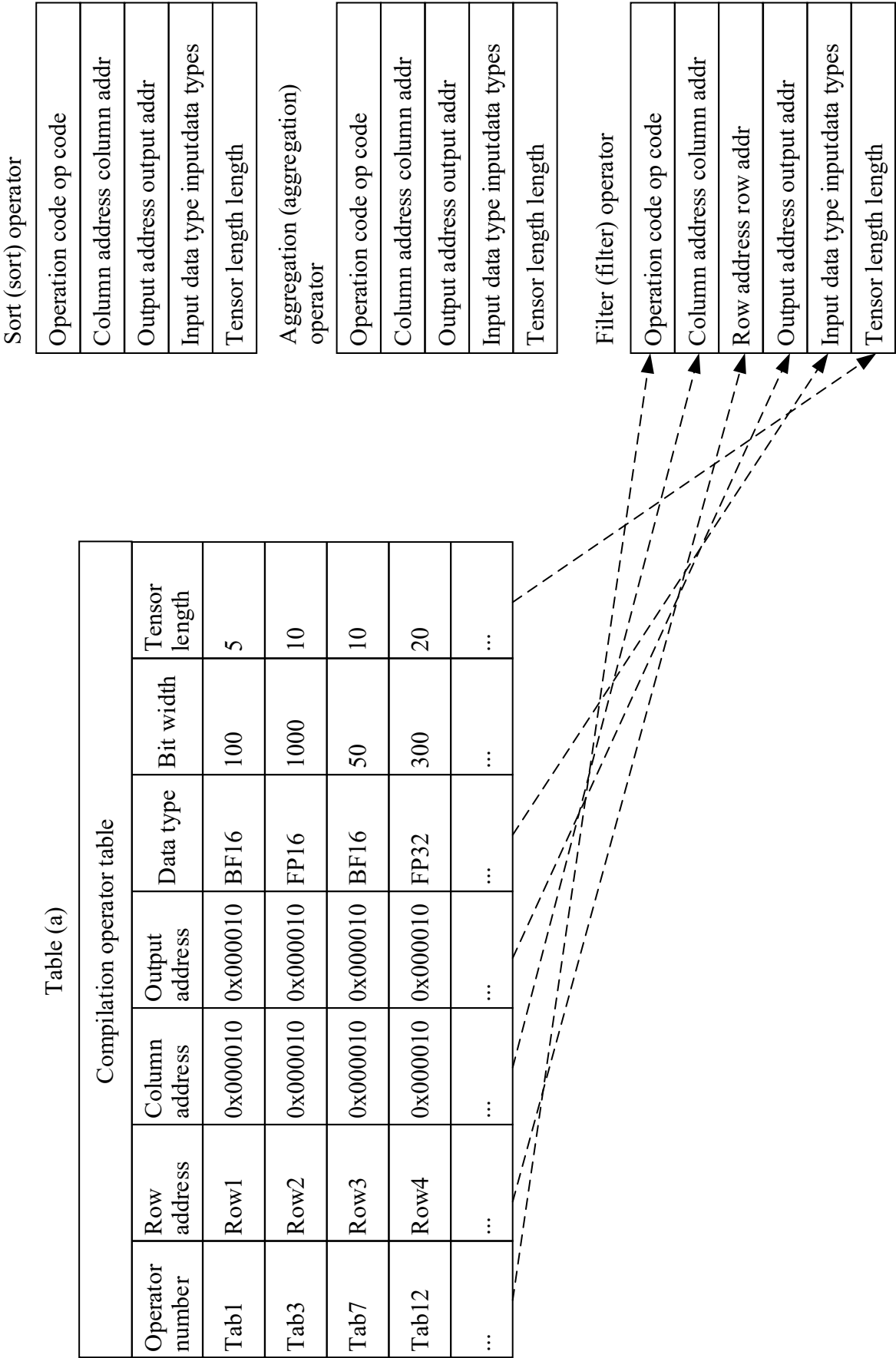


FIG. 4

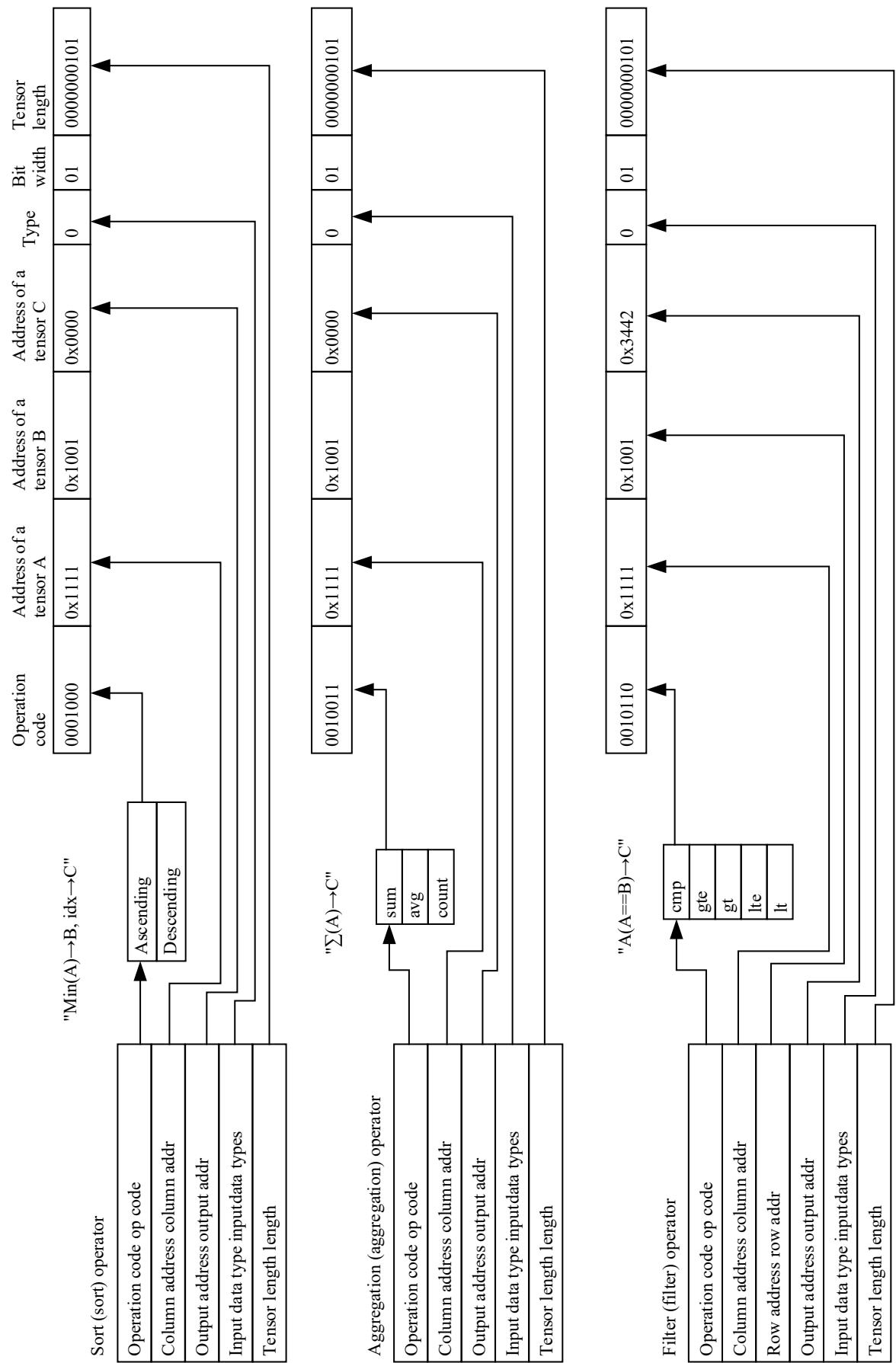


FIG. 5

Address-only participation instruction:	Operation code	Address of a tensor A	Address of a tensor B	Address of a tensor C	Type	Bit width	Tensor length
	Operation code	Address of a tensor A	Address of a tensor B	Numeric value C	Type	Bit width	Tensor length
Numeric value participation instruction:	Operation code	Address of a tensor A	Address of a tensor B	Numeric value C	Type	Bit width	Tensor length
Bank control instruction:	Operation code	Address of a tensor A	Null	Numeric value C	Null	Null	Tensor length
Near-memory circuit control instruction:	Operation code	Memory bank ID	Near-memory circuit type	Near-memory circuit status	Null	Null	Null

FIG. 6

Operator	Source code command	Command 0, instruction 0:	Operation code	Address of a tensor A	Address of a tensor B	Address of a tensor C	Type	Bit width	Tensor length
			1100101	0x1111	0x1001	00111010	0 01 00101		
	Filter Filter		Operation code	Address of a tensor A	Address of a tensor B	Address of a tensor C	Type	Bit width	Tensor length
			1000000	0x1111	0x1001	0x3443	0 01 00101		
Projection Projection	select * from t where t.a > 10	Command 1, instruction 2:	Operation code	Address of a tensor A	Address of a tensor B	Address of a tensor C	Type	Bit width	Tensor length
			0110100	0x3443	0x1101	0x3542	0 01 00101		
Sort ascend Sort ascend	select a+b*c from t	Command 2, instruction 3:	Operation code	Address of a tensor A	Address of a tensor B	Address of a tensor C	Type	Bit width	Tensor length
			1010001	0x1111	0x1001	0x0000	0 01 00101		
	select abs(x) from t	Command 3, instruction 4:	Operation code	Address of a tensor A	Address of a tensor B	Address of a tensor C	Type	Bit width	Tensor length
			0100000	0x1111	0x1001	0x3443	0 01 00101		
	sort based on ascending t.a	Command 3, instruction 5:	Operation code	Address of a tensor A	Null	Numeric value C	Null	Null	Tensor length
			1101000	0x0000	0x3443	0 0 001			
		Command 3, instruction 6:	Operation code	Address of a tensor A	Address of a tensor B	Address of a tensor C	Type	Bit width	Tensor length
			1101000	0x1111	0x1015	0x3573	0 01 00101		
		Command 3, instruction 7:	Operation code	Address of a tensor A	Null	Address of a tensor C	Null	Null	Tensor length
			0100000	0x0000	0x3565	0 0 001			
		Command 3, instruction 8:	Operation code	Address of a tensor A	Address of a tensor B	Address of a tensor C	Type	Bit width	Tensor length
			1101000	0x1111	0x1015	0x3573	0 01 00101		
		Command 3, instruction 9:	Operation code	Address of a tensor A	Null	Address of a tensor C	Null	Null	Tensor length
			0100000	0x0000	0x3565	0 0 001			
		...							

FIG. 7

Scheduler	Instruction number	Transparent transmission operator number	Operation code	Address of a variable A	...	Length	Read address	Write address	Bank identifier bank ID	Read position	Write position
Scheduler	0	0	0100000	0x0011	...	30	[0x0011, 0x0104]	[0x0111]	0	[(1, 4, 1, 8) (2, 3, 4, 7)]	[(0, -1, 0, -1)]
	1	0	0100100	0x0041	...	60	[0x0041, 0x1104]	[0x0871]	3	...	...
	2	0	0001010	0x00321	...	90	[0x0321]	[]	2	...	...
	3	1	0101000	0x1018	...	5	[0x1018]	[0x0111, 0x4443]	1	...	...
	...	...	...	...	...	...	...	...	...	...	...

FIG. 8

	Instruction 0	Instruction 1	Instruction 2	Instruction 3
Instruction 0	0	0	0	0
Instruction 1	3	0	0	0
Instruction 2	0	2	0	0
Instruction 3	0	1	2	0

The instruction 1 has a RAW dependency on the instruction 0

The instruction 2 has a WAW dependency on the instruction 1

The instruction 3 has WAR and WAW dependencies on the instruction 1 and the instruction 2 respectively

FIG. 9

Bank status list		Busy	Near-memory Add states	Near-memory XOR states	...
1	CB1	1	0xF000	0x00000000	...
2	CB2	1	0x0300	0x00000002	...
3	CB3	0	0x0000	0x00000FFF	...
4	CB4	1	0x000C	0x00FF00FF	...

FIG. 10

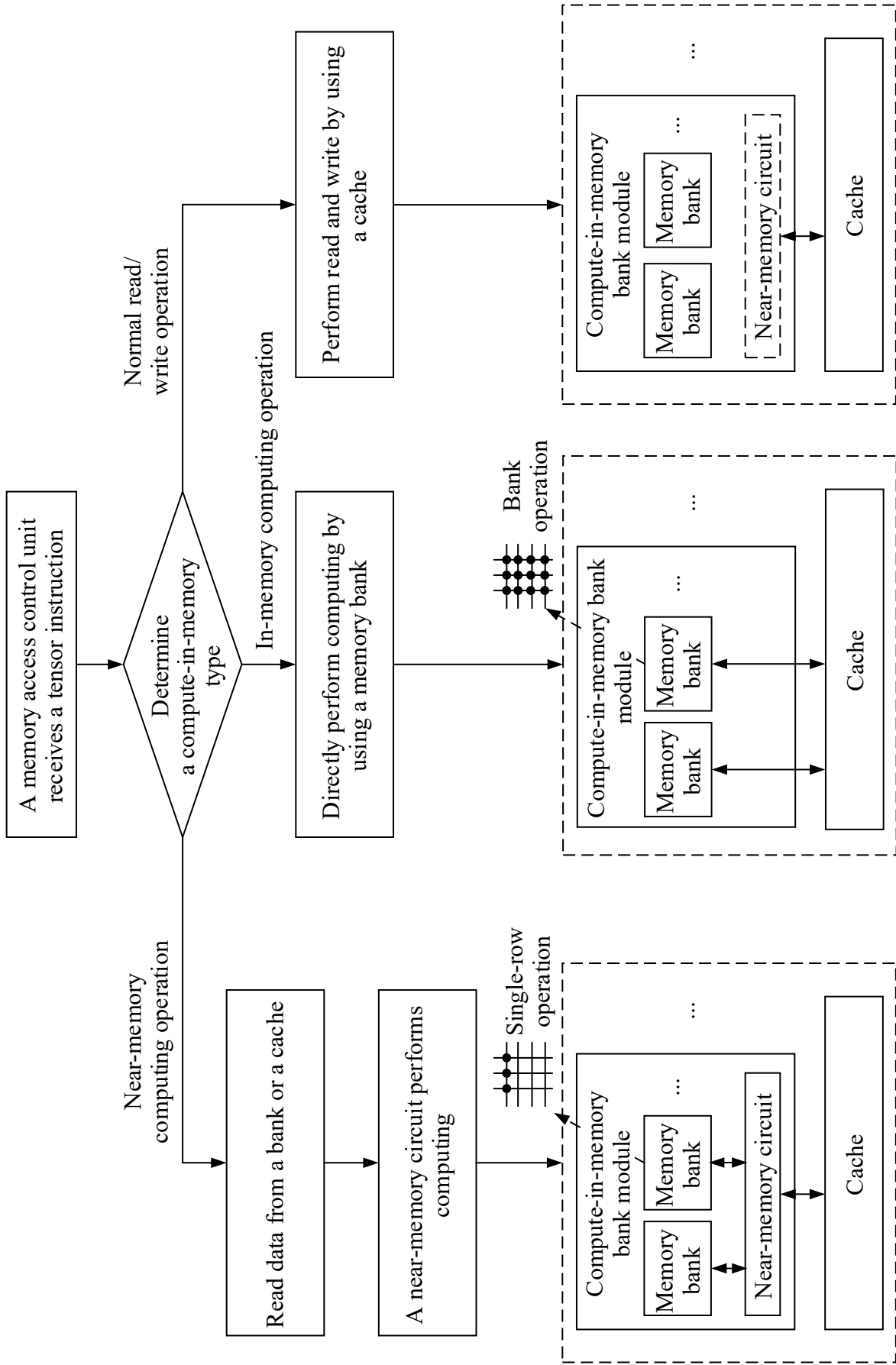


FIG. 11

Diagram (a)

Instruction ID	Operation code	Address A	Address B	Address C	Parameter C	Type	Bit width	Tensor length
0	eand	256	768	512	/	0	01	2
1	subi	512	800	/	2	0	01	2
2	max	8	620	1100	/	0	01	2
3	eand	1200	1456	1968	/	0	01	2

Diagram (b)

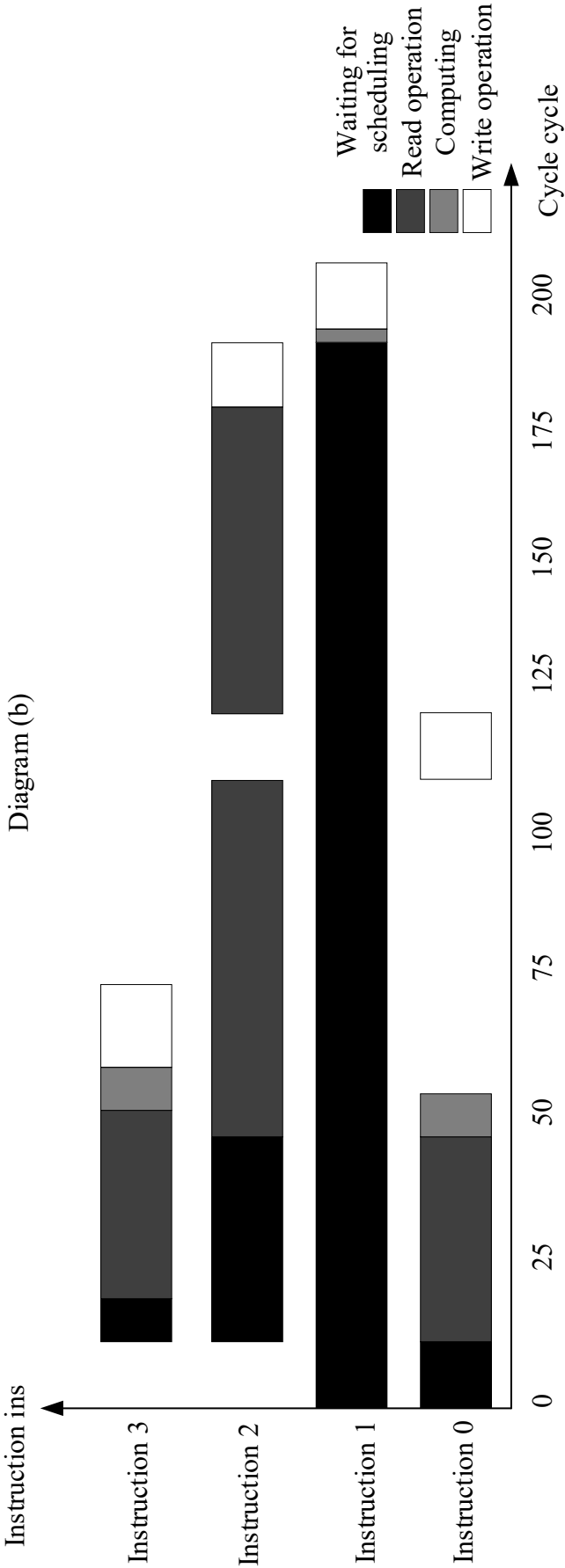


FIG. 12

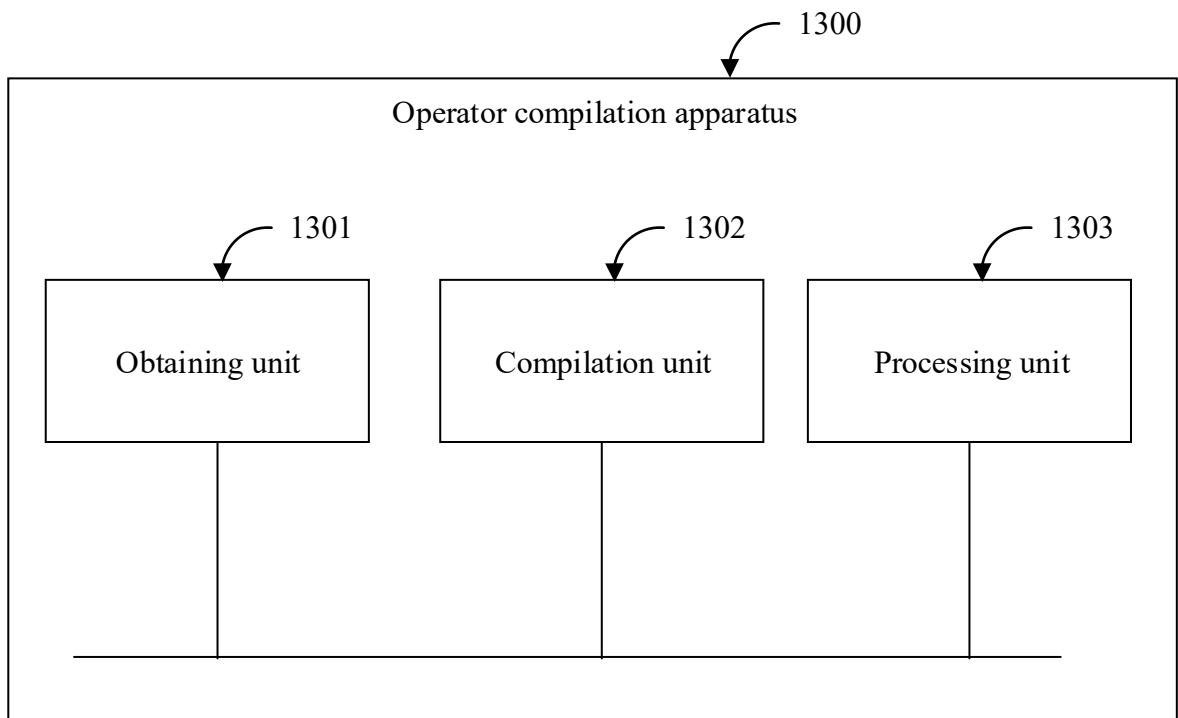


FIG. 13

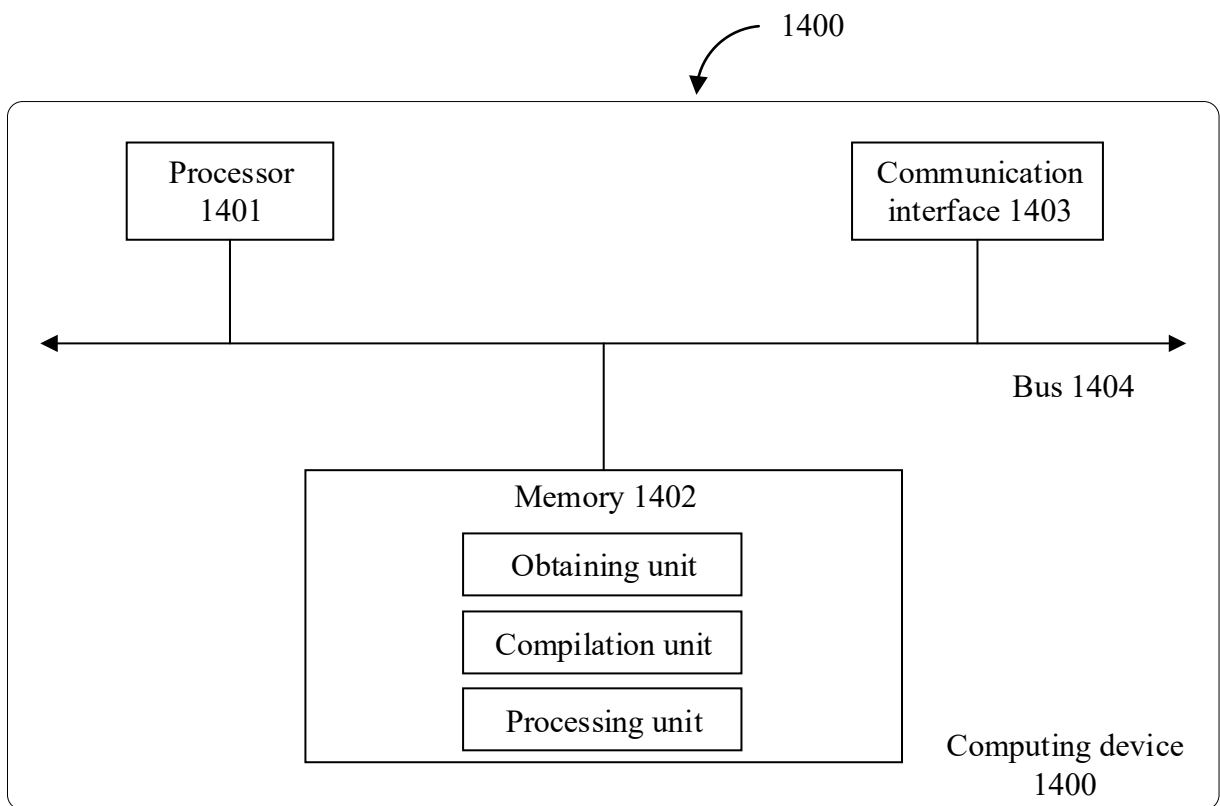


FIG. 14

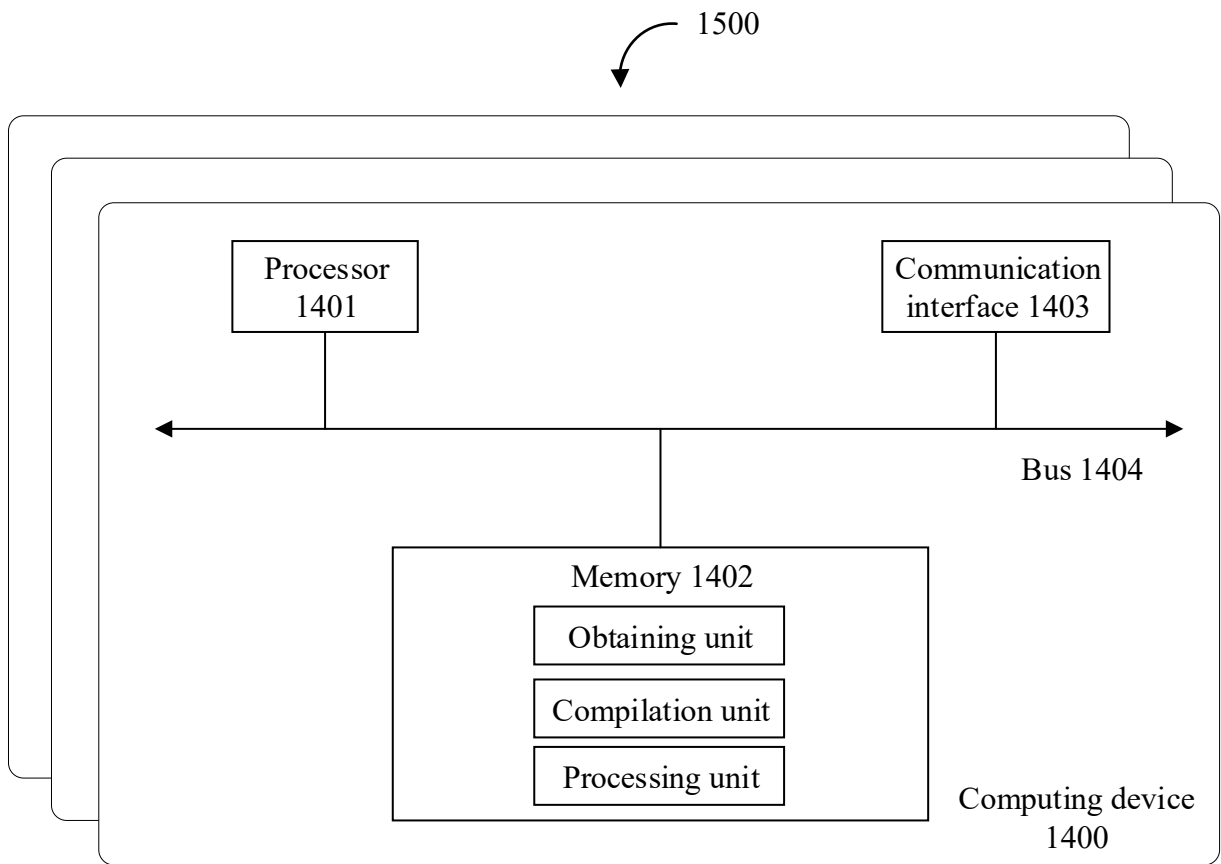


FIG. 15