CLAIMS

1. An apparatus comprising:

first memory cells located in a first device level of a memory device;

second memory cells located in a second device level of the memory device;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein the first memory cells includes a memory cell having a memory element formed in a cavity of the first control gate; and

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein the second memory cells includes a memory cell having a memory element formed in a cavity of the second control gate; and

a conductive channel extending between the memory cell of the first memory cell and the memory cell of the second memory cells, wherein a material of the memory element of the memory cell of the first memory cells is discontinuous from a material of the memory element of the memory cell of the second memory cells.

2. The apparatus of claim 1, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising:

a common source; and

data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.

3. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

5. The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.

6. The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.

7. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

8. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

9. An apparatus comprising:

a first non-volatile memory cell including a first memory element, the first memory element having a ring shape;

a second non-volatile memory cell including a second memory element, the second memory element having a ring shape; and

a conductive material extending through the first and second memory elements, wherein a material of the first memory element is discontinuous from a material of the second memory element.

10. The apparatus of claim 9, further comprising:

a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located; and

a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device.

11. The apparatus of claim 10, wherein each of the memory cells further includes a first dielectric between the respective memory element and the conductive material.

12. The apparatus of claim 11, wherein each of the memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.

13. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data line is located between the substrate and the first memory cell.

14. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line.

15. An apparatus comprising:

a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;

a first dielectric formed on the first sidewall;

a second dielectric formed on the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by the second dielectric;

a first additional dielectric formed on a side of the first memory element;

a second additional dielectric formed on a side of the second memory element; and

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first memory element by the first additional dielectric and from the second memory element by the second additional dielectric, wherein a material of the first memory element is discontinuous from a material of the second memory element.

16. The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.

17. The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.

18. The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.

19. The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.

20. The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.