CLAIMS

1. A semiconductor device (200), comprising a chip (20) and a package substrate (10), wherein the chip (20) is disposed on the package substrate (10), and the package substrate (10) comprises a substrate body (11) and a plurality of unit regions (14) arranged on the substrate body (11), wherein

a unit region (14) of the unit regions (14) comprises two first pin structures (12), one of the two first pin structures (12) comprises six first pins (13), the six first pins (13) are arranged, with two of them in a row, to form three parallel rows of two pins: a first row of pins (1201), a second row of pins (1202), and a third row of pins (1203), four of the first pins in the first row of pins (1201) and the second row of pins (1202) are respectively located at four vertices of a parallelogram, four of the first pins in the second row of pins (1202) and the third row of pins (1203) are respectively located at four vertices of another parallelogram, and the two parallelograms are arranged axisymmetric about the second row of pins (1202), wherein the two first pin structures (12) are arranged in a row direction of the second row of pins (1202), and the two first pin structures (12) are axisymmetric and adjacent to each other; and

the two first pins in the second row of pins (1202) are differential signal pins, and the two first pins in the first row of pins (1201) and the two pins in the third row of pins (1203) are single-ended signal pins; and

wherein in the unit region (14), the two first pin structures (12) are arranged in the row direction of the second row of pins (1202), the two first pin structures (12) are axisymmetric, and the distance between the first rows of pins (1201) in the two first pin structures (12) is greater than a distance between the second rows of pins (1202) in the two first pin structures (12);

the first pin structure (12) comprises a first side (121), a second side (122), a third side (123), and a fourth side (124), the first side (121) is a side that is of the first pin structure (12) and that is away from the other first pin structure in the same unit region (14), the second side (122) is opposite to the first side (121), the third side (123) and the fourth side (124) are both located between the first side (121) and the second side (122), and the third side (123) is opposite to the fourth side (124); and

ground pins are arranged around the first pin structure (12), a quantity of the ground pins arranged around the first pin structure is 11, and connection lines of the 11 ground pins sequentially spaced and arranged along a periphery of the first pin structure form a nonagon,

wherein three ground pins are arranged on the first side (121), three ground pins are respectively located at three vertices of an isosceles triangle, two legs of the isosceles triangle are respectively parallel to sides that are of the two parallelograms of the first pin structure (12) and

that face the first side (121), two ground pins are arranged on the second side (122), a connection line of the two ground pins is orthogonal to the row direction of the second row of pins (1202), three ground pins are arranged on each of the third side (123) and the fourth side (124), and the three ground pins on the same side are sequentially spaced and arranged in the row direction of the second row of pins (1202).

2. The semiconductor device (200) according to claim 1, wherein in the unit region (14), the two first pin structures (12) share the two ground pins on the second side (122).

3. The semiconductor device according to claim 1 or 2, wherein the first row of pins (1201), the second row of pins (1202), and the third row of pins (1203) are sequentially arranged in a column direction, two adjacent unit regions (14) in the row direction of the second row of pins (1202) are staggered in the column direction, and the two adjacent unit regions (14) in the row direction share some of the ground pins.

4. The semiconductor device (200) according to any one of claims 1 to 3, wherein the first row of pins (1201), the second row of pins (1202), and the third row of pins (1203) are sequentially arranged in the column direction, two adjacent unit regions (14) in the column direction are symmetrically arranged, and the two adjacent unit regions (14) in the column direction share some of the ground pins.

5. The semiconductor device (200) according to any one of claims 1 to 4, wherein in the first pin structure (12), a first pin (13) and a connection line of two adjacent first pins (13) define an isosceles triangle, the first pin being one of the pins in the first row of pins (1201) located near the first side (121).

6. The semiconductor device (200) according to any one of claims 1 to 4, wherein in the first pin structure (12), a first pin (13) and a connection line of two adjacent first pins (13) define an isosceles triangle, the first pin being one of the pins in the third row of pins (1203) located near the first side (121).

7. The semiconductor device (200) according to any one of claims 1 to 6, wherein the chip (20) is a central processing unit, the central processing unit is provided with a plurality of memory channels, each memory channel comprises a plurality of byte units, each byte unit corresponds to one unit region (14), and the single-ended signal pins in the unit region (14) are configured to transmit data signals of the corresponding byte unit.

8. An electronic device, comprising a circuit board (100) and the semiconductor device (200) according to any one of claims 1 to 7, wherein the semiconductor device (200) is disposed on the circuit board (100), signal pins are disposed on the circuit board (100), and the signal pins are electrically connected to the semiconductor device (200).