ABSTRACT OF THE DISCLOSURE

SELECTIVE ETCH METHOD FOR SELECTIVELY ETCHING MULTI-LAYER STACK LAYER

A method for forming a patterned microelectronic layer. There is first provided a substrate. There is then formed over the substrate a multi-layer stack layer comprising: (1) a first lower microelectronic layer; (2) a second intermediate patterned microelectronic layer formed over the first lower microelectronic layer; and (3) a third upper patterned microelectronic layer formed over the second intermediate patterned microelectronic layer, where the first lower microelectronic layer and the third upper patterned microelectronic layer are susceptible to etching within a first etchant. There is then formed encapsulating the first lower microelectronic layer and at least portion of the second intermediate patterned microelectronic layer while leaving exposed at least a portion of the third upper patterned microelectronic layer an encapsulating layer. There is then etched selectively, while employing a first etch method which employs the first etchant, the third upper patterned microelectronic layer while the first lower microelectronic layer and at least the portion of the second intermediate patterned microelectronic layer are encapsulated with the encapsulating layer. Finally, there is then stripped, while employing a second etch method which employs a second etchant, from the first microelectronic layer and at least the portion of the second intermediate patterned microelectronic layer the encapsulating layer. The method may be employed for stripping from a gate electrode within a field effect transistor (FET) a patterned dielectric cap layer formed upon the gate electrode while not etching a gate dielectric layer upon which is formed the gate electrode within the field effect transistor (FET).

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)