WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:

a first semiconductor chip on a first substrate;

a first mold layer provided on the first substrate to cover a side surface of the first semiconductor chip;

a solder structure provided on the first substrate; and

a second substrate provided on the solder structure, wherein:

a guide receptacle is formed at one of a top surface of the first mold layer and a bottom surface of the second substrate,

a first alignment protrusion is formed at the other of the top surface of the first mold layer and the bottom surface of the second substrate,

a second protrusion is provided on the bottom surface of the second substrate; and

wherein:

at least a portion of the first alignment protrusion is provided in the guide receptacle, and

the second protrusion is provided on a top surface of the first semiconductor chip.

2. The semiconductor package of claim 1, wherein:

the guide receptacle is formed in the top surface of the first mold layer; and

the second substrate is an interposer substrate and the first alignment protrusion is formed on a bottom surface of the interposer substrate.

3. The semiconductor package of claim 1, wherein a bottom surface of the first alignment protrusion is located at a level lower than an uppermost surface of the first mold layer, and

the bottom surface of the first alignment protrusion is located at a level equal to or higher than a bottom surface of the guide receptacle.

4. The semiconductor package of claim 2, wherein

a bottom surface of the first alignment protrusion is located at a level lower than a bottom surface of the second protrusion.

5. The semiconductor package of claim 1, wherein the first mold layer is provided to have a trench formed in the top surface thereof and to include a first guide portion defined by the trench, and

the guide receptacle is formed in the first guide portion.

6. The semiconductor package of claim 5, wherein a bottom surface of the trench is located at the same level as a bottom surface of the guide receptacle.

7. The semiconductor package of claim 2, further comprising:

a third substrate provided on the interposer substrate;

a second semiconductor chip mounted on the third substrate; and

a second mold layer provided on the third substrate to cover the second semiconductor chip.

8. The semiconductor package of claim 1, wherein the second substrate is formed of an insulating material, and the first alignment protrusion comprises the same insulating material as the first substrate.

9. The semiconductor package of claim 1, wherein the first alignment protrusion is spaced apart from the first semiconductor chip, when viewed in a plan view.

10. A semiconductor package, comprising:

a first substrate;

a first semiconductor chip on the first substrate;

a first mold layer provided on the first substrate to cover a side surface of the first semiconductor chip, the first mold layer comprising:

a first guide portion formed in a top surface thereof, wherein the first guide portion is defined by a trench,

a second guide portion defined by a trench, and provided between an outer side surface of the first substrate and an outermost one of the solder structures when viewed in a plan view;

solder structures provided on the first substrate; and

an interposer substrate provided on the solder structures and spaced apart from the first semiconductor chip,

wherein the interposer substrate comprises a first insulating protruding portion provided on a bottom surface thereof, and

at least a portion of a side surface of the first insulating protruding portion faces

a side surface of the first guide portion.

11. The semiconductor package of claim 10, wherein a bottom surface of the first insulating protruding portion is located at a level lower than a top surface of the first guide portion.

12. The semiconductor package of claim 10, wherein the first insulating protruding portion is spaced apart from the solder structures and the first semiconductor chip.

13. The semiconductor package of claim 10, further comprising an under-fill layer interposed between the side surface of the first insulating protruding portion and the side surface of the first guide portion.

14. The semiconductor package of claim 10, wherein the interposer substrate further comprises a second insulating protruding portion provided on the bottom surface thereof,

the second insulating protruding portion overlaps the first semiconductor chip, when viewed in a plan view, and

the first insulating protruding portion has a thickness in a vertical direction greater than that of the second insulating protruding portion.

15. The semiconductor package of claim 10, wherein the first guide portion comprises a plurality of sub-guide portions spaced apart from each other, and

the first insulating protruding portion is provided between the sub-guide portions.

16. The semiconductor package of claim 10, wherein the first insulating protruding portion comprises a plurality of sub-protruding portions spaced apart from each other, and

the first guide portion is provided between the sub-protruding portions.

17. A semiconductor package, comprising:

a first semiconductor chip on a first substrate;

a first mold layer covering a side surface of the first semiconductor chip, the first mold layer having a first top surface and a second top surface, which is located at a level lower than the first top surface;

a solder structure provided on the first substrate; and

a second substrate provided on the solder structure, wherein the second substrate comprises:

a first protruding portion provided on a bottom surface thereof,

a bottom surface of the first protruding portion is located at a level, which is lower than the first top surface of the first mold layer and is equal to or higher than the second top surface of the first mold layer,

a second protruding portion provided on the bottom surface thereof, and wherein:

the first protruding portion is spaced apart from the solder structure and the first semiconductor chip when viewed in a plan view,

the second protruding portion is provided on a top surface of the

first semiconductor chip.

18. The semiconductor package of claim 17, wherein the second substrate comprises an interposer substrate.

19. The semiconductor package of claim 17, wherein the protruding portion comprises a solder resist material.