SRAM INTEGRATED CIRCUITS WITH BURIED SADDLE-SHAPED FINFET AND METHODS FOR THEIR FABRICATION

ABSTRACT

SRAM ICs and methods for their fabrication are provided. One method includes depositing photoresist on a first oxide layer overlying a silicon substrate (102,) forming a pattern of locations, using said photoresist, for the formation of two inverters (330, 332), each having a pull up transistor (124, 134, 321, 333,) a pull down transistor (120, 136, 323, 331) and a pass gate transistor (128, 130, 328) on said oxide layer. The method involves anisotropically etching U-shaped channels in the oxide layer corresponding to pattern, and thereafter isotropically etching U-shaped channels in the silicon layer to form saddle-shaped fins in the silicon. A second oxide layer is deposited over the saddle-shaped fins, and a first metal layer is deposited over the second oxide layer. A contact metal layer is formed over the first metal layer and planarized to form local interconnections (308, 320) coupling the gate electrodes of one inverter to a node between the pull up and pull down transistors of the other inverter and to a source/drain of one of the pass gate transistors.

Fig. 1