

Monolithic High Voltage Driver Circuit

Field of the Invention

5 This invention relates to a monolithic high voltage driver circuit, and more particularly, though not exclusively to such a high voltage driver circuit for use as an interface between low voltage video signals input to a Cathode Ray Tube (CRT) display, such as a computer monitor, and the high voltages required at the cathodes of the CRT.

10 Background of the Invention

The video driver circuit for a computer monitor is required to interface between the low voltage video input signals, which are generally between 1 and 5 Volts peak-to-peak, and the high voltages required at the cathodes of the monitor, which should be 15 about 40-50 Volts peak-to-peak, with a bandwidth equivalent of 45-70 MHz or more. Known video driver circuits for computer monitors are generally built either using discrete components or as a hybrid circuit, for example circuit LM2407 manufactured by National Semiconductors. Such circuits are expensive, since 20 separate components are required. Furthermore, the known circuits are difficult to drive, requiring high input current and about 4 volts peak-to-peak input voltage.

It would therefore be desirable to produce a high voltage driver circuit in monolithic form. However, such a circuit would 25 usually need to be produced using high voltage analog manufacturing processes, due to the components necessary for the voltages involved. In such a manufacturing process, the PNP and NPN components are not symmetrical, causing a substantial asymmetry in the output signal, which is undesirable. Also it is 30 difficult to provide high quality transistors of both PNP and NPN types in the same process. This asymmetry can be seen as waveform 89 in FIG. 7. Waveform 86 shows the theoretical ideal waveform.

Brief Summary of the Invention

35 The present invention therefore seeks to provide a monolithic high voltage driver circuit which overcomes, or at least reduces the above-mentioned problems of the prior art.

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Accordingly, the invention provides a monolithic high voltage driver circuit comprising a circuit input for receiving a low voltage input signal, a circuit output for providing a high voltage output signal, a reference voltage source, a main amplifier coupled to a supply voltage source and having a first input coupled to the circuit input, a second input coupled to the reference voltage source, and an output, a pull-up output stage having an input coupled to the output of the main amplifier and an output coupled to the circuit output, a pull-down output stage having an input coupled to the output of the main amplifier and an output coupled to the circuit output.

In a preferred embodiment of the invention the pull-down output stage comprises a control stage and an amplifier stage having an input and an output coupled to the circuit output, the control stage comprising a first input coupled to the output of the main amplifier, a second input coupled to the circuit output and an output coupled to the input of the amplifier stage.

Preferably, the control stage comprises an auto-bias stage having a capacitor coupled between a current source and the circuit output for enabling fast pull-down of the high voltage output signal at relatively high frequencies.

In one embodiment, the auto-bias stage further comprises a transistor having a first current electrode coupled to the capacitor on the current source side, a second current electrode coupled to the input of the amplifier stage and a control electrode coupled to the output of the main amplifier.

Conveniently, the control stage comprises a comparator having a first input coupled to the output of the main amplifier, a second input coupled to the circuit output and an output coupled, via a current mirror, to the amplifier stage.

Preferably, the comparator compares a voltage at the output of the main amplifier with a voltage at the circuit output and providing a control signal to the amplifier stage to turn on the amplifier stage when the voltage at the output of the main amplifier is lower than the voltage at the circuit output so as to increase the current draining from the circuit output.

In an embodiment of the invention, the monolithic high voltage driver circuit further comprises a current buffer stage coupled between the first input of the comparator and the output of the main amplifier to provide a voltage signal to the first input of the comparator, for decreasing the load on the output of the main amplifier and for compensating, under static conditions, for the voltage drop across the pull-up output stage.

The monolithic high voltage driver circuit preferably further comprises a biasing stage coupled between the reference voltage source and a ground reference potential and provides an output to a load resistor coupled the output of the auto-bias stage. Preferably, the biasing stage biases the amplifier stage to be off during static, or low frequency, operation.

Conveniently, the circuit can be manufactured in Metal Oxide Semiconductor (MOS) technology.

Brief Description of the Drawings

One embodiment of the invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 shows a schematic block diagram of a known video monitor application system ;

FIG. 2 shows a schematic circuit diagram of a hybrid driver circuit used in the system of FIG. 1;

FIG. 3 shows a schematic block diagram of a monolithic high voltage video driver circuit according to one embodiment of the present invention;

FIG. 4 shows a schematic block diagram of one of the active pull-down circuits used in the monolithic video driver circuit of FIG. 3;

FIG. 5 shows a schematic block diagram of another of the active pull-down circuits used in the monolithic video driver circuit of FIG. 3;

FIG. 6 is a schematic circuit diagram showing the circuit of FIG. 3 in more detail; and

FIG. 7 shows a sample output waveform showing the improvements made by the circuit of FIG. 6.

Detailed Description of the Drawings

Thus, as shown in FIG. 1, a typical, known, circuit 1 used for the purpose of providing a high voltage drive at high frequency for driving CRT's in computer, and other, monitor applications, includes a pre-amplifier 2, whose output is coupled to a discrete or hybrid driver circuit 3, which is a discrete circuit of individual transistors discretely wired and including thin film, or thick film, resistors mounted on an insulating substrate. Such a hybrid circuit 3 is expensive because of the additional assembly work involved but has the advantage that optimized PNP and NPN transistors can be used in the same module. In this typical application the load capacitance C represents the typical load presented by the cathode of the CRT and it's associated components.

The conventional hybrid circuit 3 has an internal circuit as shown in FIG. 2. A voltage amplifier is formed using transistors 4 and 5 and resistors 6 and 7. Resistor 7 is used to degenerate the voltage gain and to improve the linearity of the transfer characteristic of the amplifier. The base of transistor 4 is connected to a reference voltage supply V_{ref} , which is usually 12 Volts. The output of the amplifier, taken at the junction of resistor 6 and the collector of transistor 4 is coupled to the bases of two transistors 8 and 9. Transistors 8 and 9 are coupled together to form a "Class B" output stage.

Transistors 4 and 5 are connected in a cascode arrangement used to minimize the "Miller" feedback capacitance, so as to maximize the frequency response. Since the circuit is built using discrete transistors, it is possible to select suitable PNP and NPN devices for this output stage. However, as mentioned above, the circuit is expensive to manufacture.

Referring now to FIG 3, a schematic block diagram of a Driver Circuit according to an embodiment of the present invention is shown. A main amplifier 10, which is essentially similar to that described above with reference to FIG. 2, is shown in detail in FIG. 6 as box 10 including transistors 21 and 22 and resistors 20 and 23. In this case, however, transistor 21 is formed of an MOS

device, which has some desirable characteristics, as will be described below.

As shown in FIG. 3, the output of the main amplifier 10 is coupled to an pull-up stage 11, a first active pull-down stage 13 and a second active pull-down stage 14. The outputs of the active pull-up stage 11, the first active pull-down stage 13 and the second active pull-down stage 14 are coupled together, and to the output of a static pull-down stage 12 to provide the output.

The pull-up stage 11 is essentially similar to transistor 8 used in the known circuit of FIG. 2, except that this transistor 8 is replaced in the circuit shown in FIG. 6 by a pair of MOSFET devices 26 and 27 coupled together in a Darlington manner, together with resistor 28. As shown in the circuit of FIG. 6, the static pull-down stage 12, formed by resistor 29, transistor 30 and resistor 31 coupled in series between the Vout and Gnd, also provides some small pull-down current to provide a negative-going transition. The gate of transistor 30 is coupled to reference voltage source Vref. Resistor 29 is used to provide a small voltage shift, as will be more fully described below.

It is a requirement of any driver circuit that is uses a minimum of power, so the static pull-down stage 12 will only be useful at low frequencies. Also, in the monolithic manufacturing processes available at the present time, no suitable PNP transistor or P-channel MOSFET is available. The present invention therefore seeks to overcome the deficiency of the available processes.

The first active pull-down stage 13 is shown in diagrammatic form in FIG. 4. This stage 13 is formed by a current source 81, used to provide current to an auto-bias amplifier 15, whose output is coupled to a pull-down amplifier 16 biased by a bias reference voltage source 17. The auto-bias amplifier 15 receives two inputs V1 and V2, which are taken from the output of the main amplifier 10 and the output terminal Vout of the driver circuit.

The auto-bias amplifier 15 includes a MOS transistor 32 and a capacitor 33, as shown in FIG. 6. The input from the main amplifier 10 is applied to the gate of transistor 32. However, since the gate voltage of the available P-channel MOS transistor 32 cannot be sufficiently well defined in the present manufacturing process, an "auto-bias" arrangement is used by taking a current provided from the current source 81. The current source 81 receives current from a current generator 80 formed by a transistor 38 and resistor 39 and mirrors it by means of a current mirror formed by transistor 37 and resistor 36. The current source 81 also includes current transistor 34 and degenerating resistor 35, with the output current being provided at the drain of transistor 34. Capacitor 33 provides the coupling from the other input taken from the output terminal Vout. The output of the auto-bias amplifier 15 is coupled to a pull-down amplifier 16, formed by transistors 40, 41 and 42 and resistor 43. In this way the signal at the output terminal is compared with the output on the main amplifier in the amplifier transistor 32, so that when the output terminal is slow to respond to the change of voltage at the output of the main amplifier, then further current may be provided through the arrangement of the auto-bias amplifier 15 and the pull-down amplifier 16. This technique enables the required improvement of the waveform for fast edges, as is shown by waveform 87 in FIG. 7.

An important aspect of the arrangement of the first active pull-down stage 13 is that it must not increase the static load current of the total circuit. In order to achieve this, the bias reference voltage source 17 is provided to bias the pull-down amplifier 16. The bias reference voltage source 17 is formed by resistors 44, 45 and 48 and transistors 46 and 47. The resistor 45 provides an offset voltage so that the transistor 42 of the pull-down amplifier 16 is normally biased below its threshold gate voltage.

The second active pull-down stage 14 is shown in more detail in FIG. 5. Similarly to the first active pull-down stage, the second active pull-down stage includes an amplifier 18 supplied

from a current source 19 and having an output coupled to an output stage 82, the output of which is coupled to the output terminal Vout. The amplifier 18 also has two inputs, of which one input V3 is taken from a voltage shifted point relative to the output terminal Vout, and the other input is coupled to an extra "dummy" output stage 83, which takes its input V4 from the output of main amplifier 10. The "dummy" output stage 83 is actually internal to the circuit so that it does not have the capacitive load normally associated with the actual output stage due to the load applied to the terminal Vout.

As shown in FIG. 6, the amplifier 18 is formed as a comparator formed by a long-tailed pair of transistors 49 and 50. The current source 19 is formed by the current mirror formed by current transistor 52 and degenerating resistor 51, in conjunction with the current mirror formed by transistor 37 and resistor 36 of current source 81. The voltage shift for input V3 is provided using the resistor 29 and the static pull down current provided by the static pull-down stage 12, already described. The "dummy" output stage 83, providing the other input to the amplifier 18 is formed as a current buffer stage provided by transistors 53 and 54 and resistor 55. This arrangement of the long tailed pair 49 and 50 in the second active pull-down circuit enables improvement of the output waveform for frequencies intermediate to the low frequencies where the static pull-down stage 12 is sufficient and the high frequencies where the first active pull-down stage 13 is used. This improvement can be seen in waveform 88 in FIG. 7.

The output of amplifier 18 is coupled to the output stage 82 formed as an amplifier using transistors 62, 63, 64, 65, 66 and 67 and resistors 61 and 68, as shown in FIG. 6, to provide the additional pull-down current required at Vout in response to the "dummy" output stage 83 providing a lower voltage than that already achieved at the output terminal Vout. This situation occurs whenever there is a significant load at the output terminal.

The complete circuit also includes a buffer stage 84 to increase the input impedance of the whole circuit, and this is

formed by transistors 70 and 72 and resistors 69, 71, 73 and 74, as shown in FIG. 6. Transistors 56, 57 and 59 and resistors 58 and 60 form a pull-down amplifier 85, which pulls down the output of the "dummy" output stage 83 and takes as input the output from the auto-bias amplifier 15.

As shown in FIG. 7, the first active pull-down stage 13, produces a large improvement in the negative-going edge, shown as waveform 87, and the second active pull-down stage 14 further improves the waveform, as shown by waveform 88, to move it downwards towards the ideal negative level. In all cases, the rising edge is not ideal, but is relatively sharp.

Thus, there has been described a monolithic video driver circuit having a lower cost than previously known driver circuits, but still providing the performance necessary for high voltage applications.

It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

Claims

1. A monolithic high voltage driver circuit comprising:
a circuit input for receiving a low voltage input signal;
5 a circuit output for providing a high voltage output signal;
a reference voltage source;
a main amplifier coupled to a supply voltage source and
having a first input coupled to the circuit input, a second input
coupled to the reference voltage source, and an output;
10 a pull-up output stage having an input coupled to the output
of the main amplifier and an output coupled to the circuit output;
at least one pull-down output stage having an input coupled
to the output of the main amplifier and an output coupled to the
circuit output.
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2. A monolithic high voltage driver circuit according to claim 1,
wherein the pull-down output stage comprises a control stage and
an amplifier stage having an input and an output coupled to the
circuit output, the control stage comprising a first input coupled to
20 the output of the main amplifier, a second input coupled to the
circuit output and an output coupled to the input of the amplifier
stage.
3. A monolithic high voltage driver circuit according to claim 2,
25 wherein the control stage comprises an auto-bias stage having a
capacitor coupled between a current source and the circuit output
for enabling fast pull-down of the high voltage output signal at
relatively high frequencies.
- 30 4. A monolithic high voltage driver circuit according to claim 3,
wherein the auto-bias stage further comprises a transistor having
a first current electrode coupled to the capacitor on the current
source side, a second current electrode coupled to the input of the
amplifier stage and a control electrode coupled to the output of
35 the main amplifier.



5. A monolithic high voltage driver circuit according to any one of claims 2, 3 or 4, wherein the control stage comprises a comparator having a first input coupled to the output of the main amplifier, a second input coupled to the circuit output and an output coupled, via a current mirror, to the amplifier stage.
6. A monolithic high voltage driver circuit according to claim 5, wherein the comparator compares a voltage at the output of the main amplifier with a voltage at the circuit output and provides a control signal to the amplifier stage to turn on the amplifier stage when the voltage at the output of the main amplifier is lower than the voltage at the circuit output so as to increase the current draining from the circuit output.
7. A monolithic high voltage driver circuit according to either claim 5 or claim 6, further comprising a current buffer stage coupled between the first input of the comparator and the output of the main amplifier to provide a voltage signal to the first input of the comparator, for decreasing the load on the output of the main amplifier and for compensating, under static conditions, for the voltage drop across the pull-up output stage.
8. A monolithic high voltage driver circuit according to claim 7, wherein the current buffer stage comprises a Darlington source-follower.
9. A monolithic high voltage driver circuit according to either claim 3 or claim 4, further comprising a biasing stage coupled between the reference voltage source and a ground reference potential and provides an output to a load resistor coupled the output of the auto-bias stage.
10. A monolithic high voltage driver circuit according to claim 9, wherein the biasing stage biases the amplifier stage to be off during static, or low frequency, operation.



11. A monolithic high voltage driver circuit according to any preceding claim, wherein the circuit is manufactured in Metal Oxide Semiconductor (MOS) technology.
- 5 12. A monolithic high voltage driver circuit according to any preceding claim, wherein the circuit is manufactured utilising active elements which are formed of any one or more of Metal Oxide Semiconductor (MOS) transistors, Field Effect Transistors (FET),
- 10 Bipolar Junction Transistors (BJT), P-channel transistors, N-channel transistors, PNP transistors or NPN transistors.
13. A monolithic high voltage driver circuit substantially as hereinbefore described with reference to the drawings.

