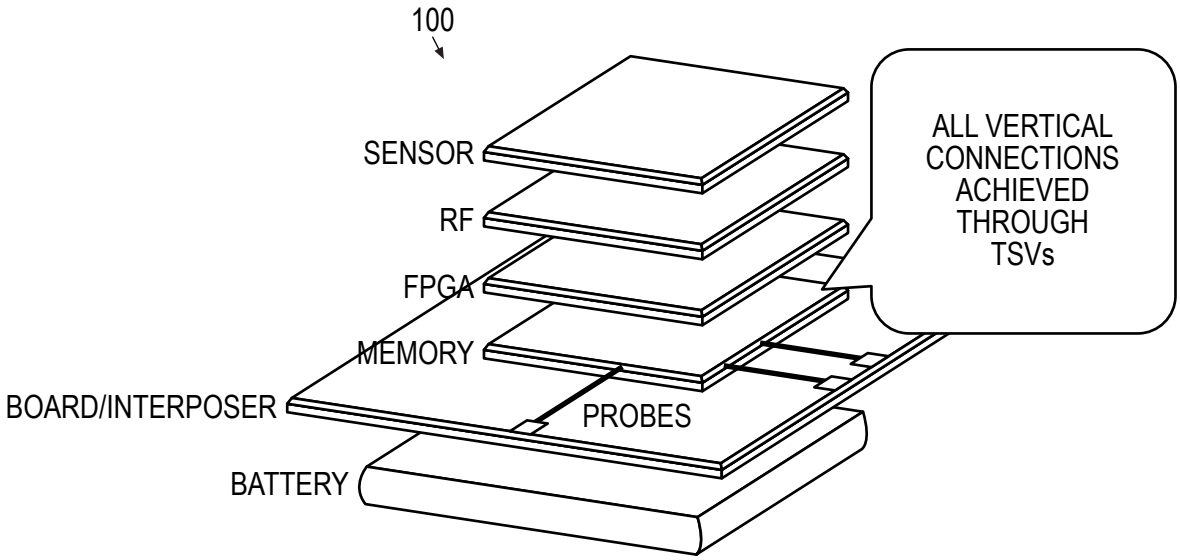

100
SENSOR
RF
FPGA
MEMORY
BOARD/INTERPOSER
PROBES
BATTERY
ALL VERTICAL CONNECTIONS ACHIEVED THROUGH TSVs

FIG. 1

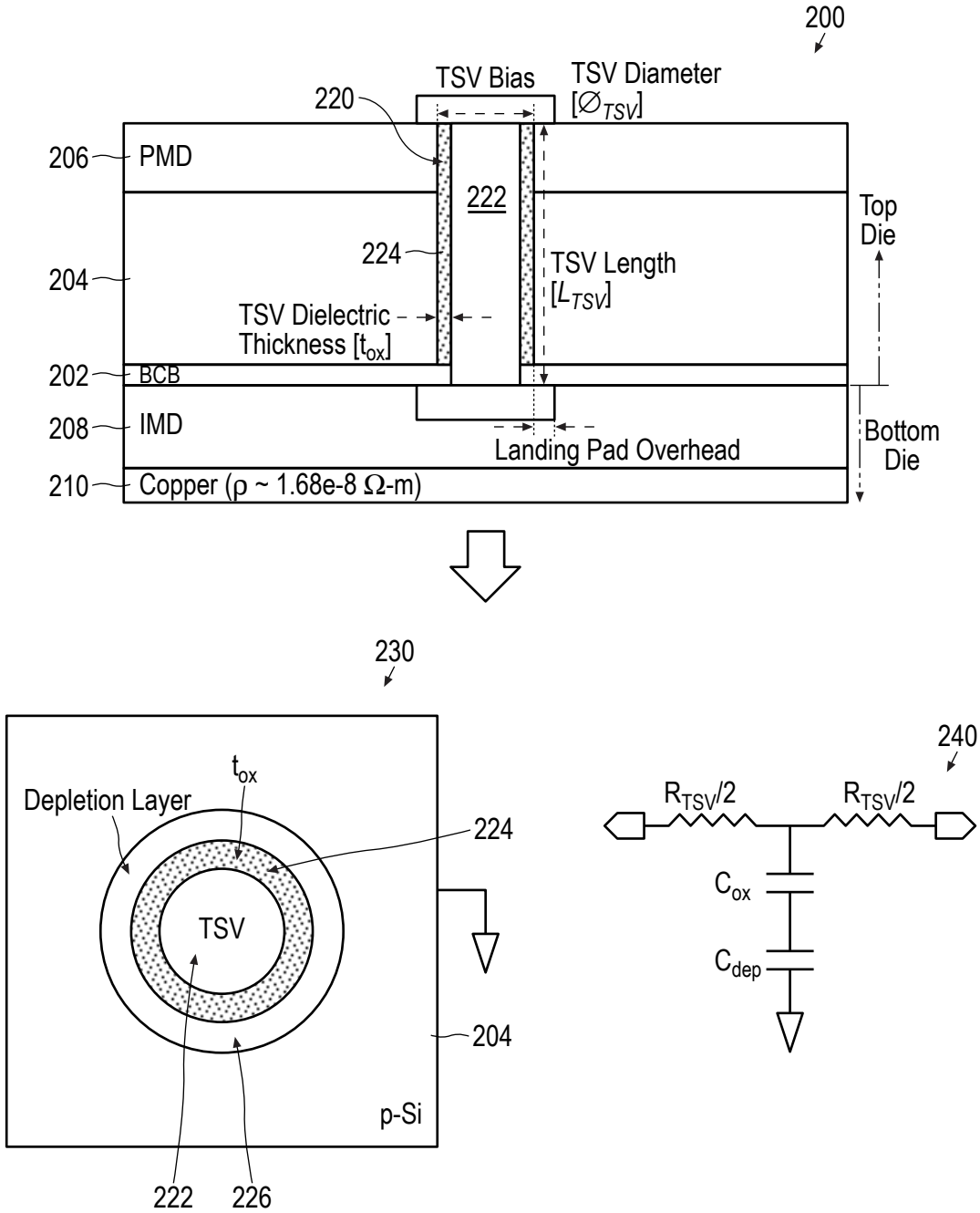

200
TSV Bias
TSV Diameter
[∅TSV]
220
206
PMD
222
Top
Die
224
204
TSV Length
[LTSV]
TSV Dielectric
Thickness [tox]
202
BCB
208
IMD
Landing Pad Overhead
Bottom
Die
210
Copper (ρ ~ 1.68e-8 Ω-m)
230
tox
Depletion Layer
224
TSV
204
p-Si
222
226
240
RTSV/2
RTSV/2
Cox
Cdep

FIG. 2

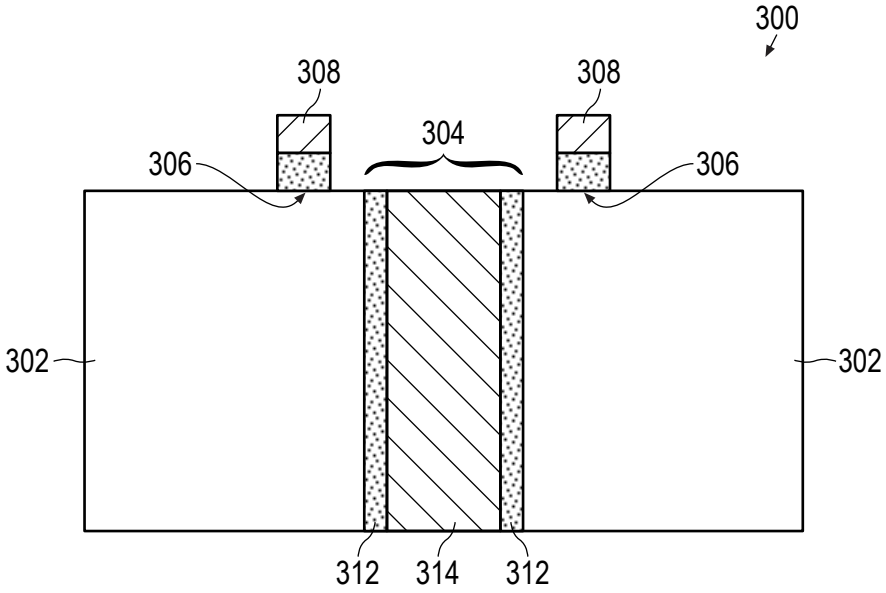


FIG. 3

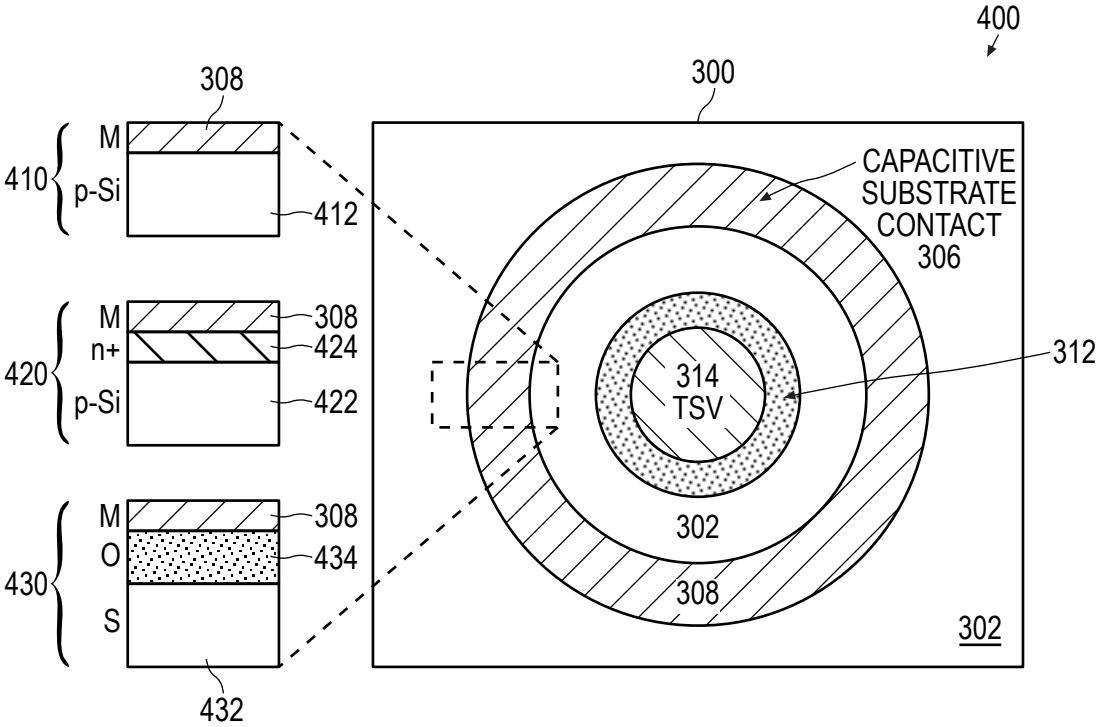

400
308
300
410
M
p-Si
412
CAPACITIVE
SUBSTRATE
CONTACT
306
420
M
n+
p-Si
308
424
422
312
314
TSV
302
308
302
430
M
O
S
308
434
432

FIG. 4

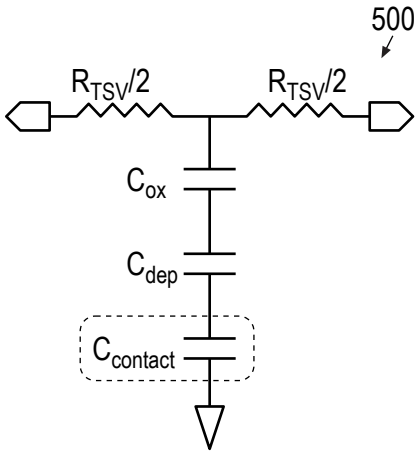


FIG. 5

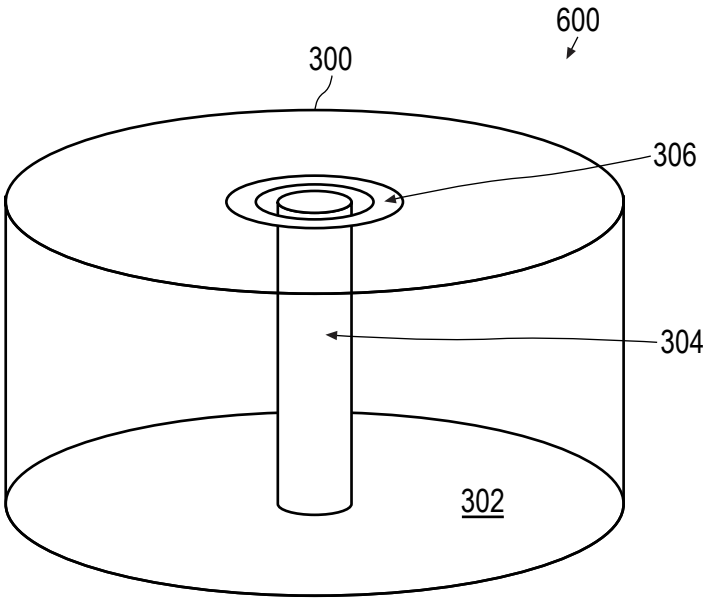


FIG. 6

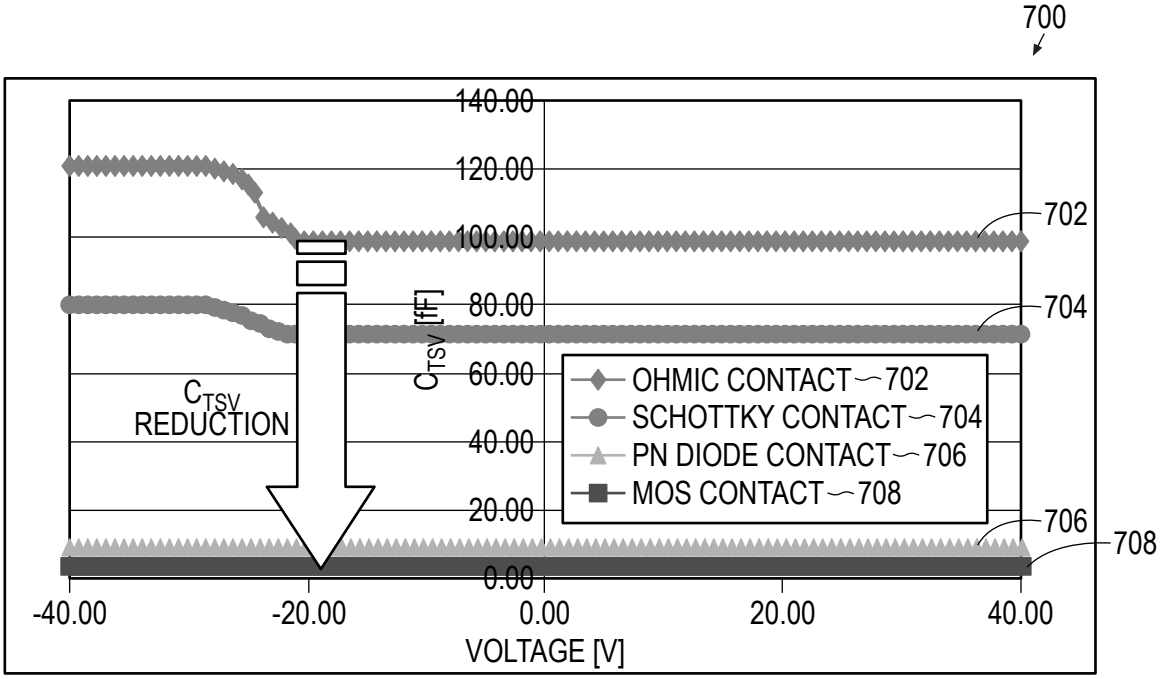

700
140.00
120.00
100.00
80.00
60.00
40.00
20.00
0.00
C_{TSV} [fF]
C_{TSV} REDUCTION
OHMIC CONTACT 702
SCHOTTKY CONTACT 704
PN DIODE CONTACT 706
MOS CONTACT 708
702
704
706
708
-40.00
-20.00
0.00
20.00
40.00
VOLTAGE [V]

FIG. 7A

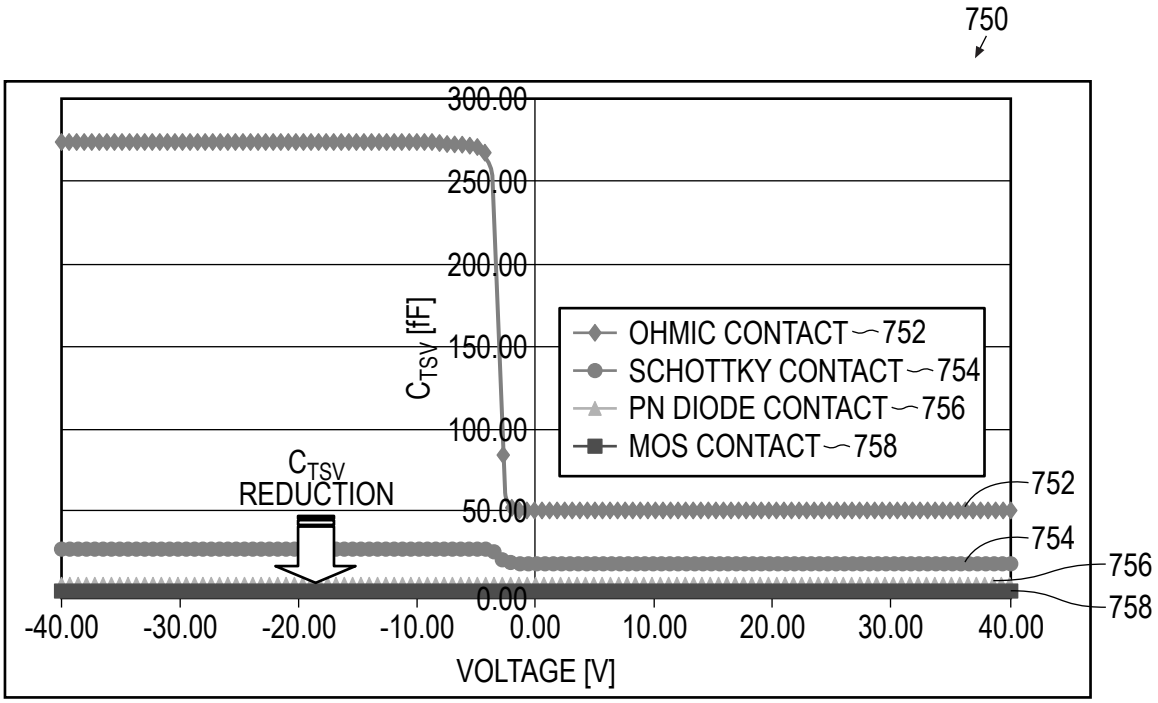

750
300.00
250.00
200.00
150.00
100.00
50.00
0.00
C_{TSV} [fF]
OHMIC CONTACT 752
SCHOTTKY CONTACT 754
PN DIODE CONTACT 756
MOS CONTACT 758
C_{TSV} REDUCTION
752
754
756
758
-40.00
-30.00
-20.00
-10.00
0.00
10.00
20.00
30.00
40.00
VOLTAGE [V]

FIG. 7B

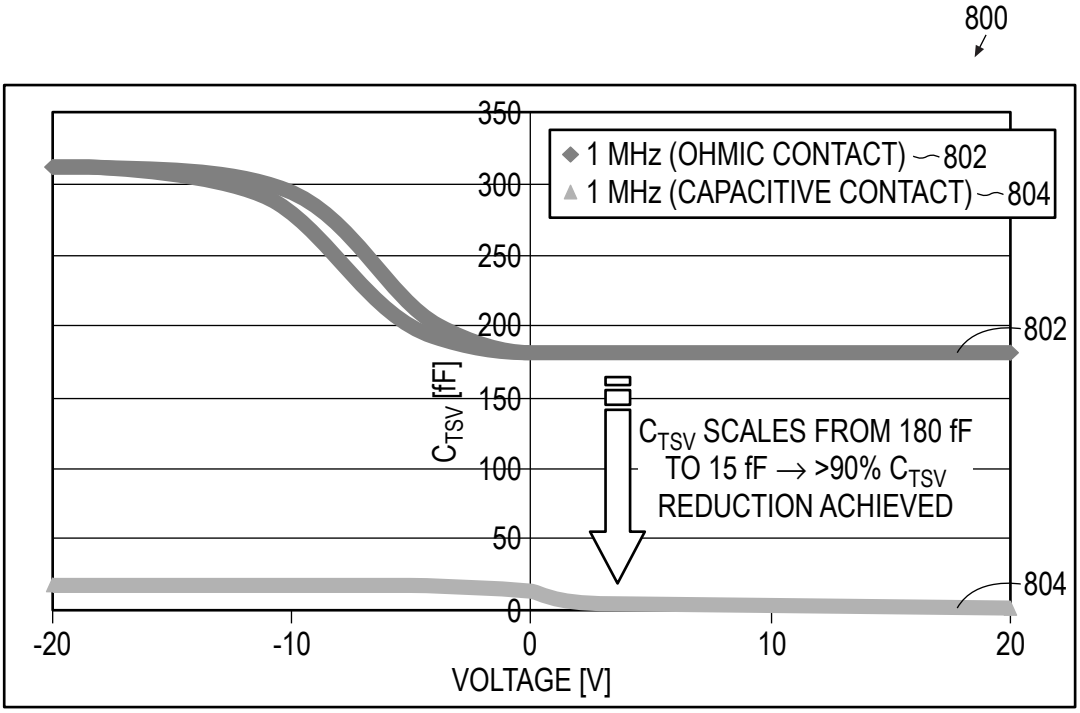

800
350
300
250
200
150
100
50
0
-20
-10
0
10
20
VOLTAGE [V]
C_{TSV} [fF]
1 MHz (OHMIC CONTACT) 802
1 MHz (CAPACITIVE CONTACT) 804
802
804
C_{TSV} SCALES FROM 180 fF TO 15 fF → >90% C_{TSV} REDUCTION ACHIEVED

FIG. 8

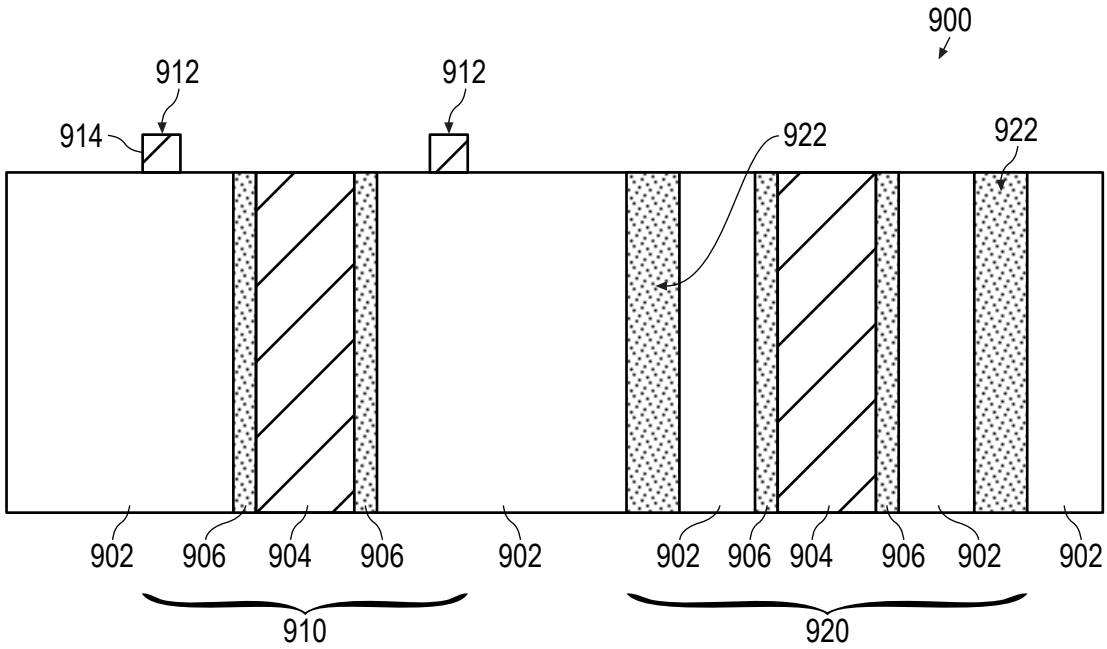

900
912
912
914
922
922
902
906
904
906
902
902
906
904
906
902
902
910
920

FIG. 9

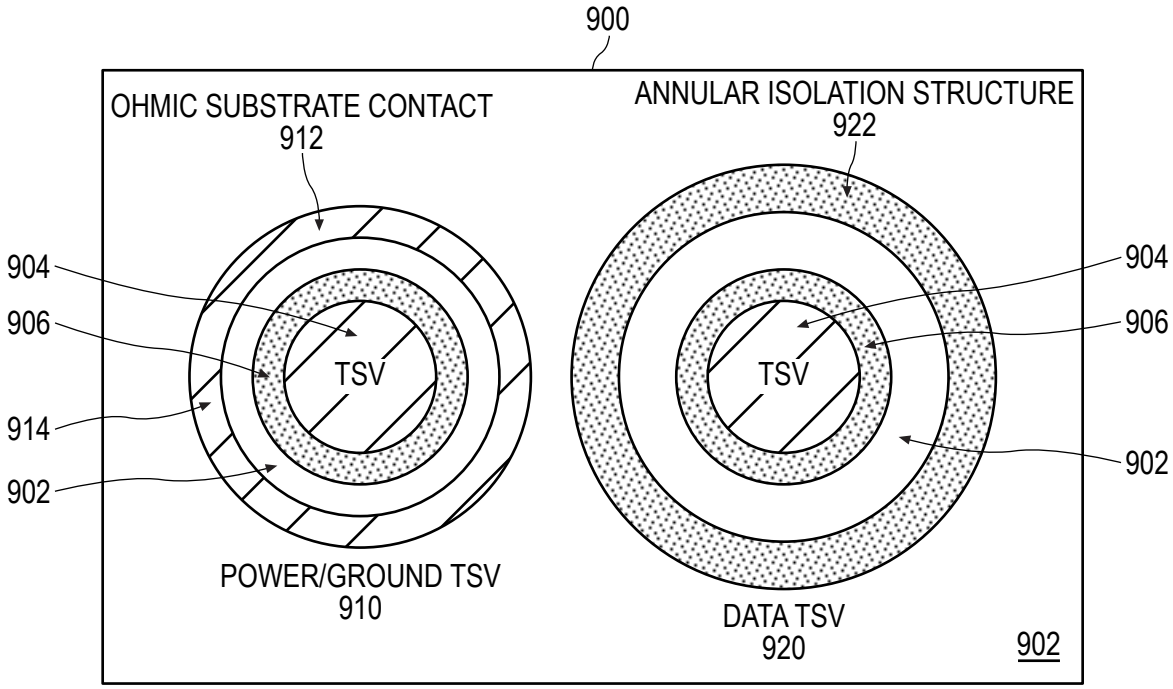

900
OHMIC SUBSTRATE CONTACT
912
ANNULAR ISOLATION STRUCTURE
922
904
906
914
902
TSV
TSV
904
906
902
POWER/GROUND TSV
910
DATA TSV
920
902

FIG. 10