SEMICONDUCTOR DIE WITH THROUGH-HOLE VIA ON SAW STREETS AND THROUGH-HOLE VIA IN ACTIVE AREA OF DIE

Field of the Invention

The present invention relates in general to semiconductor packaging and, more particularly, to stackable semiconductor die having through-hole vias formed along saw streets and through-hole vias on the active silicon area of the die.

Background of the Invention

Semiconductor devices are found in many products used in modern society. Semiconductors find applications in consumer items such as entertainment, communications, networks, computers, and household items markets. In the industrial or commercial market, semiconductors are found in military, aviation, automotive, industrial controllers, and office equipment.

The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each die contains hundreds or thousands of transistors and other active and passive devices performing a variety of electrical functions. For a given wafer, each die from the wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and/or environmental isolation.

Semiconductor manufacturers are increasingly adopting packaging techniques which involve three-dimensional (3D) interconnects between the semiconductor devices. The 3D interconnects provide advantages such as size reduction, reduced interconnect length, and integration of devices with different functionality into an overall 3D package. One way of implementing 3D interconnects involves the use of through-hole vias (THV). THVs are typically located around the perimeter of the die along its saw street guides. Most, if not all, semiconductor packages use the THVs to route signals between adjacent die. However, THVs on saw streets alone limit signal routing options and reduce signal routing density. Present day high density packaging require high density and flexible interconnect capability, which is difficult to achieve through the THVs on saw streets.

A need exists to increase signal routing options and density in a semiconductor wafer having THVs.

Summary of the Invention

In one embodiment, the present invention is a method of forming a semiconductor wafer comprising the steps of forming a semiconductor wafer having a plurality of die with contact pads disposed on a first surface of an active area of each die, the semiconductor wafer having saw street guides between each die, forming a trench in the saw street guides, filling the trench with organic material, forming a plurality of first via holes in the organic material, forming a plurality of second via holes through the contact pads on the active area of the die, forming traces between the contact pads and first via holes, depositing conductive material in the first and second via holes to form first

metal vias on saw streets and second metal vias on the active area of the die, and singulating the semiconductor wafer along the saw street guides to separate the die into individual units.

In another embodiment, the present invention is a semiconductor wafer comprising a plurality of die with contact pads disposed on a first surface of an active area of each die. The semiconductor wafer includes saw street guides between each die. A plurality of first metal vias is formed in the saw street guides and is surrounded by organic material. A plurality of second metal vias is formed in the active area of the die. A plurality of traces connects the contact pads and first metal vias.

In another embodiment, the present invention is a semiconductor package comprising a plurality of stacked die, each die including a plurality of contact pads disposed on a first surface of an active area of the die, a plurality of first metal vias formed along a perimeter of the die, a plurality of second metal vias formed in the active area of the die, and a plurality of traces electrically connecting the first metal vias to the contact pads. The first and second metal vias provide electrical interconnect between the stacked die.

In another embodiment, the present invention is a semiconductor package comprising a first semiconductor die having contact pads and a plurality of first metal vias formed along a perimeter of the die electrically connected to the contact pads through a plurality of traces. The first semiconductor die further include a plurality of second metal vias formed through an active area of the die. A second semiconductor die is disposed adjacent to the first semiconductor die and is electrically connected to the first semiconductor die through the first and second

metal vias.

Brief Description of the Drawings

FIGs. 1a–1b illustrate top and side views of a semiconductor wafer having a plurality of die separated by saw street guides;

FIGs. 2a–2b illustrate top and side views of the semiconductor wafer with trenches formed in the saw street guides;

FIGs. 3a–3b illustrate top and side views of expanding the saw street guides;

FIGs. 4a–4b illustrate top and side views of the expanded saw streets filled with organic material;

FIGs. 5a–5b illustrate top and side views of forming via holes through the organic material in the saw streets and via holes in an active area of the die;

FIGs. 6a–6b illustrate top and side views of depositing conductive material in the via holes;

FIGs. 7a–7b illustrate top and side views of cutting the metal vias on the saw streets into two half-circle vias;

FIGs. 8a–8b illustrate top and side views of a semiconductor die with metal vias formed along the saw streets and metal vias formed in the active area of the die;

FIGs. 9a–9b illustrate top and side views of a semiconductor die with redistribution layers formed on a backside of the die;

FIGs. 10a–10b illustrate top and side views of two side-by-side metal vias formed along the saw streets;

FIGs. 11a–11b illustrate top and side views of cutting the organic material between the two side-by-side

metal vias to separate the die;

FIGs. 12a–12b illustrate top and side views of a semiconductor die with full-circle vias along the saw streets and vias formed in the active area of the die;

FIG. 13 illustrates die-to-die stacking using direct metal-to-metal via bonding;

FIG. 14 illustrates die-to-die stacking using via bonding with solder paste;

FIG. 15 illustrates the semiconductor die with metal vias connected to a second die with wire bonds;

FIG. 16 illustrates the semiconductor die with metal vias connected to a second die with bond wires and solder bumps;

FIG. 17 illustrates another embodiment of interconnecting die using metal vias on saw streets and metal vias in the active area of the die; and

FIG. 18 illustrates another embodiment of interconnecting die using metal vias on saw streets and metal vias in the active area of the die.

Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the Figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each die contains hundreds or thousands of transistors and other active and passive devices performing one or more electrical functions. For a given wafer, each die from the wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and/or environmental isolation.

A semiconductor wafer generally includes an active front side surface having semiconductor devices disposed thereon, and a backside surface formed with bulk semiconductor material, e.g., silicon. The active front side surface contains a plurality of semiconductor die. The active surface is formed by a variety of semiconductor processes, including layering, patterning, doping, and heat treatment. In the layering process, semiconductor materials are grown or deposited on the substrate by techniques involving thermal oxidation, nitridation, chemical vapor deposition, evaporation, and sputtering. Patterning involves the use of photolithography to mask areas of the surface and etch away undesired material to form specific structures. The doping process injects concentrations of dopant material by thermal diffusion or ion implantation. The active surface is substantially planar and uniform with electrical interconnects, such as bond pads.

Flip chip semiconductor packages and wafer level chip scale packages (WLP) are commonly used with integrated

circuits (ICs) demanding high speed, high density, and greater pin count. Flip chip style packaging involves mounting an active area of the die facedown toward a chip carrier substrate or printed circuit board (PCB). The active area contains active and passive devices, conductive layers, and dielectric layers according to the electrical design of the die. The electrical and mechanical interconnect is achieved through a solder bump structure comprising a large number of individual conductive solder bumps or balls. The solder bumps are formed on the bump pads which are disposed on the active area. The bump pads connect to the active circuits by conduction tracks or traces in the active area. The solder bumps are electrically and mechanically connected to the contact pads on the carrier substrate by a solder reflow process. The flip chip semiconductor package provides a short electrical conduction path from the active devices on the die to conduction tracks on the carrier substrate in order to reduce signal propagation, lower capacitance, and achieve overall better circuit performance.

In the present discussion, a WLP is provided having through-hole vias (THV) formed along saw streets. The backside of the wafer has redistribution layers (RDL) for interconnect flexibility separated by repassivation layers. WLP with THV formed along saw streets are described in U.S. Patent Application Serial No. 11/744,657, entitled "Through-Hole Via on Saw Streets", and further in U.S. Patent Application Serial No. 11/768,844, entitled "Package on Package Using Through-Hole Via Die on Saw Streets", which are incorporated herein by reference.

Turning to FIG. 1a, a semiconductor wafer 30 is shown having a plurality of die 32. The die are separated by inter die wafer area 36, commonly known as saw street

guides. The saw street guides are routed around the wafer such that there is a saw street on every side of each die on the wafer, i.e., around a perimeter of the die. Each die 32 has a plurality to contact pads 38 formed on silicon, i.e., formed in an active area of die 32 and not in saw street guides 36. Contact pads 38 are made of aluminum, copper, or aluminum/copper alloys. Contact pads 38 electrically connect to active and passive devices through conduction tracks or layers formed on die 32. The contact pads can be disposed side-by-side a first distance from the edge of the die, as shown in FIG. 1a. Alternately, the contact pads can be offset in multiple rows such that a first row of contact pads are disposed a first distance from the edge of the die, and a second row of contact pads alternating with the first row are disposed a second distance from the edge of the die. A solder bump or wire bond will later be formed to connect to each metal contact pad for electrical and mechanical interconnect to a chip carrier substrate or printed circuit board (PCB).

FIG. 1b is a cross-sectional view of wafer 30, taken along line 1b-1b in FIG. 1a, showing die 32 separated by saw street guides 36. In one embodiment, die 32 may have dimensions ranging from 2x2 millimeters (mm) to 15x15 mm. The saw streets provide cutting areas to singulate the wafer into individual die. A first die 32 is disposed to the left of the leftmost saw street 36. A second die 32 is disposed between the saw streets 36. A third die 32 is disposed to the right of the rightmost saw street 36. Once the wafer is singulated, each set of contact pads disposed on the respective die will provide the electrical and mechanical interconnect for that die.

In FIG. 2a, semiconductor wafer 30 is again shown with its plurality of die 32, separated by saw street

guides 36. Dicing tape 40 is applied to the back of semiconductor wafer 30 for structural support of the wafer during the following manufacturing operations, as shown in FIG. 2b which is a cross-sectional view taken along line 2b-2b. Saw streets 36 are cut by cutting tool 44. In one embodiment, cutting tool 44 can be a saw or laser. Note that the cutting tool completely severs through wafer 30 to form a well or trench 42. The bottom of trench 42 is defined by dicing tape 40. The formation of trench 42 arises from a first singulation of wafer 30, which creates a trench width that is less than a width of the channel of saw street guide 36.

In FIG. 3a, semiconductor wafer 30 is shown with its plurality of die 32, separated by cut saw street guides 36. Wafer 30 undergoes a wafer expansion step to increase the width of saw street guides 36. FIG. 3b is a cross-sectional view of wafer 30, taken along line 3b-3b, showing the die being pulled using a wafer expansion table as shown by directional arrows 46. Alternately, the die can be picked and placed onto a wafer support system. In any case, the die are positioned farther apart following the steps of FIGs. 3a-3b to create wider saw street guides. In one embodiment, the die separation increases from 50 micrometers (μm) to 200 μm. The expanded dimension depends on the design embodiment, i.e. half via, full via, single row via, or double/multiple row via.

In FIG. 4a, semiconductor wafer 30 is shown with its plurality of die 32, separated by cut saw street guides 36. Organic material 48 is deposited in trench 42 by spin-coating or needle dispensing. Organic material 48 can be benzocyclobutene (BCB), polyimide (PI), or acrylic resin. FIG. 4b is a cross-sectional view of wafer 30, taken along line 4b-4b, showing organic material 48 deposited in trench

42. Organic material 48 fills trench 42 from dicing tape 40 up to the top surface of die 32. The backside of wafer 30 is transferred onto wafer support system 49, which is made from glass, silicon substrate, or other wafer support material.

In FIG. 5a, semiconductor wafer 30 is shown with its plurality of die 32, separated by saw street guides 36 filled with organic material 48. A via hole 50 is cut into organic material 48 along saw streets 36. The via cutting operation uses a laser drill or etching process. Via holes 50 are placed along die 32 adjacent to contact pads 38. In one embodiment, contact pads 38 and via holes 50 have a minimum separation distance of about 20 µm to 150 µm, depending on the diameter and depth of the via.

In FIG. 5b, the cross-sectional view of wafer 30, taken along line 5b-5b, shows via holes 50 cut into organic material 48 down to wafer support system 49. The laser drilling operation is centered about the channel of the saw street guide and makes a hole having a diameter less than the width of trench 42, which leaves a layer of organic material 48 surrounding via hole 50. The width of trench 42 is dependent on the width of saw street width, but typically smaller than the saw street width. The diameter of via hole 50 is typically about 10 µm to 100 µm, depending on the required via depth. In addition, via holes 53 are cut through contact pads 38 down through wafer 30 to wafer support system 49. The laser drilling operation is centered about contact pad 38 and makes a hole having a diameter less than the width of the contact pad, which leaves part of the contact pad surrounding via hole 53 at the top of die 32. Note that via holes 53 are formed on silicon, i.e., through an active area of die 32.

A metal track or trace 52 is routed from each contact

pad 38 to the corresponding via hole 50. Trace 52 is formed by a metal patterning process to connect contact pads 38 to via holes 50, which will be filled with conductive material in a later step. Traces 52 are provided for each contact pad and via hole pairing as shown. Some via holes 50 are dummy vias performing no electrical function. Accordingly, metal trace 52 need not be routed to every via depending on the device function.

In FIG. 6a, semiconductor wafer 30 is shown with its plurality of die 32, separated by saw street guides 36 with metal-filled vias 54 and 56. A conductive material is deposited into via holes 50 through a deposition process such as plating or plugging to form metal vias 54. The same conductive material is also deposited into via holes 53 to form metal vias 56. Metal vias 56 are formed through an active area of die 32. The conductive material can be copper (Cu), aluminum (Al), tungsten (W), or alloys thereof, or mixtures of other conductive materials. Metal vias 54 are formed in and are surrounded by organic material 48. Metal vias 56 are formed in and are surrounded by contact pad 38 and the active area of wafer 30. Metal via 54 electrically connects to contact pad 38 by way of trace 52. Traces 52 are provided for each contact pad and metal via pairing as shown. FIG. 6b is a cross-sectional view of wafer 30, taken along line 6b-6b, showing metal vias 54 electrically connecting to contact pads 38 through traces 52, and metal vias 56 electrically connecting to contact pads 38 directly. Wafer support system 49 is replaced with dicing tape 58 for structural support of the wafer during the second or final singulation to separate die 32. The bottom of metal vias 54 and 56 coincides with dicing tape 58.

A redistribution layer (RDL) can be formed on the

backside of wafer 30. The backside RDL operates as an intermediate conductive layer to route electrical signals to various areas of the die, including active and passive circuits, and provides various electrical interconnect options during package integration, such as shown in FIGs. 15-18. A repassivation layer is formed between the individual nodes of the backside RDL for electrical isolation. The formation of backside RDL and repassivation layer is disclosed in U.S. Patent Application No. (Pending), Attorney Docket No. 125155.00033, entitled "Semiconductor Wafer having Through Hole Vias on Saw Streets with backside redistribution layer."

In FIGs. 7a-7b, metal vias 54 are cut through center area 68 by cutting tool 70. In one embodiment, cutting tool 70 can be a saw or laser. The cut extends down to dicing tape 58 to completely sever metal vias 54 into two equal half-circle vias 64. A pick and place operation removes die 32 as individual units from dicing tape 58.

In FIG. 8a, semiconductor die 32 is shown with both metal vias 64 on saw streets and through silicon metal vias 56. FIG. 8b is a cross-sectional view of die 32, taken along line 8b-8b, showing metal vias formed through silicon of die 32 and metal vias on saw street configuration, as produced by the manufacturing steps of FIGs. 1-7.

In FIG. 9a, semiconductor die 32 is shown with through silicon metal vias 56 and further metal vias 64 on saw streets. FIG. 9b is a cross-sectional view of die 32, taken along line 9b-9b, showing metal vias formed through silicon of die 32 and metal vias on saw street configuration, as produced by the manufacturing steps of FIGs. 1-7. RDL 74 and repassivation layer 76 are shown on the backside of die 32. RDL 74 can be made with nickel (Ni), nickel vanadium (NiV), Cu, or Cu alloy. RDL 74

operates as an intermediate conductive layer to route electrical signals to various areas of the die, including active and passive circuits, and provides various electrical interconnect options during package integration, such as shown in FIGs. 15–18. Repassivation layer 76 is formed between the individual nodes of backside RDL 74 for electrical isolation. The repassivation layer can be made with silicon nitride (SiN), silicon dioxide (SiO2), silicon oxynitride (SiON), polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), or other insulating material.

In FIG. 10a, semiconductor die 32 is shown with contact pads 38 connected to metal vias 80 by traces 52. FIG. 10b is a cross-sectional view of die 32, taken along line 10b–10b, showing metal vias 80 along saw street 36. The metal via is produced by the steps described in FIGs. 1–7, with the exception that two via holes like 50 are formed side-by-side in organic material 48. The side-by-side via holes 50 are separated by organic material 48. Conductive traces 52 connect contact pads 38 and via holes 50. The side-by-side via holes are filled with conductive material to form metal vias 80.

In FIG. 11a, semiconductor die 32 is shown with contact pads 38 connected to metal vias 80 by traces 52. Dicing tape is applied to the back of semiconductor wafer 30 for structural support of the wafer during the final singulation to separate die 32, as shown in FIG. 11b which is a cross-sectional view taken along line 11b–11b. The second or final singulation to separate the plurality of die 32 is cut through organic material 48 along line 82 between the side-by-side vias 80 with a cutting tool like 70. The singulation between metal vias 80 results in the metal vias on saw street configuration in combination with through silicon vias 56.

In FIG. 12a, semiconductor die 32 is shown with contact pads 38 connected to metal vias 80 by traces 52. FIG. 12b is a cross-sectional view of die 32, taken along line 12b-12b, showing metal vias on saw street configuration. The metal full-circle vias are produced by the steps described in FIGs. 1-7 and 10-11. The side-by-side via holes like 50 are separated by organic material 48. Conductive traces like 52 electrically connect the contact pads and via holes. The side-by-side via holes are filled with conductive material to form metal vias 80. The final singulation to separate the plurality of die 32 is cut through organic material 48 between the side-by-side metal vias 80 resulting in the metal via on saw street configuration in combination with through silicon vias 56.

FIG. 13 illustrates direct die-to-die stacking using direct via metal bonding. A plurality of die 32 is stacked as shown to suit a particular application. Each of the metal half-vias 64 and through silicon vias 56 can be joined together as shown by union 90 using a direct via metal bonding process. The combination of vias 64 and 56 provide greater interconnect flexibility and options for electrically connecting the stacked die 32. Alternately, semiconductor die 32 with metal full-vias 80 and through silicon vias 56 can be joined together by union 90 using a direct via metal bonding process.

FIG. 14 illustrates die-to-die stacking using via bonding with solder paste 92. A plurality of die 32 is stacked as shown to suit a particular application. Each of the metal vias 64 and through silicon vias 56 can be joined together as shown by reflowing solder paste 92 to create a strong metallurgical bond between each of stacked die 32. The combination of vias 64 and 56 provide greater interconnect flexibility and options for electrically

connecting the stacked die 32. Alternately, semiconductor die 32 with metal vias 80 and through silicon vias 56 can be joined together by solder paste 92 using a reflow process.

In FIGs. 15–18 shows various packaging applications using, in part, an interconnect technique with the THVs formed on saw streets and THVs on silicon. FIG. 15 has semiconductor die 100 attached to die 32 with adhesive 102. Die 100 electrically connects through wire bonds 104 to metal vias 64 on die 32. Die 32 is supported by substrate 106. Metal vias 64 and 56 electrically connect to solder bumps 108 through conductive layer 110. The packages are sealed by epoxy encapsulant 112.

FIG. 16 shows semiconductor die 120 attached to die 122 with adhesive 124. Die 120 electrically connects through wire bonds 126 to metal vias 64 on die 32. Die 122 electrically connects through solder bumps 128 to metal vias 56 on die 32. Die 32 is supported by substrate 130. Metal vias 64 and 56 electrically connect to solder bumps 132 through conductive layer 134. The packages are sealed by epoxy encapsulant 136.

FIG. 17 shows semiconductor die 140 electrically connected to metal vias 64 or 80 on die 32 by way of bond wires 152. Semiconductor die 154 electrically connects to metal vias 64 and 56 on die 32 by way of wire bonds 156 and conductive layer 158. Die 32 and 140 are supported by substrate 160. The entire assembly is mounted to substrate 161. Wire bonds 162 from substrate 160 provide the electrical connection to solder bumps 164 through conductive layer 166. The packages are encased by epoxy encapsulant 168. Molding compound 170 encapsulates die 154.

FIG. 18 shows semiconductor die 180 electrically

connected to die 32 with solder bumps 182. Passive devices 184 also connect to metal vias 64 with solder paste 186. Die 32 is mounted to a semiconductor package containing die 190 with adhesive 192. Die 190 electrically connects to solder bumps 200 through wire bonds 194, conductive layer 196, and conductive layer 198. The assembly of semiconductor die 32, 180, and 190 are supported by substrate 202. Metal vias 56 electrically connect to solder bumps 200 through wire bonds 204 and conductive layer 198. The packages are sealed by epoxy encapsulant 206. An underfill material 208 provides stress relief.

In summary, stackable semiconductor die has been described with THVs formed in the saw streets and THVs formed on silicon. The electrical interconnect is accomplished using the THVs on saw streets and THVs on silicon, in addition to a redistribution layer, separated by a repassivation layer, to increase signal routing options and density. The THVs on saw streets and THVs on silicon, in addition to the RDLs, provide more signal routing functionality and flexibility within the package.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims

Claims

What is claimed:

1. A semiconductor wafer, comprising:

a plurality of die with contact pads disposed on a first surface of an active area of each die, the semiconductor wafer having saw street guides between each die;

a plurality of first metal vias formed in the saw street guides and surrounded by organic material;

a plurality of second metal vias formed in the active area of the die; and

a plurality of traces connecting the contact pads and first metal vias.

2. The semiconductor wafer of claim 1, further including:

a plurality of redistribution layers (RDL) formed on a second surface of the die opposite the first surface; and

a plurality of repassivation layers formed between the RDL on the second surface of the die.

3. The semiconductor wafer of claim 1, wherein the die are stackable and connected by the first and second metal vias when stacked.

4. The semiconductor wafer of claim 1, wherein at least one metal via is formed between the contact pads on adjacent die.

5. The semiconductor wafer of claim 4, wherein the semiconductor wafer is singulated through the at least one metal via to form metal vias electrically connected to the contact pads by the traces.

6. The semiconductor wafer of claim 1, wherein two metal vias are formed side by side between the contact pads on adjacent die.

7. The semiconductor wafer of claim 6, wherein the semiconductor wafer is singulated along the saw street guides between the two metal vias to form metal vias electrically connected to the contact pads by the traces.

8. The semiconductor wafer of claim 1, further including solder bumps electrically connected to the RDL.

9. A semiconductor package, comprising:

a plurality of stacked die, each die including

(a) a plurality of contact pads disposed on a first surface of an active area of the die,

(b) a plurality of first metal vias formed along a perimeter of the die,

(c) a plurality of second metal vias formed in the active area of the die, and

(d) a plurality of traces electrically connecting the first metal vias to the contact pads;

a plurality of redistribution layers (RDL) formed on a second surface of the die opposite the first surface; and

a plurality of repassivation layers formed between the RDL on the second surface of the die;

wherein the first and second metal vias provide electrical interconnect between the stacked die.

10. The semiconductor package of claim 9, wherein the semiconductor wafer is singulated through the at least one metal via to form metal vias electrically connected to the

contact pads by the traces.

11. The semiconductor package of claim 9, wherein two metal vias are formed side by side between the contact pads on adjacent die.

12. The semiconductor package of claim 11, wherein the semiconductor wafer is singulated along saw street guides between the two metal vias to form metal vias electrically connected to the contact pads by the traces.

13. A semiconductor package, comprising:

a first semiconductor die having contact pads and a plurality of first metal vias formed along a perimeter of the die electrically connected to the contact pads through a plurality of traces, the first semiconductor die further including a plurality of second metal vias formed through an active area of the die;

a second semiconductor die disposed adjacent to the first semiconductor die and electrically connected to the first semiconductor die through the first and second metal vias; and

bond wires electrically connecting the first and second semiconductor die.

14. The semiconductor package of claim 13, wherein two metal vias are formed side by side between the contact pads on an adjacent die.

15. The semiconductor package of claim 14, wherein the semiconductor wafer is singulated along saw street guides between the two metal vias to form metal vias electrically connected to the contact pads by the traces.