ABSTRACT

SEMICONDUCTOR FABRICATION PROCESS INCLUDING AN SiGe REWORK METHOD

A method for fabricating a semiconductor device includes forming an SiGe region. The SiGe region can be an embedded source and drain region, or a compressive SiGe channel layer, or other SiGe regions within a semiconductor device. The SiGe region is exposed to an SC1 solution and excess surface portions of the SiGe region are selectively removed. The SC1 etching process can be part of a rework method in which overgrowth regions of SiGe are selectively removed by exposing the SiGe to and SC1 solution maintained at an elevated temperature. The etching process is carried out for a period of time sufficient to remove excess surface portions of SiGe. The SC1 etching process can be carried out at elevated temperatures ranging from about 25ºC to about 65ºC.

FIG. 1