WHAT IS CLAIMED IS:

1. A memory system, comprising:

at least one non-volatile memory device in which a multi-level mapping table is stored, the multi-level mapping table being configured to implement mapping from a logical address to a physical address; and

a memory controller coupled to the at least one non-volatile memory device and including a buffer in which a portion of the multi-level mapping table is stored, the memory controller being configured to:

perform a random read operation on data stored in the memory device;

in response to a random read range being greater than or equal to a preset value, obtain a target buffer hit rate of a mapping table of the multi-level mapping table;

detect a current buffer hit rate of the mapping table of the multi-level mapping table; and

in response to the current buffer hit rate of the mapping table being lower than the target buffer hit rate of the mapping table of the multi-level mapping table, adjust capacity for storing different levels of mapping tables in the buffer.

2. The memory system of claim 1, wherein:

the multi-level mapping table comprises a first-level mapping table, a second-level mapping table, and a third-level mapping table,

a physical address of the second-level mapping table is stored in the first-level mapping table, a physical address of the third-level mapping table is stored in the second-level mapping table, a physical address of data is stored in the third-level mapping table, and

the whole first-level mapping table, a portion of the second-level mapping table, and a portion of the third-level mapping table are stored in the buffer.

3. The memory system of claim 2, wherein the memory controller is configured to:

in response to the random read range being greater than or equal to a preset value, increase a ratio of capacity for storing the second-level mapping table to total capacity for storing the second-level mapping table and the third-level mapping table in the buffer.

4. The memory system of claim 3, wherein the memory controller is further configured to:

increase the ratio of the capacity for storing the second-level mapping table to the total capacity for storing the second-level mapping table and the third-level mapping table in the buffer in response to the current buffer hit rate of the mapping table being lower than the target buffer hit rate of mapping table until the current buffer hit rate of mapping table is greater than or equal to the target buffer hit rate of mapping table.

5. The memory system of claim 4, wherein the memory controller is configured to:

determine a difference between the current buffer hit rate of mapping table and the target buffer hit rate of mapping table; and

determine increasing quantity of the capacity for storing the second-level mapping table in the buffer in this adjustment according to the difference,

wherein the increasing quantity is positively correlated with the difference.

6. The memory system of claim 4, wherein the memory controller is configured to:

in response to the current buffer hit rate of mapping table being lower than the target buffer hit rate of mapping table, and a ratio of current capacity for storing the second-level mapping table to the total capacity for storing the second-level mapping table and the third-level mapping table in the buffer reaching a preset ratio, stop adjusting the capacity for storing different levels of mapping tables in the buffer.

7. The memory system of claim 4, wherein the memory controller is configured to:

determine the target buffer hit rate of mapping table according to the random read range.

8. The memory system of claim 3, wherein the memory controller is configured to:

in response to the random read range being less than the preset value, maintain the capacity for storing the second-level mapping table and the capacity for storing the third-level mapping table in the buffer being unchanged.

9. The memory system of claim 3, wherein the memory controller is configured to:

determine the preset value according to a current capacity for storing the second-level mapping table in the buffer and in combination with mapping rules for various levels of mapping tables.

10. The memory system of claim 2, wherein the memory controller is configured to:

in response to the random read range being greater than or equal to a preset value, increase a total capacity for storing the second-level mapping table and the third-level mapping table in the buffer.

11. The memory system of claim 1, wherein:

the multi-level mapping table includes a first-level mapping table and a second-level mapping table,

a physical address of the second-level mapping table is stored in the first-level mapping table, a physical address of data is stored in the second-level mapping table, a portion of the first-level mapping table and a portion of the second-level mapping table are stored in the buffer, and

the memory controller is further configured to:

in response to the random read range being greater than or equal to a preset value, increase a ratio of the capacity for storing the first-level mapping table to a total capacity for storing the first-level mapping table and the second-level mapping table in the buffer.

12. The memory system of claim 1, wherein the memory system includes a dynamic random-access memory (DRAM)-less memory system and the buffer includes a static random access memory (SRAM).

13. The memory system of claim 1, wherein the memory system includes a flash storage and the memory device includes a NOT AND (NAND) memory.

14. A method of operating a memory system, comprising:

performing, by a memory controller coupled to at least one non-volatile memory device and including a buffer in which a portion of a multi-level mapping table is stored, a random read operation on data stored in the at least one non-volatile memory device in which a multi-

level mapping table is stored, the multi-level mapping table being configured to implement mapping from a logical address to a physical address;

in response to a random read range being greater than or equal to a preset value, obtaining, by the memory controller coupled to the at least one non-volatile memory device and including the buffer in which a portion of the multi-level mapping table is stored, a target buffer hit rate of a mapping table of the multi-level mapping table;

detecting, by the memory controller coupled to the at least one non-volatile memory device and including the buffer in which the portion of the multi-level mapping table is stored, a current buffer hit rate of the mapping table of the multi-level mapping table; and

in response to the current buffer hit rate of mapping table being lower than the target buffer hit rate of the mapping table of the multi-level mapping table, adjusting, by the memory controller coupled to the at least one non-volatile memory device and including the buffer in which the portion of the multi-level mapping table is stored, capacity for storing different levels of mapping tables in the buffer.

15. The method of claim 14, wherein:

the multi-level mapping table includes a first-level mapping table, a second-level mapping table, and a third-level mapping table,

a physical address of the second-level mapping table is stored in the first-level mapping table, a physical address of the third-level mapping table is stored in the second-level mapping table, and a physical address of data is stored in the third-level mapping table,

the whole first-level mapping table, a portion of the second-level mapping table, and a portion of the third-level mapping table are stored in the buffer, and

the method further comprises:

in response to a random read range corresponding to the random read operation meeting a preset condition, adjusting the capacity for storing different levels of mapping tables in the buffer; and

in response to the random read range being greater than or equal to a preset value, increasing a ratio of the capacity for storing the second-level mapping table to a total capacity for storing the second-level mapping table and the third-level mapping table in the buffer.

16. The method of claim 15, further comprising:

in response to the random read range being greater than or equal to a preset value, increasing the ratio of the capacity for storing the second-level mapping table to the total capacity for storing the second-level mapping table and the third-level mapping table in the buffer; and

increasing the ratio of the capacity for storing the second-level mapping table to the total capacity for storing the second-level mapping table and the third-level mapping table in the buffer in response to the current buffer hit rate of the mapping table being lower than the target buffer hit rate of mapping table until the current buffer hit rate of mapping table is greater than or equal to the target buffer hit rate of mapping table.

17. The method of claim 16, further comprising:

determining a difference between the current buffer hit rate of mapping table and the target buffer hit rate of mapping table; and

according to the difference, determining increasing quantity of the capacity for storing the second-level mapping table in the buffer in this adjustment,

wherein the increasing quantity is positively correlated with the difference.

18. The method of claim 16, further comprising:

in response to the current buffer hit rate of mapping table being lower than the target buffer hit rate of mapping table, and the ratio of a current capacity for storing the second-level mapping table to the total capacity for storing the second-level mapping table and the third-level mapping table in the buffer reaching a preset ratio, stopping adjusting the capacity for storing different levels of mapping tables in the buffer.

19. A memory controller, comprising:

a buffer configured to:

store a portion of a multi-level mapping table in a non-volatile memory device, the multi-level mapping table being configured to implement mapping from a logical address to a physical address; and

a control component configured to:

perform a random read operation on data stored in the non-volatile memory device; in response to a random read range being greater than or equal to a preset value, obtain a target buffer hit rate of a mapping table of the multi-level mapping table;

detect a current buffer hit rate of the mapping table of the multi-level mapping table; and

in response to the current buffer hit rate of the mapping table being lower than the target buffer hit rate of the mapping table of the multi-level mapping table, adjust a capacity for storing different levels of mapping tables in the buffer.

20. The memory controller of claim 19, further including:

a flash translation layer, which connects the control component and the buffer and is configured to:

translate the logical address into a corresponding physical address according to mapping information in the multi-level mapping table stored in the buffer.