

FIG. 1

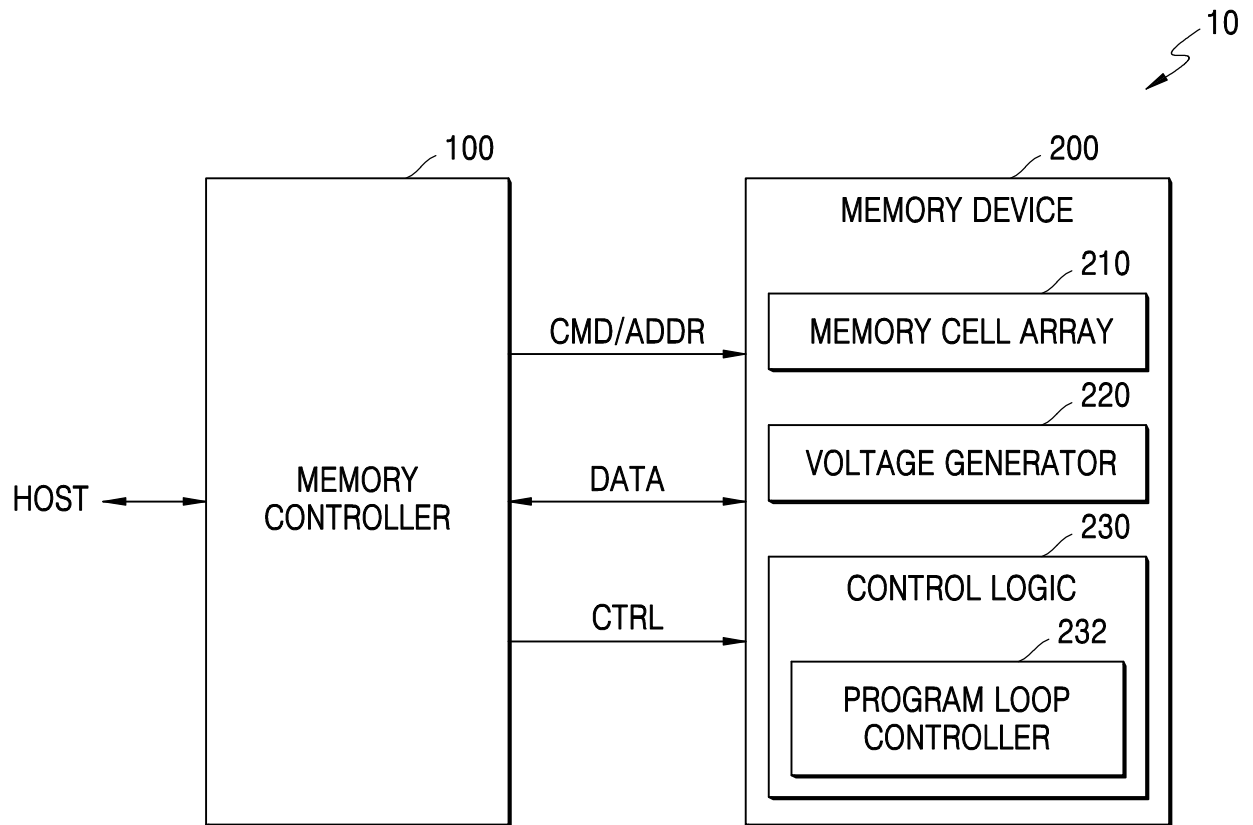


FIG. 2

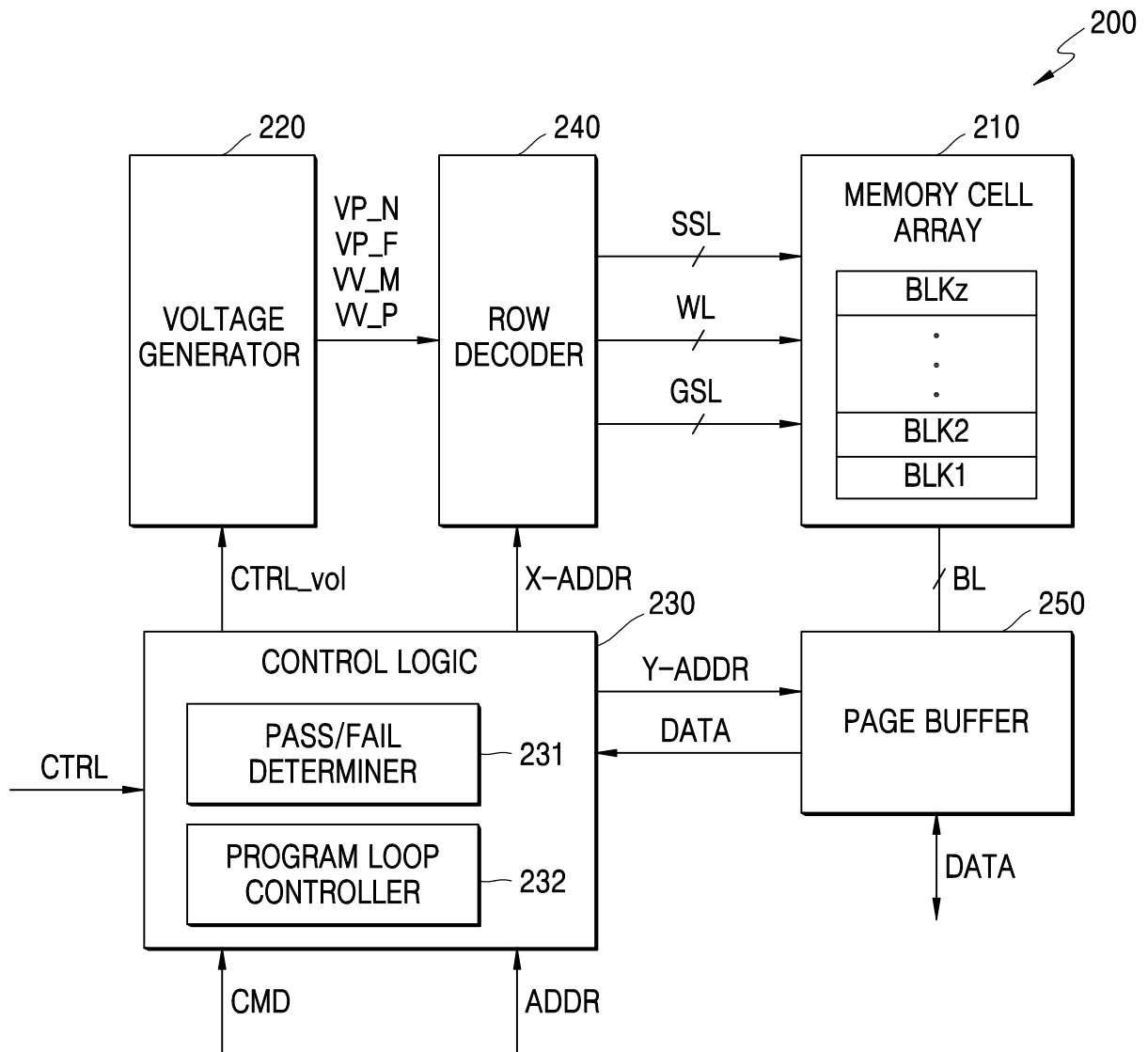


FIG. 3

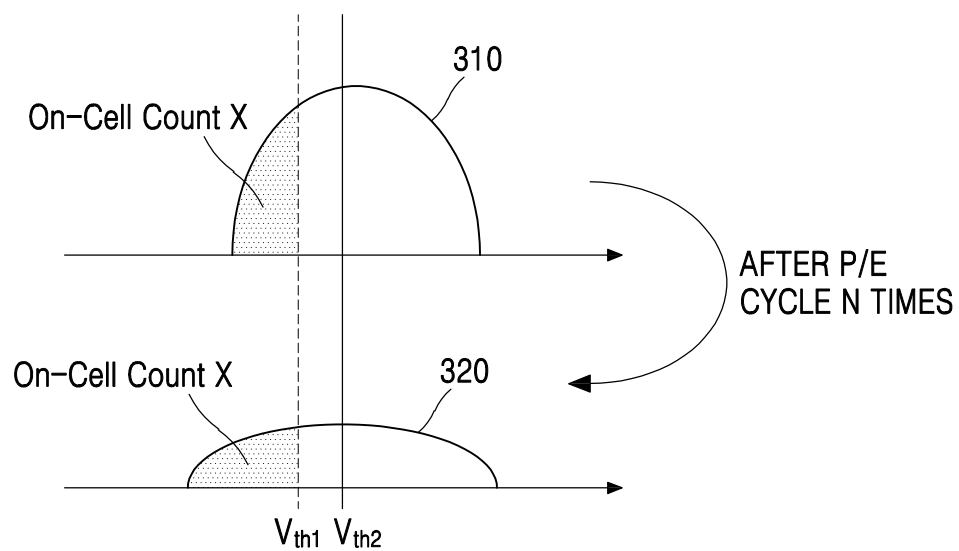


FIG. 4

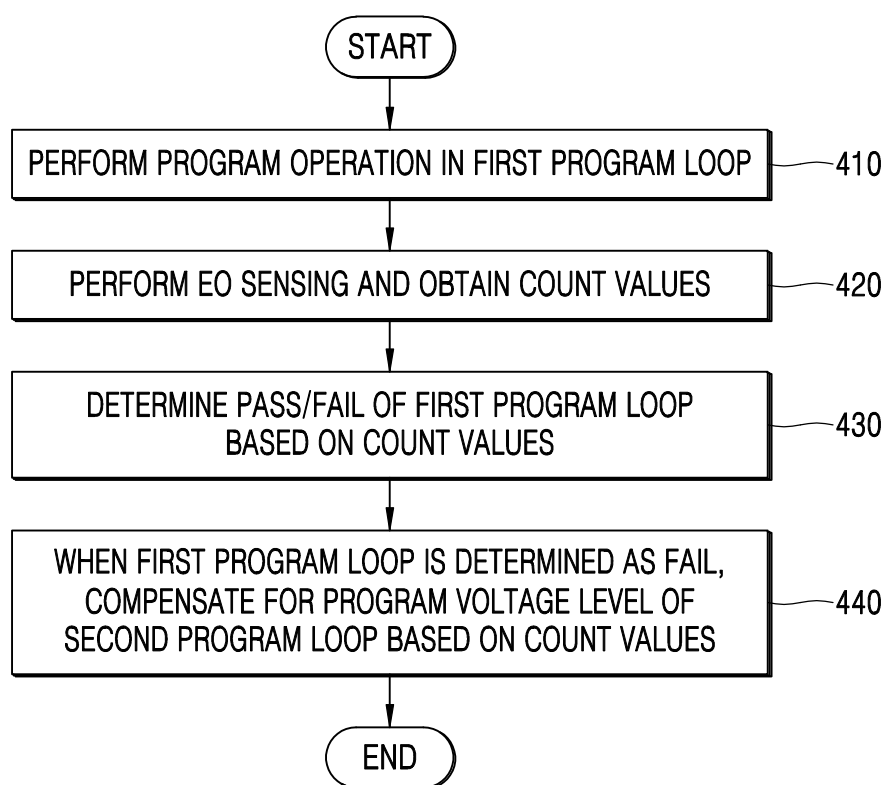


FIG. 5A

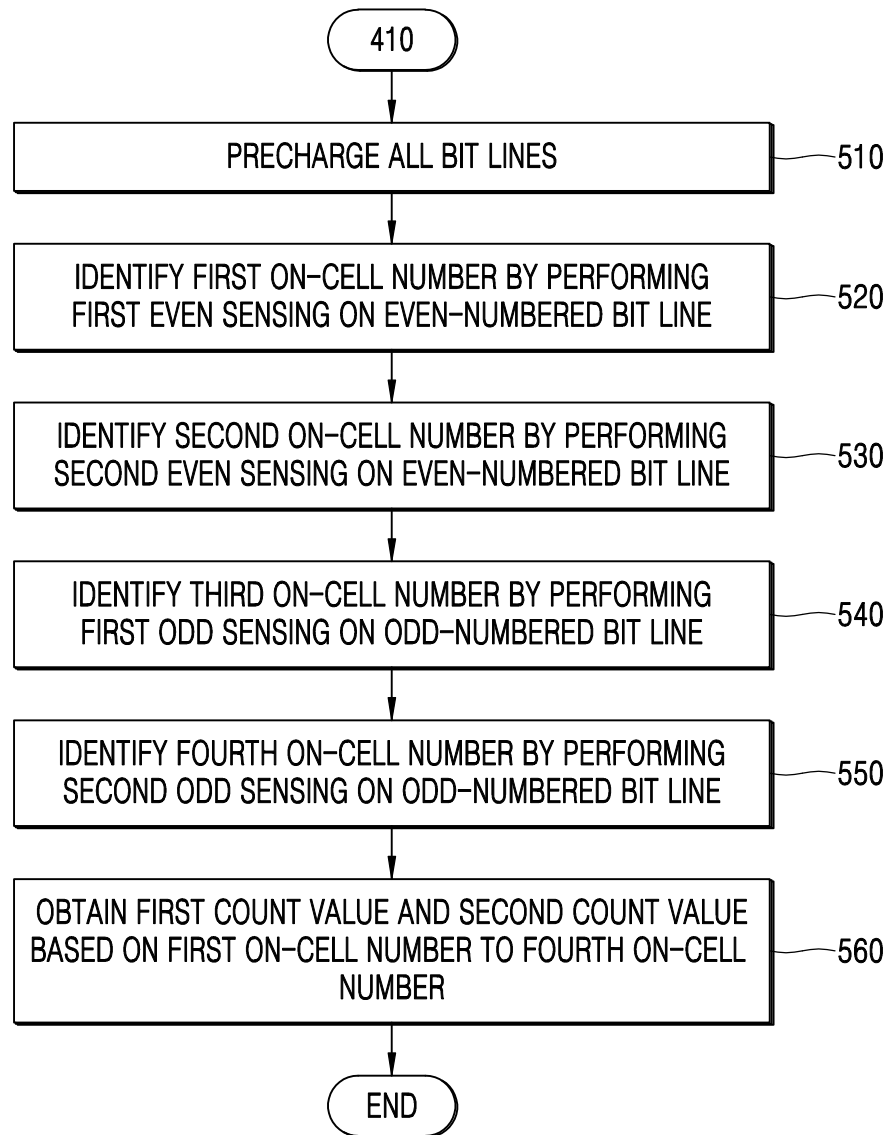


FIG. 5B

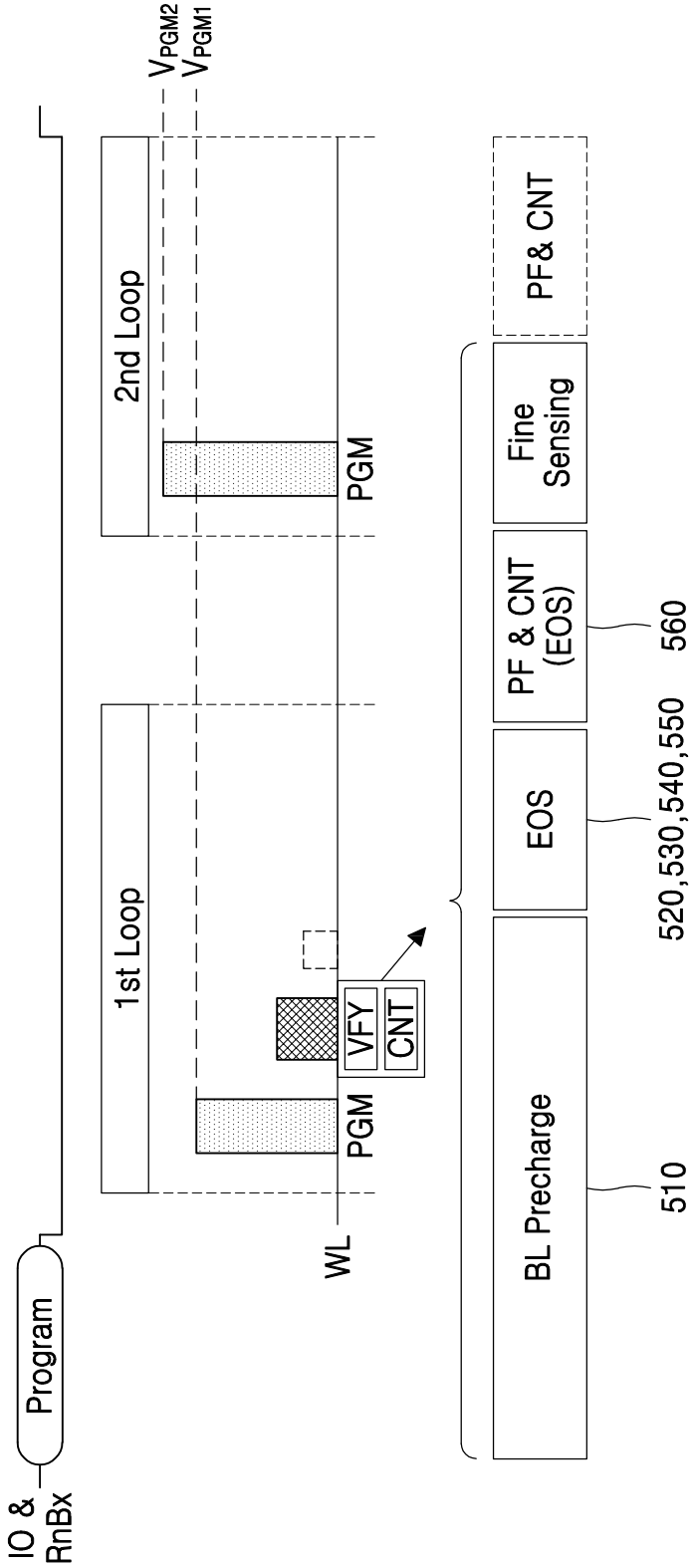


FIG. 6A

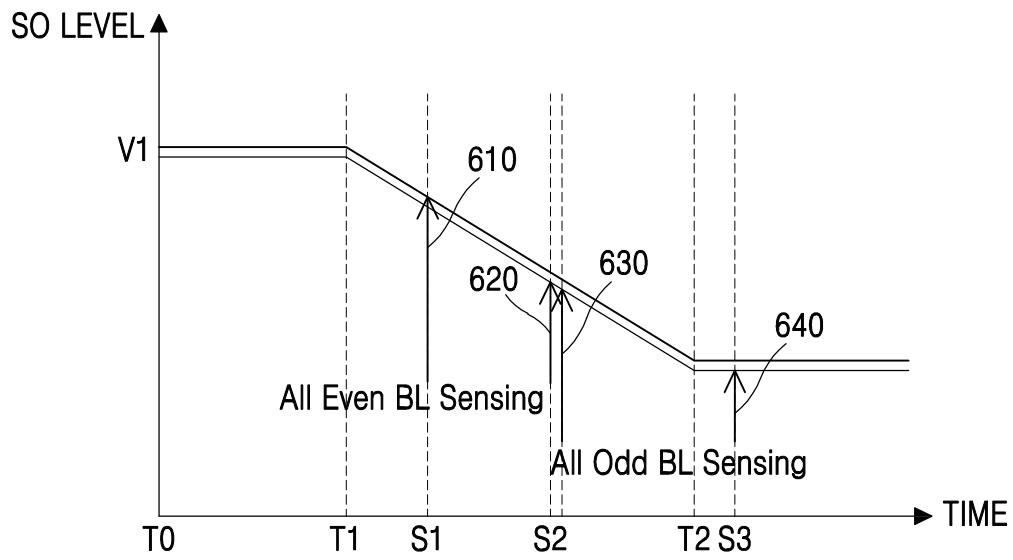


FIG. 6B

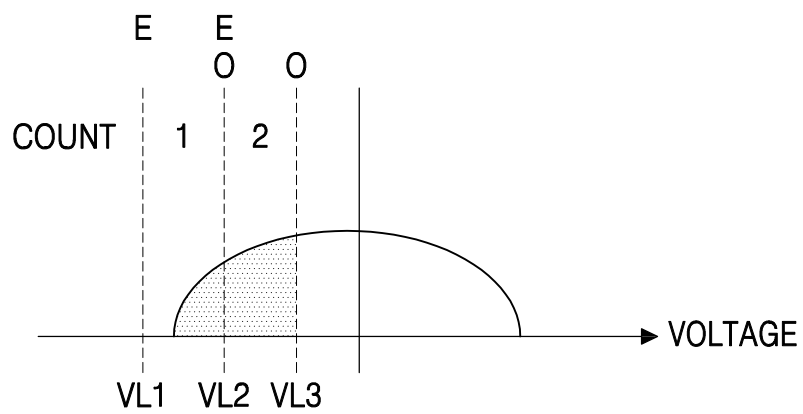


FIG. 7

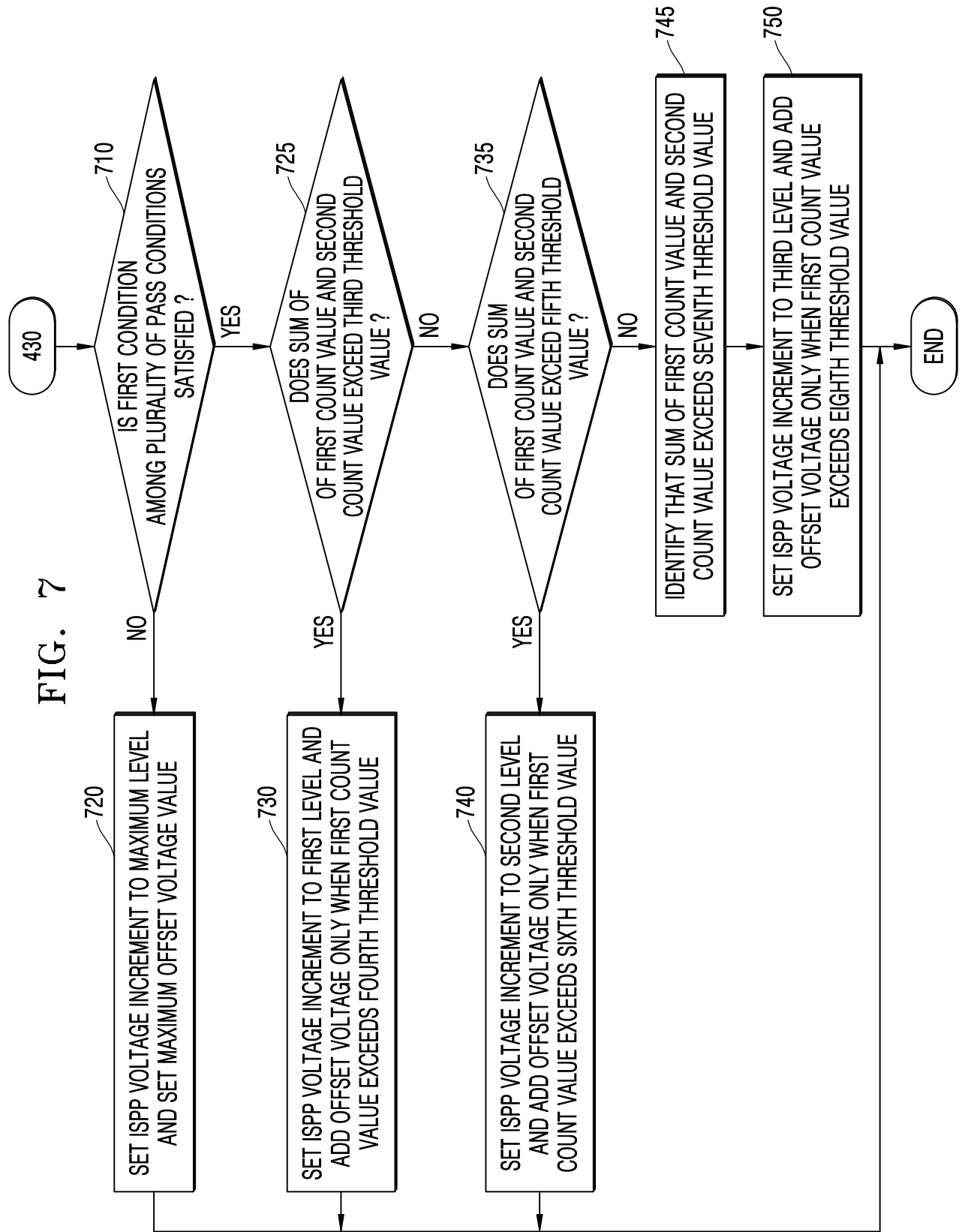


FIG. 8

FIRST CONDITION	SECOND CONDITION	THIRD CONDITION	COMPENSATION OF PROGRAM VOLTAGE LEVEL
Y>X	X+Y>300bit	X < 90bit	500(ISPP) + 0(Offset) [mV]
		X > 90bit	500(ISPP) + 50(Offset) [mV]
	X+Y>200bit	X < 60bit	400(ISPP) + 0(Offset) [mV]
		X > 60bit	400(ISPP) + 50(Offset) [mV]
	X+Y>100bit	X < 30bit	300(ISPP) + 0(Offset) [mV]
		X > 30bit	300(ISPP) + 50(Offset) [mV]
Y<X	Don't Care	Don't Care	ISPP Max + 600 [mV]

FIG. 9

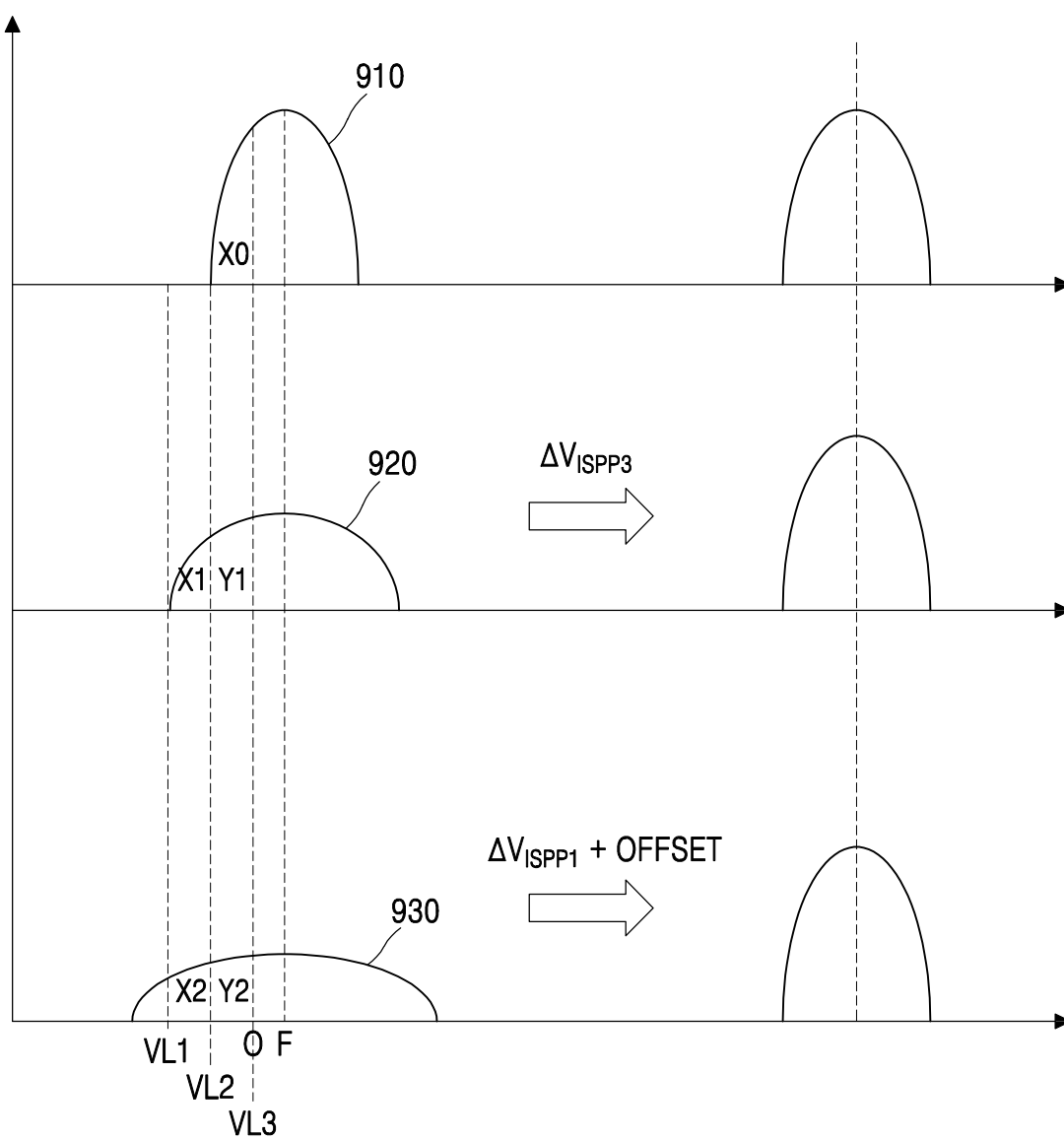


FIG. 10A

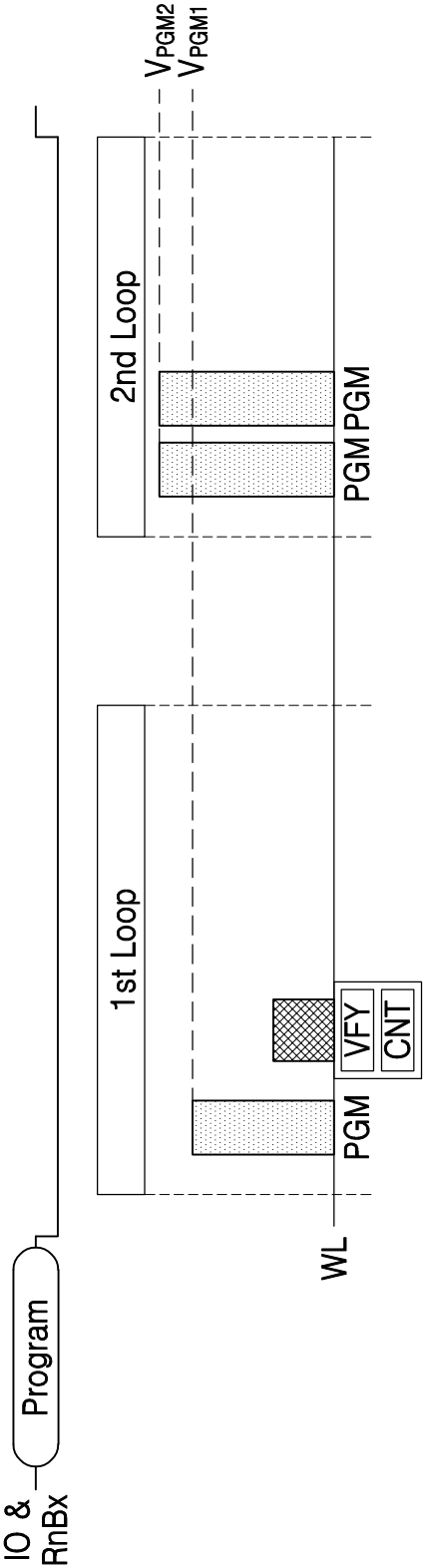


FIG. 10B

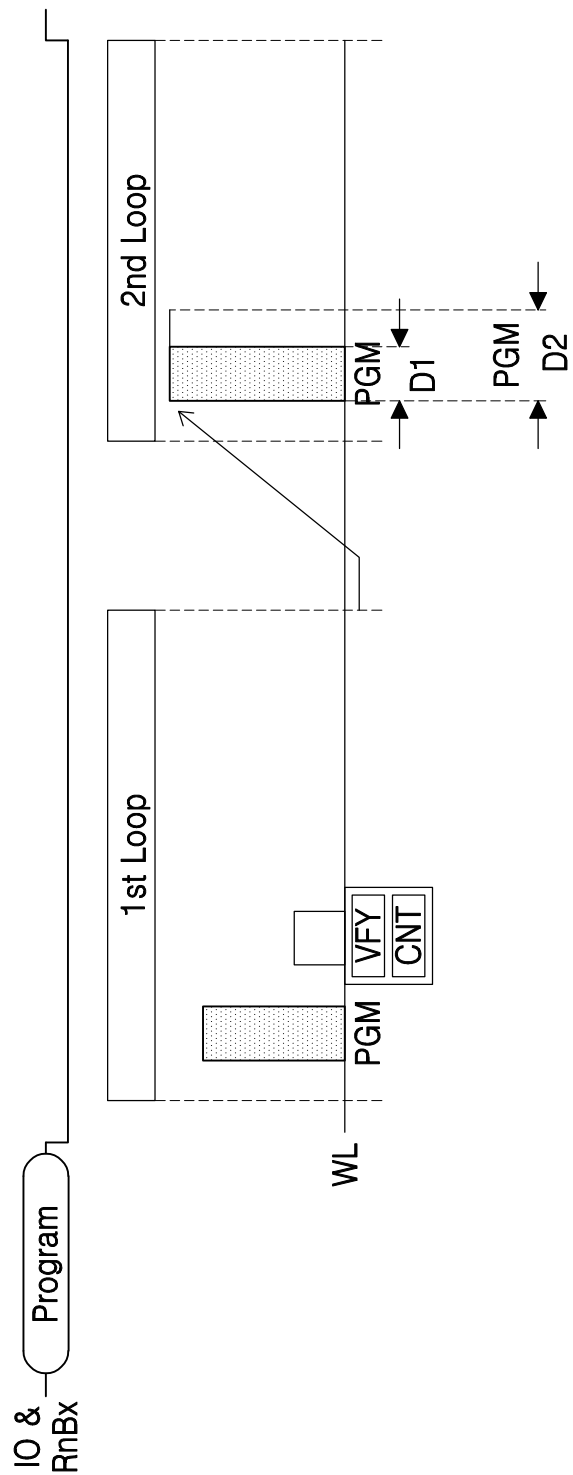


FIG. 11

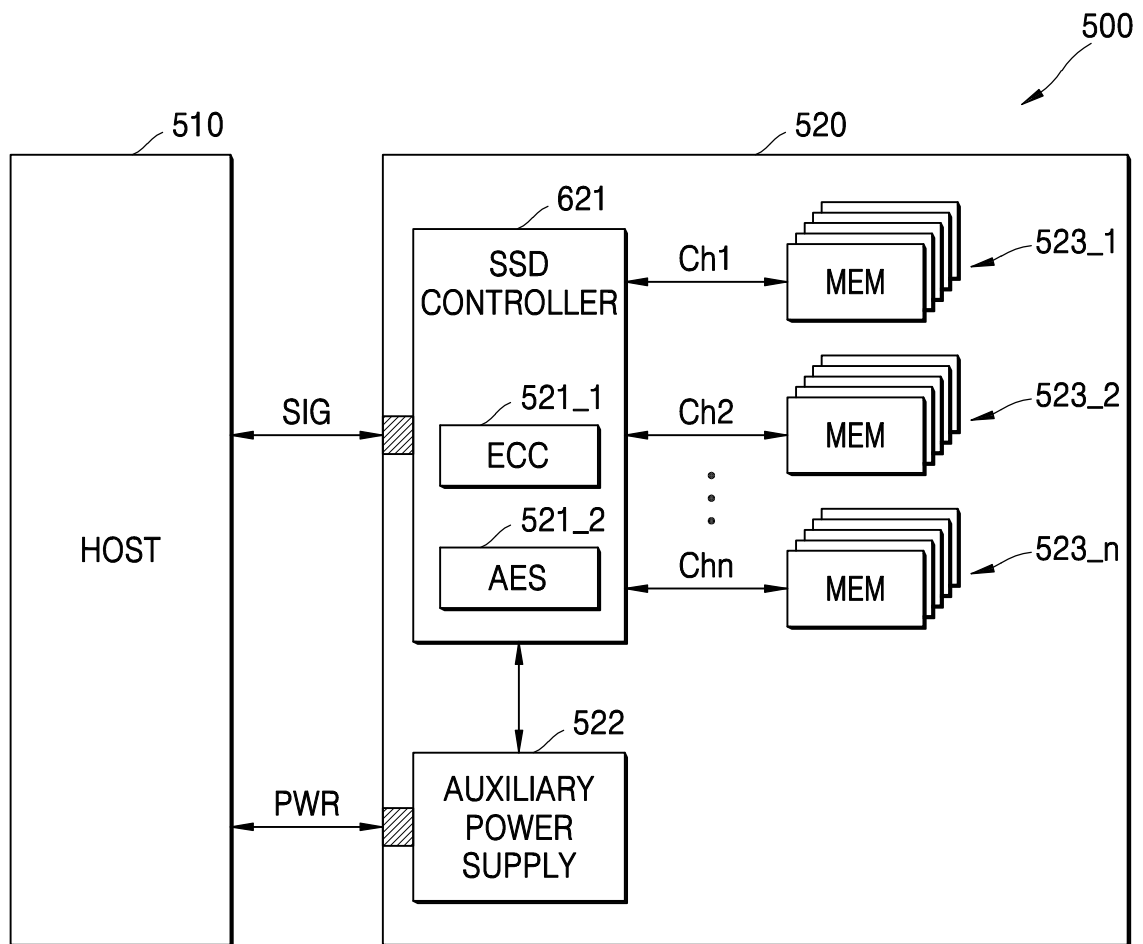
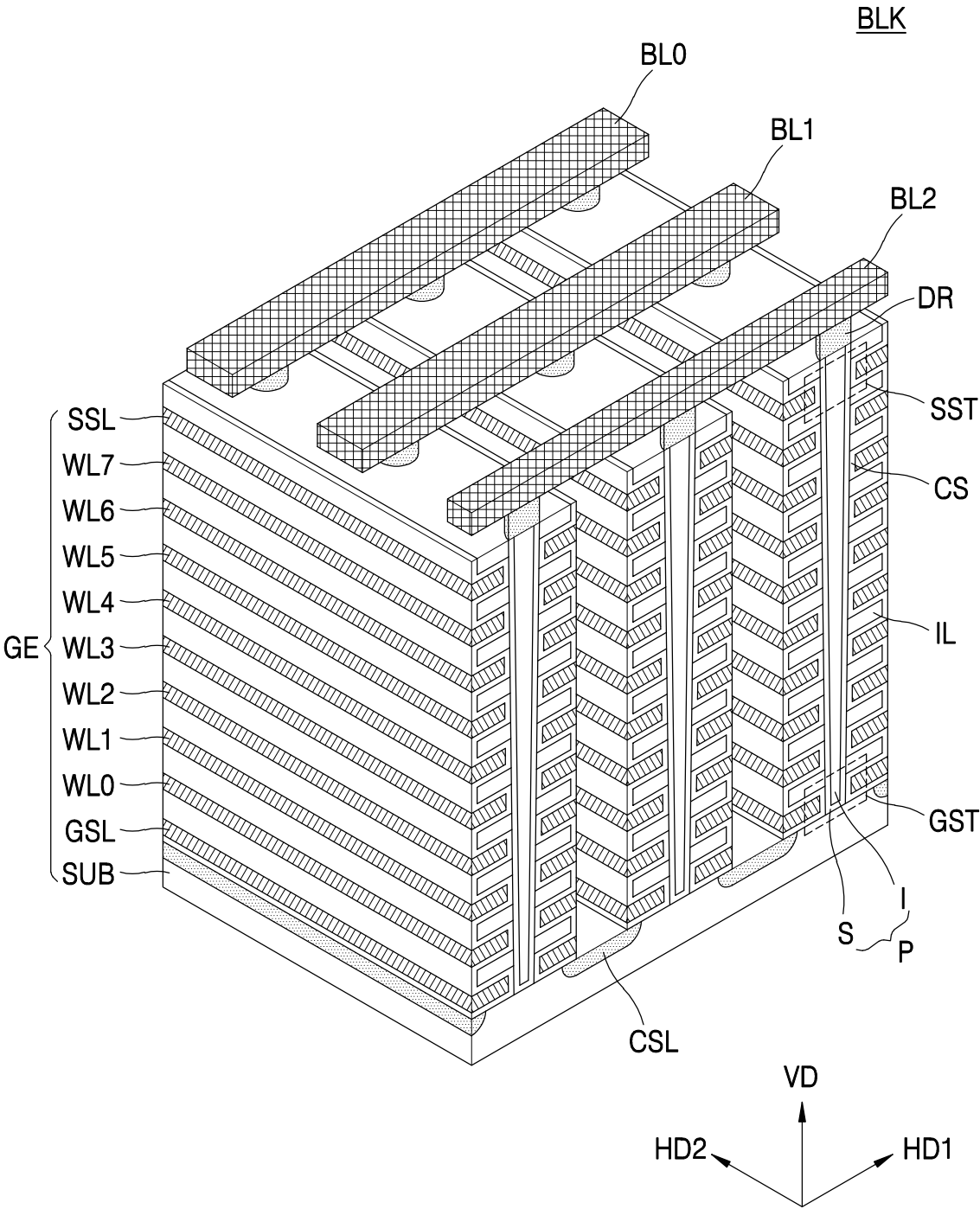


FIG. 12



600