

Power supply control system and device

Field of the invention

The present invention relates to a power supply control system and device using
5 single cycle control for power sources such as for lights, and more particularly, to
switch mode power supplies (SMPS) but not limited to such.

Background to the invention

A power supply often has an inverter or converter device for the conversion of
10 available power of one set of characteristics to another set of characteristics to meet
specified requirements. It can therefore be a circuit that provides power with the
characteristics required by the load from a mains supply power source. For example
a mains supply power source might be the 50 Hertz, single phase, 240 Volt AC
power found in Australia but the load can be a circuit in a personal computer that
15 requires regulated 5V DC power. Alternatively the load could be a 20 Watt Halogen
light supply. The power supply therefore requires a circuit that makes the 240 V AC
power source and 5 V DC load compatible.

A switching-mode power supply is a power supply that provides the power supply
20 function through low loss components such as capacitors, inductors, and
transformers and in which the use of switches that are in one of two states - on or off.
The advantage with such a system is that the switch dissipates very little power in
either of these two states and power conversion can be accomplished with minimal
power loss which results in high efficiency.

25 Electronic transformers for halogen lamps typically require 20Watts or more of
resistive loads. The inverters used require correct load to maintain oscillation,
capacitances greater than 100pF can stall the inverter. Generally inverters have
over-current detection, to detect currents exceeding a predetermined maximum to
30 cause temporary shutdown.

Typical energy saving products implement standard diode based rectifiers with
capacitance for stable operation and EMC. However inrush currents can exceed
15Amps when inverters first start, stalling oscillation and damaging rectifiers, causing
35 early failure in both transformers energy saving globes.

It is an object of the present invention to provide an improved power supply control system and device that overcomes or at least ameliorates one or more of the disadvantages of the prior art.

5 Summary of the Invention

According to one aspect, the present invention provides a switching-mode power supply with cycle by cycle, asynchronous control scheme.

10 The power supply control system can comprise a switching-mode power supply with cycle by cycle, asynchronous control scheme, the control scheme using logical switching means, wherein the control is for managing the power source to match the required load as well as determining the regulation of the load.

15 The power supply control system can make use of simulated electronic logic gates for the logical switching means and further including assimilation and artificial intelligence neural control network, such as a perceptron, to determine the electronic simulation and to make use of a mixing of instant and averaged signals through a feedback system.

20 The power supply control system can further include a rectifier for front end supply where AC to DC conversion is required, the control scheme in the middle for controlling power conversion, and the step down or step up as final conditioning of the power conversion.

25 The control is for managing the power source to match the required load as well as determining the regulation of the load.

The power source can include boosting which provides a 'Virtual load' to the electronic transformers.

30 The cycle by cycle, asynchronous control scheme is preferably based on artificial intelligence neural nodes. In particular it uses a perceptron type model to provide a control.

35 The model makes use of multiple inputs and use of simulated electronic NAND gates and NOR gates or combinations

The model uses feedback in order to correct control and adapt to the changing input waveform in real time.

Further it preferably uses this perceptron type model in a hardware approach.

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The hardware approach can include using logical switching gates. This allows primitive decision making to occur at speeds faster than normal such as in the megahertz or gigahertz, using cheap available hardware

- 10 A preferred embodiment uses an 'AND' or 'NAND' gate comprising of a comparator with voltage of multiple inputs summed, whereby the conditioned signals can behave like an analogue 'AND' or 'NAND' gate. Each input is transformed independently so that the sum will 'fire' the comparator once the sum exceeds the reference.

- 15 The 'AND' or 'NAND' gate preferably has multiple inputs in parallel each conditioned by respective resistor feeding to and being summed by the comparator.

- The invention further provides for a control system comprising of a multi input NOR/OR gate comprising of a comparator with isolated, conditioned signals which
20 can behave like an analogue independently fired 'OR' or 'NOR' gate. Each input is transformed independently or proportionally, so that each can 'fire' the comparator once the reference is exceeded.

- The multi input NOR gate preferably has multiple inputs in parallel each conditioned
25 by respective diode feeding to comparator.

- Preferably the asynchronous systems controlled each cycle can have instantaneous peak currents monitored and adjusted in real time. In particular with mixing of instant and average signals, the input current can be controlled with incredibly low ripple
30 current for AND or NAND gates whilst maintaining control of the output.

The multiple inputs of the multi input NOR gate can be feedback from boost current and voltage and load.

- 35 The power control can include an active rectifier of input power to guarantee FET gate is within threshold in which there is a FET controller in combination with a linear regulator. The linear regulator can incorporate a large Resistor and large Zener

voltage so as to minimise power losses through minimising current in control switching. Control can be analogous to AND or NAND gates.

5 The power control can include a rectifier formed of a plurality of pairs of P and N doped MOSFETs wherein gate of one P doped MOSFETs is connected to drain of N doped MOSFET and vice versa. Preferably there is a pair of pairs of P and N doped MOSFETs.

10 In this way operation of FETs with voltages of less than 1 Volt are still controlled by the rectifier. This also avoids punch through as operation of a pair of MOSFETs cannot occur at the same time.

15 It can be seen that the invention provides a clockless design with asynchronous operation- up to approximately 2 MHz burst or beyond with very ordinary components.

There is continuous current mode inductor- virtually no input capacitance. Simultaneous regulation of high and low speed parameters (e.g. load current, voltage, temperature, etc). No electrolytic capacitance is necessary due to high speed, ceramic based design (cheap, incredibly long life, compact)

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It provides a vastly superior step response due to single cycle control.

25 EMC is easier due to low, asynchronous ripple. Further the power factor is improved due to virtually no input capacitance.

Brief Description of the Drawings

A preferred embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

30 Figure 1 is a circuit diagram of a simple peak biasing for a power supply control system using single cycle control in accordance with an embodiment of the invention;

Figure 2 is a circuit diagram of load compensation for a power supply control system using single cycle control in accordance with an embodiment of the invention, showing that an additional feedback can be derived from the perceptron output and then subtracted from an input to achieve a desired regulation;

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Figure 3 is a circuit diagram of a load variation control for a power supply control system using single cycle control in accordance with an embodiment of the invention showing an addition of an external line allowing current control;

5 Figure 4 is a circuit diagram of a voltage clamp for a power supply control system using single cycle control in accordance with an embodiment of the invention;

Figure 5 is a diagrammatic view of an artificial intelligence control of a single cycle control the power supply using a Perceptron algorithm;

10 Figure 6 is a diagrammatic view of a logical multi input NAND gate and associated truth table while figure 7 is a diagrammatic of a circuit element simulating such logical NAND gate using the Perceptron algorithm. Figure 7 shows the construction using buffers, resistor network, comparator and bias linked with figure 6;

Figure 8 is a diagrammatic view of a logical multi input NOR gate and associated truth table while figure 9 is a diagrammatic of a circuit element simulating such logical NOR gate using the Perceptron algorithm. Figure 8 shows a physical
15 construction using buffers, diodes, comparators and bias.;

Figure 10 is a diagrammatic view of the circuit having a combined inclusive and summing Perceptron algorithm of figures 7 and 9;

20 Figure 11 is a diagrammatic view of the use of the logical multi input gates of figures 6 to 10 in order to provide feedback and boost of the current and voltage to for efficiency and component size etc.;

Figures 12 and 13 are diagrammatic views of a more complex instruction according to the Perceptron algorithm making use of certain elements simulating logical multi input gates and showing that the signals can be adjusted by external control as required. In particular Figure 13 shows that can be made into far more
25 complex decision systems including in multi layers;

Figure 14 is a circuit diagram of a subtraction circuit in a comparative usage in logical switching means of the invention;

Figures 15, 16, 17 and 18 are each a diagrammatic view of various topologies controlled by Duty cycle,

30 Figure 19 is a diagrammatic view of a possible complete circuit having Rectifier and Step Down sections;

Figure 20 is a trace of gated input current with regard to circuit of Figure 19;

Figure 21 is a circuit diagram of power control of one embodiment of the invention showing rectifier;

35 Figures 22A and 22B is a circuit diagram of NFET and PFET models for use in rectifier of Figure 21;

Figure 23 is a circuit diagram of power control of rectifier of prior art shown for comparative purposes;

Figure 24A is an operational trace of V and I of power control circuit of Figure 22 in comparison to an operational trace of V and I of power control circuit of prior art of Figure 23 showing clear losses in the lower line of Figure 24B in comparison to lower line of Figure 24A showing minimal loss or disturbance;

Figure 25 is a circuit diagram of power control of one embodiment of the invention showing rectifier with active pulldown;

Figure 25 is an operational trace of V and I of power control circuit of Figure 24;

Figures 26 and 27 are N and P FET equivalent sub circuits respectively showing the details of FETS X1 to X4 of Figure 25 in combination with linear regulator;

Figures 28 and 29 are circuit diagrams of power control of one embodiment of add on voltage control element to load of the invention showing step down and flyback alternatives;

Figure 30 is an operational trace of V and I of power control circuit using step down result on load current; and

Figure 31 is an operational trace of step down showing simple FET fixed duty and frequency drive.

Description of a Preferred Embodiment of the Invention

The invention with reference to the drawings shows a power supply control system and its components comprising a switching-mode power supply with cycle by cycle, asynchronous control scheme, the control scheme using logical switching means, wherein the control is for managing the power source to match the required load as well as determining the regulation of the load.

The invention provides a switching-mode power supply with cycle by cycle, asynchronous control scheme. This makes use of simulated electronic logic gates that are provided in hardware. However to determine the electronic simulation and to make use of a mixing of instant and average signals through a feedback system is necessary to assimilate and artificial intelligence neural control network such as a perceptron.

Referring to Figures 1 to 4 there are four aspects of the switching-mode power supply with cycle by cycle, asynchronous control scheme of the invention.

Figure 1 is a circuit diagram of a simple peak biasing.

$$V_{sum} = g1 \cdot n/(m+n) \cdot V_L + g2 \cdot m/(m+n) \cdot i(V_i)$$

The amplifier with gain g1 presents V_{sum} with a scaled signal representing the
 5 Inductor (or primary in transformer configuration) current. The amplifier with gain g2
 applies a voltage proportional to the load current sense V_i , smoothed by function $j()$.
 The result is a bias which allows the system to trigger on a V_L peak that varies
 Inversely with V_i , eventually reaching equilibrium at the desired level. Note that in this
 example we use V_i or load current, this can easily be any other signal desired for the
 10 given application ie, Voltage, position, frequency, anything that can be transformed
 by a suitable function such as $k()$.

A limitation of this example is that it relies on the system to reach equilibrium, which
 is exacerbated when one parameter varies much slower than the other. While this
 15 makes the system inherently stable, step response is poor.

Figure 2 is a circuit diagram of load compensation for a power supply control system
 using single cycle control.

$$V_{sum} = g1 \cdot n/(m+n) \cdot V_L + g2 \cdot m/(n+m) \cdot (i(V_i) - j(V_c))$$

20 Where

$$V_c = du \cdot V_{cc}$$

$$du = (M - 1) / M$$

$$M = r \cdot V_{out} / V_{in}$$

du is duty cycle ratio

25 r is the transformer ratio, 1 for a normal booster

This variation shows an addition of a feedback loop subtracting the averaged
 comparator output. This novel modification greatly accelerates target parameter
 convergence by applying negative bias to the load signal ($j(V_c)$) whilst below the
 30 desired level, which in turn results in a higher peak current sought by the reduction in
 offset at V_{sum} . This results in higher V_L peaks and therefore more power provided
 until the desired $k(V_i)$ is reached, at which point $j(V_c)$ drops until equilibrium is
 reached. Parameter 'du' is useful in indicating the ratio ($r \cdot V_{out} / V_{in}$). As V_{in}
 approaches $n \cdot V_{out}$, $du \rightarrow 0$, du is greatest with $V_{in} \rightarrow 0$.

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Figure 3 is a circuit diagram of a load variation control for a power supply control
 system;

$$V_{sum} = g1 \cdot n/(m+n) \cdot V_L + g2 \cdot m/(n+m) \cdot (g3 \cdot (i(V_i) - k(V_t)) - j(V_c))$$

With the addition of the amplifier with gain $g3$, we are able to repeat the step in stage two to subtract yet another signal. Here $k(V_t)$ is subtracted from $i(V_i)$ to allow the target load current to be modified by an external signal.

$$V_{sum} = g1 \cdot n/(m+n) \cdot V_L + g2 \cdot m/(n+m) \cdot (i(V_i) + k(-V_t) - j(V_c))$$

As shown, if inversion of various control signals is possible, amplifiers need not be required when summing signals - only subtraction. Here the negative sign inside function $k()$ removes the need to subtract, and therefore the need for an additional amplifier. This can help reduce cost and complexity.

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Figure 4 is a circuit diagram of a voltage clamp for the power supply control system. One advantage of the ripple reduction scheme is that rectifier capacitance can be effectively removed. This does present a problem however when the input supply has an inductance large relative to the system inductance- the resulting current delta can induce large voltages. Fortunately the switching inductor can be modified to act as a clamp. An equivalent circuit is shown in Figure 4, the system appears to have zener behaviour in that it will only conduct when the input voltage exceeds a threshold. The difference being that in a zener the energy is lost as heat, where as in this configuration the energy is transferred to the load filter capacitance. This is particularly useful in applications where supply sources react poorly with capacitive loads. By selecting the desired ratios, the voltage clamp will be seen as very high impedance until the threshold is reached.

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In order to understand the operation of the power supply control system using single cycle control of the invention it is necessary to see the basis of the invention.

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A Perceptron model is artificial intelligence which is a binary classifier which maps its input via a function to output value across the range of multiple inputs. The output value must be "0" or "1" in a binary classifier and therefore can be used as a switch.

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Further the model provides a learning algorithm that can make use of feedback within the function. A diagrammatic view of this function is shown in figure 5.

Referring to figures 6, 7, 8 and 9 there are shown electronic simulation of logic gates.

In Figure 6 there is a 'NAND' gate or alternatively an 'AND' gate represented by its symbol and truth table.

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Figure 7 shows the electronic simulation making use of a comparator with voltage of multiple inputs summed, whereby the conditioned signals can behave like an analogue 'NAND' gate but could alternatively be an 'AND' gate. Each input is transformed proportionally, so that the sum will 'fire' the comparator once the reference is exceeded. The 'AND' or 'NAND' gate has multiple inputs in parallel each conditioned by respective resistor feeding to comparator.

In Figure 8 there is an 'OR' gate or alternatively a 'NOR' gate represented by its symbol and truth table.

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Figure 9 shows the electronic simulation making use of a control system comprising of a multi input NOR gate comprising of a comparator with isolated, conditioned signals which can behave like an analogue 'OR' or 'NOR' gate. Each input is transformed proportionally, so that each can 'fire' the comparator once the reference is exceeded. The multi input NOR gate preferably has multiple inputs in parallel each conditioned by respective diode feeding to comparator.

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Figure 10 is a diagrammatic view of the circuit having a combined inclusive and summing Perceptron algorithm of figures 7 and 9. It will be seen that includes the NAND gates as an input in parallel with the multiple inputs NOR gates. In use as is shown in figure 11 the logical multi input gates of figures 6 to 10 provide feedback and boost of the current and voltage to minimise inductor ripple which can affect electromagnetic interference, efficiency and component size etc. Such principles can be seen to be included in figures 1 to 4.

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Figures 12 and 13 show a more complex instruction according to the Perceptron algorithm making use of certain elements simulating logical multi input gates and showing that the signals can be adjusted by external control as required. In particular Figure 13 shows that can be made into far more complex decision systems including in multi layers;

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Figure 14 is an improvement over Figure 2 and includes power supply control system comprising of a comparator with multiple inputs summed into positive input and compared to further input into negative terminal of comparator and offset voltage by bias, whereby the sum less the further input less the bias will 'fire' the comparator once the reference is exceeded. In this way an addition of a feedback loop subtracts the averaged comparator output using comparison to bias feedback, wherein this

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greatly accelerates target parameter convergence by applying negative bias to the load signal whilst below the desired level, which in turn results in a higher peak current sought by the reduction in offset which results in more power provided until the desired current is reached, at which point it drops until equilibrium is reached.

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Referring to the original section on signal summing, to add voltages can be as simple as summing resistor networks, whereas to subtract one signal from another may require an amplifier utilizing the positive and negative inputs. Depending on the relative scaling requirements of each signal, it may be possible to sum all 'like signed' signals into the perspective inputs of the summing comparator instead. For example, instead of:

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$$V_{sum} = g1 \cdot n/(m1+n1) \cdot VL + g2 \cdot m/(m1+n1) \cdot (g3 \cdot (i(Vi) - k(Vt)) - j(Vc))$$

Where V_{sum} is compared with a fixed value such that the resulting output is:

$$V_{sum} > V_{ref}, \text{Output} = 0$$

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$$V_{sum} < V_{ref}, \text{output} = 1$$

We can instead group the negative terms and sum them into V_{ref} , and group positive terms and sum into V_{sum} , so:

$$V_{sum} = n / (m + n) \cdot VL + m / (m + n) \cdot k(Vi)$$

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$$V_{ref_new} = x / (x + y + z) \cdot$$

$$V_{ref} + y / (x + y + z) \cdot k(Vt) + z / (x + y + z) \cdot j(Vc)$$

Where V_{sum} is compared with a fixed value such that the resulting output is:

$$V_{sum} > V_{ref_new}, \text{Output} = 0$$

$$V_{sum} < V_{ref_new}, \text{output} = 1$$

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This can achieve the same result without the need of amplifiers, reducing cost and complexity.

It can therefore be seen that power supply control system and device provides the following in some form:

Problem	Competitors	Current invention.
Compatibility with existing infrastructure – huge variety of product in the field	Not rated or warranted to work with electronic transformers	Works with existing electronic and magnetic transformers
Dimming with existing infrastructure	Poor dimming and compatibility issues with existing installations	Dims with electronic transformers on correctly installed dimmers
Electronic transformers require a minimum load of 20W draw to work	Fail to draw minimum load and not warranted with electronic transformers	Virtual load allows transformers to operate correctly.
Power factor	Varies greatly and usually poor (0.3 – 0.5 typically)	Higher power factor - the system draws current in phase with the mains input (0.6 to 0.7 typically, higher if required.)

It can therefore be seen that the invention provides a new approach to single cycle control inspired by the simple, yet powerful, perceptron model. While simple in construction, the perceptron can make very simple decisions based on multiple inputs incredibly quickly and even faster when implemented in hardware. This provides many commercial implications particularly with respect to switch mode power supply is bringing meant many added benefits such as asynchronous clockwork operation with latencies limited only by the native silicon.

Although switching speeds of 2 MHz can readily be achieved to switch, the speeds can extend well beyond to about 3 to 5 MHz due to limitations of current FETs. However if this limitation is overcome, even far greater speeds could be achieved.

Examples of usage

Referring to figures 15 to 18 there is illustrated alternative topologies wherein for each of these topologies or published derivatives of these topologies can be controlled by duty cycle or component values or current or voltage applied to a circuit node or nodes.

Figure 15 shows a class d stage (either one or other switch is on or in the changeover state) loaded via a series resonant circuit and a network which loads this resonant circuit by passive and or active means. The complexity is greater, (2 switches) but the device voltage is the same as the input voltage.

Figure 16 is a Class e stage (single switch loaded by various stages connected to the switch via a series resonant cct) loaded by a half wave rectifier and decoupling capacitor. It is a single input device stage that can be designed to zero voltage switch with high speed and very good efficiency at low or medium power levels along with very good EMI profiling.

Other half or full wave circuits may be used such as but not limited to half wave inductive and in class e form, such as in figure 17, with cap loading across diode, cap loading across secondary, synchronous and asynchronous rectifiers, class d type rectifiers class e rectifiers and variations and combinations of both to achieve the advantages of ZVS and class e stages

Many of these alternatives are shown in descriptive form in figure 18 where the class e is loaded by a network which can consist of active and/or passive components which load the class e stage.

However one application is as shown in Figure 19. Power supply control system includes a rectifier for front end supply, the control scheme in the middle for controlling power conversion, and the step down or step up as final conditioning of the power conversion. It can clearly be seen that Figure 19 uses the logical gate system of Figure 7 and 14 to provide control from the feedback including in the load current detection subcircuit.

Power supply control system according to Figure 19 comprises of a comparator with multiple inputs summed into positive input and compared to further input into

negative terminal of comparator and offset voltage by bias, whereby the sum less the further input less the bias will 'fire' the comparator once the reference is exceeded.

Power supply control system includes an addition of a feedback loop subtracting the averaged comparator output using comparison to bias feedback, wherein this greatly accelerates target parameter convergence by applying negative bias to the load signal whilst below the desired level, which in turn results in a higher peak current sought by the reduction in offset which results in more power provided until the desired current is reached, at which point it drops until equilibrium is reached.

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The Schematic of the power supply control system further includes a rectifier for front end supply, the control scheme in the middle for controlling power conversion, and the step down or step up as final conditioning of the power conversion. It illustrates the various major stages, consisting of:

- 15 1. Signal summing and comparing
2. Load current detection
3. Step down
4. Rectifier capacitor decision

The combination of these stages results in a product which provides a system capable of reacting to the various environments in such a way that allows correct low energy product compatibility, very similar in behavior to a halogen globe.

Rectifier

A prior art active rectifier circuit can be seen in Figure 23 with operational trace in Figure 24B. In particular the FETs being either P type or N type are connected to external resistors such as R4 which are of the order of 100 Ohm and therefore allow substantial current flow and corresponding power loss. In particular the trace of Figure 9 shows the input at the top and the effective output in the middle. However as shown by the lower trace there is substantial power losses throughout operation.

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However the invention as shown in Figures 21 in its simplest form and Figures 22A, 22B and 25 in detail with trace in Figure 24A shows a rectifier which can make use of the power control including an active rectifier of input power to guarantee FET gate is within threshold. This is achieved by a FET controller in combination with a linear regulator. The linear regulator can incorporate a large Resistor R4 of the order of 100K Ohm and voltage close to operative voltage of the FET so as to minimise power losses through minimising current in control switching. In contrast to the trace

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of Figure 24B the trace in Figure 24A shows the input at the top and the effective output in the middle with the lower trace showing there is minimal intermittent power losses throughout operation.

- 5 As shown in Figure 21, the power control can include a rectifier formed of a plurality of pairs of P and N doped MOSFETs wherein gate of one P doped MOSFETs is connected to drain of N doped MOSFET and vice versa. In this case there are a pair of pairs of P and N doped MOSFETs with each of X1 and X2 are an NFET and with each of X3 and X4 are PFET of Figures 22A and 22B.

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In this way operation of FETs with voltages of less than 1 Volt are still controlled by the rectifier. This also avoids punch through as operation of a pair of MOSFETs cannot occur at the same time and therefore cannot add voltages beyond threshold.

- 15 Particularly in low voltage, high current applications, AC to DC rectification can be more efficiently performed with a FET full bridge rather than diodes (Schottky, PN, carbide etc) as they need not have a forward conduction voltage drop anywhere near as large. There are some considerations in implementation:

- 20 1. If the maximum voltages exceed the FET gate values, protection must be implemented to ensure the MOSFETs are not destroyed. This is the purpose of the Zener/resistor arrangement in the schematic provided.
2. The Zener should be just slightly smaller than the max gate voltage, otherwise conduction through the Zener consume large amounts of energy,
- 25 this unfortunately means that the gate capacitance has far more energy than is necessary to turn the FET on.
3. The resistor must be large enough to limit current when input voltage exceeds the Zener, but small enough to keep the turn on and off time small enough, and to prevent FET shoot through.
- 30 4. As MOSFETs have gate capacitance, any resistance used as with the example cause issues with turn on and turn off delay,
5. The gate capacitance and resistor form an RC filter, which will consume energy when any AC is present on the input, worsening with frequency and amplitude

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The new configuration shown in Figure 21 looks similar to the prior art of Figure 23. However clear differences are shown with further inspection into the X modules is

given in Figures 22A and 22B. Each sub circuit (N and P) are designed to replace the MOSFET, Zener and resistor in the prior art, with the N's on the bottom, P's on the top of the bridge.

- 5 Examining the N FET subcircuit of Figure 22A, the complete FET model is represented within the box. External to the Box is the added circuitry, a diode and FET (which would be only one device as MOSFETs always have body diodes) a resistor and a Zener. The addition of the MOSFET has a large impact on the circuit, such as:
- 10 1. The Zener can now be only large enough to ensure the rectifier FET is turned on, keeping the transfer of energy low.
 2. The MOSFET's impedance is low during the charge of the bridge MOSFET, which allows for rapid charge, but becomes very high once the Zener voltage is reached, ensuring no leakage regardless of what AC signal is on the input.
 - 15 3. As the Zener bias resistor is no longer charging the bridge MOSFET gate cap, its value can be very large, using very little energy.
 4. When the gate signal pulls low, D1 (T1's body diode) discharges the bridge gate capacitance.

The P FET subcircuit shown in Figure 22B is identical in operation, just in a negative voltage sense as it is a P FET.

- Referring to the Trace files of prior art Figure 24B and new active rectifier Figure 24A, the red (top) trace shows a constructed wave form, a base signal of 12Volts RMS (+/- 17 Volt peak to peak) AC, with a 5V peak to peak signal at much higher frequency.
- 25 The next trace indicates the current from the source, the green is the voltage on the load resistor R1, the final trace is the current going into one half bridge P/N FET pair. The greatest indicator of improvement is the trace of Figure 24A, as illustrated in the lower trace of the new active rectifier, with the exception of switching currents, no visible current. Measurements have indicated that with a simple comparison to
 - 30 Figure 24B, the new system is 98% efficient versus the old of 95%. This divide would become much greater over large input voltage ranges as the Zeners in the prior art conduct more and more, or if the frequency was increased.

Finally the next iteration of Fig 25 with reference to Figures 26 and 27 shows an enhancement which allow the bridge FET's threshold voltage to be lower than the body diode of the new gate drive FET. Signals are shared between N and P

subcircuits to ensure the FETs are shutdown. In each N or P pair, the opposing drive FET now also drives the other's newly added 'pull down' FET.

5 As shown in Figure 19 this component is specific to low voltage MR16 transformer discrimination (either electronic or magnetic.) The issue is that magnetic transformers must have some capacitance to reduce voltage ripple important for efficiency and Electro-Magnetic Compliance (EMC) whereas electronic transformers must not see capacitance for more than an instant or risk stalling, or worse. The goal is therefore to make an intelligent decision as to correctly enable or disable a rectifier capacitor. This is achieved by sensing the wave form coming into the rectifier, and
10 deciding the most likely input source type based on the characteristics present. Serious complexity occurs when magnetic and electronic transformers begin to look alike, particularly when used with dimmers.

15 Referring to the Schematic, the 'Rectifier cap decision block' interprets signals from one or more of the illustrated 'Transformer detect points' and applies mathematical manipulations and state based decisions to then turn the rectifier capacitor on or off via 'CAP_SWITCH_CNTL'

20 **Step Down / Fly Back**

The step down/ fly back components as shown in Figures 28 and 29 are often needed to connect at the output across Capacitor C2 as shown in Figure 2 for power control of LEDs due to operational voltage limitation. However such system may not be required in other power control areas.

25 Due to the constant forward voltage nature of Light Emitting Diodes (LEDs) the usable energy in a capacitor connected in parallel is very limited. This is because any voltage in the capacitor above the LED V_f (forward voltage) is quickly discharged at higher currents, until the voltage falls to V_f , at which point conduction stops. A
30 simple approach to this is to have a resistor in series, which limits the current at voltages over V_f . The drawback to this is of course wasted energy in the resistor.

A more elaborate method is to implement a full 'buck' circuit. Done well this can minimize the additional power loss, at the expense of complexity and cost. A
35 potential issue with this is the introduction of a 'negative impedance'- as voltage goes up, current goes down and vice versa. This is in contrast to a 'positive impedance' which has current and voltage moving up and down together, proportionally or

otherwise. In a standalone circuit a buck's negative impedance may not be an issue, but if used in conjunction with another control scheme this may become problematic.

Another problem with having a capacitor directly in parallel with a LED occurs when
5 we are using a boost topology. As the output voltage must always be greater than the input voltage, LED Vf's must therefore be relatively high. In the case of MR16 where the input voltage can reach over 17V peak (12VRMS) this limits the product to 20V+ dies. If we wish to use a lower voltage LED, a natural solution is to introduce a buck stage after the boost. However this introduces a problem where the individual
10 boost and buck stages 'fight' each other, which is why despite the large capacitive energy reserve buffering between, the booster frequently turns off due to over voltage output conditions caused by a negative impedance load (the buck).

The present invention includes a much simpler step down mechanism to be
15 introduced, which is much cheaper to implement, and still provides the boost with a positive impedance.

Referring to the Figure 28, there is shown a general possible combination. These can be used for a 9V and a 21V LED solution. Even though the 21V LED already
20 meets the greater voltage requirements, the ripple current in the LED over mains frequencies (50-60Hz) is much better due to the more readily available energy reserve due to the large operational voltage range now available.

There are advantage of bucks in the prior art including allowing precise load
25 regulation down to the load voltage if buck, or complete range if flyback. However there are also issues with bucks and flybacks including:

1. Expensive,
2. Complex closed loop systems and inefficient particularly if a high side FET drive is necessary (in buck configurations)
- 30 3. Imposes negative impedance characteristics on the voltage supply
4. Complexity and stability requirements generally limits maximum speed, which in turn requires larger passive components to implement

Similarly there are advantages of fixed frequency and duty step down or flyback

- 35 1. Open loop (no feedback) so very cheap and easy to implement
2. Only ever need low side switching so easy to implement

3. Imposes positive impedance at all times, easy to combine with regulation stage such as boost
4. Simplicity means that upper speeds are only limited by resonant source drive capabilities, so can be incredibly high.
- 5 Issues with fixed frequency and duty step down or flyback
 1. Open loop means that operation is limited to fixed transformation of input voltage- ie no adaption possible.

The operation of the present invention is with reference to the drawings but noting that Figure 28, R4 is included in series with D1 to represent a 'real' LED made up of desired and parasitic components. The step down referred to in the 9V schematic and traces, has a very simple operation implements an oscillating source of any type capable of driving a FET, in this example V3. When the FET is biased on, current begins to rise in L3 the LED (D1) and C3. When the FET turns off, the inductor discharges into D1 and C3. C3 acts purely as an AC bypass to keep the current ripple in the LED to a minimum, and can therefore be extremely small. This simple action results in L3 appearing as an additional impedance in series with the LED, varying only with the difference in voltage between the LED V_f and the reservoir C3. This impedance can be varied by either changing the inductance of L1, or the frequency/duty cycle ratio of the inverter.

The flyback referred to in the 21V Traces and Schematics, as above the implementation is remarkably simple and also generally shown in Figure 28. When the FET is biased on, L1 begins to charge. When the FET is turn off, L1 discharges into C4 and the LED. Again, C4 is included to merely bypass AC, providing DC current to the LED. This circuit differs to the step down in that it is possible to discharge C4 below the LED voltage. Whilst desirable with a large V_f such as 21V, this is highly undesirable with voltages already lower than the minimum allowed boost voltage. As with the step down, the inductor appears as a roughly linear, positive impedance, so long as the frequency and duty cycle ratio are fixed.

Note that any frequency and duty can be implemented, there are advantages to some adjustments, such as:

1. Frequency Jitter- this can help if Electro Magnetic Interference (EMI) are encountered
2. Duty cycles ratios other than 50/50 (as used in the examples) may be useful particularly if lower V_f 's are desired, setting the duty to say 15/85 on/off would

allow step down voltages as low as 3Volts (single LED die) without adding any more complexity or feedback, depending on the oscillator source used.

- 5 Those of skill in the art will appreciate that such modifications or changes to the particular embodiments exemplified can be made without departed from the scope of the invention. All such modifications and changes are intended to be included within the scope of this invention as defined in the following claims.

Claims

1. Power supply control system comprising a switching-mode power supply with cycle by cycle, asynchronous control scheme, the control scheme using logical switching means, wherein the control is for managing the power source to match the required load as well as determining the regulation of the load.
2. Power supply control system according to claim 1 for a switching-mode power supply with cycle by cycle, asynchronous control scheme, making use of simulated electronic logic gates for the logical switching means and further including assimilation and artificial intelligence neural control network, such as a perceptron, to determine the electronic simulation and to make use of a mixing of instant and average signals through a feedback system.
3. Power supply control system according to claim 1 wherein the logical switching means of the cycle by cycle, asynchronous control scheme is based on artificial intelligence neural nodes.
4. Power supply control system according to claim 3 wherein artificial intelligence neural nodes uses a perceptron type model to provide a control.
5. Power supply control system according to claim 1 wherein the logical switching means has a model making use of multiple inputs and use of simulated electronic NAND gates and NOR gates or combinations.
6. Power supply control system according to claim 1 wherein the power source includes boosting which provides a 'Virtual load' to the electronic transformers.
7. Power supply control system according to claim 5 wherein the model uses feedback in order to correct control and adapt to the changing input waveform in real time.
8. Power supply control system according to claim 4 wherein uses this perceptron type model in a hardware approach using logical switching gates.

9. Power supply control system according to claim 1 wherein the logical switching means has a model making use of an 'AND' or 'NAND' gate comprising of a comparator with voltage of multiple inputs summed, whereby the conditioned signals can behave like an analogue 'AND' or 'NAND' gate wherein each input is transformed independently so that the sum will 'fire' the comparator once the reference is exceeded.
10. Power supply control system according to claim 9 wherein the 'AND' or 'NAND' gate has multiple inputs in parallel each conditioned by respective resistor feeding to comparator.
11. Power supply control system according to claim 1 wherein the logical switching means has a model making use of a multi input NOR/OR gate comprising of a comparator with isolated, conditioned signals which can behave like an analogue 'OR' or 'NOR' gate wherein each input is transformed independently or proportionally, so that each can 'fire' the comparator once the reference is exceeded.
12. Power supply control system according to claim 11 wherein the multi input OR or NOR gate has multiple inputs in parallel each conditioned by respective diode feeding to comparator.
13. Power supply control system according to claim 1 wherein the asynchronous systems controlling each cycle have instantaneous peak currents monitored and adjusted in real time wherein in particular with mixing of instant and average signals, the input current is controlled with low ripple current whilst maintaining control of the output.
14. Power supply control system according to claim 11 wherein the multiple inputs of the multi input NOR or OR gate can be feedback from boost current and voltage and load.
15. Power supply control system according to claim 1 including a combined inclusive and summing Perceptron algorithm that includes the NAND gates as an input in parallel with the multiple inputs NOR gates wherein in use the logical multi input gates provide feedback and boost of the current and

voltage to minimise inductor ripple which can affect electromagnetic interference, efficiency and component size etc.

- 5 16. Power supply control system according to claim 15 comprising of a comparator with multiple inputs summed into positive input and compared to further input into negative terminal of comparator and offset voltage by bias, whereby the sum less the further input less the bias will 'fire' the comparator once the reference is exceeded.
- 10 17. Power supply control system according to claim 16 including an addition of a feedback loop subtracting the averaged comparator output using comparison to bias feedback, wherein this greatly accelerates target parameter convergence by applying negative bias to the load signal whilst below the desired level, which in turn results in a higher peak current sought by the
- 15 reduction in offset which results in more power provided until the desired current is reached, at which point it drops until equilibrium is reached.
- 20 18. Power supply control system according to any one of the above claims further including a rectifier for front end supply, the control scheme in the middle for controlling power conversion, and the step down or step up as final conditioning of the power conversion.
- 25 19. Power supply control system according to claim 18 wherein the control scheme and step down complement each other.
20. Power supply control system according to claim 18 wherein the rectifier and the control scheme complement each other.
- 30 21. Power supply control system according to claim 20 includes an active rectifier of input power to guarantee FET gate is within threshold in which there is a FET controller in combination with a linear regulator wherein the linear regulator can incorporate a large Resistor and large Zener voltage so as to minimise power losses through minimising current in control switching.
- 35 22. Power supply control system according to claim 20 includes a rectifier formed of a plurality of pairs of P and N doped MOSFETs wherein gate of one P doped MOSFETs is connected to drain of N doped MOSFET and vice versa.

23. Power supply control system according to claim 20 includes step down as final conditioning of the power conversion comprising of an oscillating source of any type capable of driving a FET, such that when the FET is biased on, current begins to rise in the LED and when the FET turns off, the inductor discharges including into output capacitor which acts purely as an AC bypass to keep the current ripple in the LED to a minimum, and can therefore be extremely small, wherein this simple action results in an additional impedance in series with the LED, varying only with the difference in voltage between the LED output capacitor.
24. Power supply control system according to claim 20 includes step up as final conditioning of the power conversion comprising a flyback wherein when the FET is biased on, inductor begins to charge and when the FET is turn off, inductor discharges into feedback capacitor and the LED wherein feedback capacitor is included to merely bypass AC, providing DC current to the LED, and wherein the inductor appears as a roughly linear, positive impedance, so long as the frequency and duty cycle ratio are fixed.
25. Power supply control system substantially as hereinbefore described with reference to the drawings.
26. Power supply control system substantially as hereinbefore described with reference to Figures 19 to 31 of the drawings but excluding Figures 23 and 24B.