What is claimed is:

1. A method for programming a non-volatile memory device, the method comprising:

applying a program word line voltage with a voltage level changed stepwise to a selected word line connected to a plurality of memory cells, the program word line voltage including a first voltage level during a first time interval and a second voltage level different from the first voltage level during a subsequent second time interval;

applying a first program bit line voltage to a first bit line of a plurality of bit lines connected to a plurality of first memory cells, while the program word line voltage is applied to the selected word line;

when the first program bit line voltage has a program inhibit voltage level, inhibiting the plurality of first memory cells from programming; and

when the first program bit line voltage has a program voltage level, programming the plurality of first memory cells,

wherein the first program bit line voltage has a third voltage level between the program inhibit voltage level and the program voltage level during the first time interval, and one of the program inhibit voltage level, the program voltage level, and a fourth voltage level between the program inhibit voltage level and the program voltage level during the subsequent second time interval, and

wherein the method further comprises: while applying the first program bit line voltage to the first bit line, applying a second program bit line voltage to a second bit line of the plurality bit lines connected to a plurality of second memory cells, the second program

bit line voltage having the program inhibit voltage level during the first time interval, and the program voltage level during the subsequent second time interval.

2. The method of claim 1, wherein the second voltage level is lower than the first voltage level.

3. The method of claim 2, wherein the program inhibit voltage level is a power supply voltage level,

wherein the program voltage level is a ground voltage level, and

wherein the third voltage level is a forcing voltage level which is applied to the first bit line to improve threshold voltage dispersion of the plurality of first memory cells connected to the first bit line.

4. The method of any one of claims 1 to 3, wherein the first program bit line voltage has the program inhibit voltage level during the subsequent second time interval.

5. The method of any one of claims 1 to 3, wherein the first program bit line voltage has the fourth voltage level lower than the third voltage level during the subsequent second time interval.

6. The method of any one of claims 1 to 3, wherein the first program bit line voltage has the fourth voltage level higher than the third voltage level during the subsequent second time interval.

7. The method of any one of claims 1 to 3, wherein the first program bit line voltage has the program voltage level during the subsequent second time interval.

8. The method of claim 7, wherein the plurality of first memory cells are programmed to a predetermined program state by applying the program word line voltage and the first program bit line voltage.

9. A method for programming a non-volatile memory device, the method comprising:

applying a program word line voltage with a voltage level changed stepwise to a selected word line connected to a plurality of memory cells, the program word line voltage including a first voltage level during a first time interval and a second voltage level different from the first voltage level during a subsequent second time interval;

applying a first program bit line voltage to a first bit line of a plurality of bit lines connected to a plurality of first memory cells, while the program word line voltage is applied to the selected word line;

when the first program bit line voltage has a program inhibit voltage level, inhibiting the plurality of first memory cells from programming; and

when the first program bit line voltage has a program voltage level, programming the plurality of first memory cells,

wherein the first program bit line voltage has the program inhibit voltage level during the first time interval, and one of a third voltage level and a fourth voltage level between the program inhibit voltage level and the program voltage level during the subsequent second time interval, and

wherein the method further comprises: while applying the first program bit line voltage to the first bit line, applying a second program bit line voltage to a second bit line of the plurality bit lines connected to a plurality of second memory cells, the second program bit line voltage having the program inhibit voltage level during the first time interval, and the program voltage level during the subsequent second time interval.

10. The method of claim 9, wherein the second voltage level is lower than the first voltage level, and

wherein the first program bit line voltage has the program inhibit voltage level during the first time interval, and the third voltage level during the subsequent second time interval.

11. The method of claim 10, wherein the program inhibit voltage level is a power supply voltage level,

wherein the program voltage level is a ground voltage level, and

wherein the third voltage level is a forcing voltage level which is applied to the first bit line to improve threshold voltage dispersion of the plurality of first memory cells connected to the first bit line.

12. The method of claim 9, wherein the first bit line and the second bit line are disposed adjacent to each other.

13. A method for programming a non-volatile memory device, the method comprising:

applying a program word line voltage with a voltage level changed stepwise to a selected word line connected to a plurality of memory cells, the program word line voltage including a first voltage level during a first time interval and a second voltage level different from the first voltage level during a subsequent second time interval;

applying a first program bit line voltage to a first bit line of a plurality of bit lines connected to a plurality of first memory cells, while the program word line voltage is applied to the selected word line;

when the first program bit line voltage has a program inhibit voltage level, inhibiting the plurality of first memory cells from programming;

when the first program bit line voltage has a program voltage level, programming the plurality of first memory cells; and

turning off a string selection transistor connected to the plurality of first memory cells before the first program bit line voltage transitions to the program voltage level,

wherein the method further comprises: while applying the first program bit line voltage to the first bit line, applying a second program bit line voltage to a second bit line of the plurality bit lines connected to a plurality of second memory cells, the second program bit line voltage having the program inhibit voltage level during the first time interval, and the program voltage level during the subsequent second time interval.

14. The method of claim 13, further comprising:

applying the second program bit line voltage to the second bit line of the plurality of bit lines connected to the plurality of second memory cells, while the program word line voltage is applied to the selected word line,

wherein when the first program bit line voltage transitions from the program inhibit voltage level to the program voltage level, the second program bit line voltage transitions

from the program inhibit voltage level to a third voltage level having a level higher than the program inhibit voltage level, and

wherein the first bit line and the second bit line are disposed adjacent to each other.

15. The method of claim 14, wherein the string selection transistor is turned off, before the second program bit line voltage transitions from the program inhibit voltage level to the third voltage level.

16. The method of claim 14 or claim 15, further comprising:

applying a third program bit line voltage to a third bit line of the plurality of bit lines connected to a plurality of third memory cells, while the program word line voltage is applied to the selected word line,

wherein when the first program bit line voltage transitions from the program inhibit voltage level to the program voltage level, the third program bit line voltage transitions from the program inhibit voltage level to a fourth voltage level lower than the program inhibit voltage level and higher than the program voltage level.

17. The method of claim 14, wherein the string selection transistor is turned on while applying the first program bit line voltage having the program voltage level to the first bit line and after transitioning the second program bit line voltage from the third voltage level to the program inhibit voltage level.

18. The method of claim 13, further comprising:

applying the second program bit line voltage to the second bit line of the plurality of bit lines connected to the plurality of second memory cells, while the program word line voltage is applied to the selected word line,

wherein when the first program bit line voltage transitions from the program inhibit voltage level to the program voltage level, the second program bit line voltage transitions from the program inhibit voltage level to a third voltage level lower than the program inhibit voltage level and higher than the program voltage level.