

HIGH SPEED, REAL-TIME, STATE INTERCONNECT FOR AUTOMATIC TEST EQUIPMENT

This invention relates generally to automatic test equipment, and more specifically to high-speed, general purpose, automatic test equipment.

5 The following background art can be regarded as useful for understanding the invention: WO 97 12254 A (Credence Systems Corp), 3 April 1997.

Automatic test equipment (also known as a "tester") is commonly used in processes for manufacturing semiconductor devices to determine whether the manufactured devices are defective. Testers generally include computerized control
10 circuitry that controls various types of instruments used to perform tests including applying signals to a device under test, detecting signals produced by the device under test, and measuring any parameters related the device under test. The computerized control circuitry then generally compares the detected signals and measured parameters with stored expected values, thereby determining whether the device under
15 test contains defects.

Semiconductor devices may include digital circuitry, analog circuitry, or both. Devices that include both analog and digital circuitry are commonly called mixed-signal devices, and the testers that test them are commonly called mixed-signal testers. Further, the speed, density, and overall complexity of these devices generally increase
20 with successive generations of the devices. Accordingly, it is increasingly important that testers provide a high-level of operator control and programming flexibility in order to test these devices thoroughly.

FIG. 1 shows a tester 100 that is useful for testing mixed-signal devices such as a device under test (DUT) 118. In particular, the tester 100 includes a test
25 computer 104 coupled to a sequencer 102 and a plurality of instruments such as a high-speed digital (HSD) instrument 106, a precision AC instrument 108, and a precision DC instrument 110. The test computer 104 is typically housed in a workstation (not shown) and generally provides signals for controlling the sequencer 102 and the instruments 106, 108, and 110. Further, tester pins 112, 114, and 116
30 connect the instruments 106, 108, and 110, respectively, to electrical nodes of the DUT 118.

The test computer 104 is coupled to the sequencer 102 and the instruments 106, 108, and 110 by way of a test computer (TC) bus 122. Similarly, the sequencer 102 is coupled to the instruments 106, 108, and 110 by way of a state bus 120.

AMENDED SHEET

During a typical test session, a test engineer uses the workstation to specify various operating conditions and to enter various tester commands. For example, the test engineer may specify a test cycle time and values to be applied to and detected from the DUT 118 during each test cycle. The values that are specified for a particular test cycle are collectively known as a "vector," and a group of vectors that constitutes a complete test is generally known as a "pattern."

The test engineer then typically loads a pattern into a memory (not shown) included in the sequencer 102 and enters a command to start the test. This generally causes the sequencer 102 to read a different vector during each test cycle, and place data derived from the vectors on the state bus 120. The data typically includes both the values that are to be applied or detected by certain instruments during a test cycle and the times when these values are to be applied or detected relative to the start of the test cycle.

For example, the information may direct the HSD instrument 106 to apply and detect digital signals at a node of the DUT 109. The information may also direct the AC instrument 108 to apply and capture analog signals at another node of the DUT 109. Further, the information may direct the DC instrument 110 to apply or measure specified levels at still another node of the DUT. 109.

The state bus 120 also typically includes various clock signals and condition flags that may be used by the test computer 104 and the instruments 106, 108, and 110 during each test cycle. The information on the state bus 120 therefore defines the status of the tester 100 during each cycle of tester operation.

Although the tester 100 has been successfully used to test many complex mixed-signal devices, we have recognized several shortcomings. In particular, there has arisen a need for testers that can test complex semiconductor devices that are sometimes called "systems-on-a-chip." These complex devices are generally high-speed, high-density, mixed-signal devices that require an even higher level of operator control and programming flexibility than can be achieved with the conventional tester configuration described above.

For example, in order to test complex devices like the systems-on-a-chip, it would be desirable to have a tester with more sequencers. This is because such devices generally have a greater number of nodes, and therefore a greater number of nodes operating at different data rates. By programming multiple sequencers to operate according to different test cycle times, the test engineer would be able to test multiple nodes operating at different data rates simultaneously. However, increasing

AMENDED SHEET

the number of sequencers generally complicates the distribution of state information to the instruments.

As described above, the tester 100 includes a sequencer 102 that distributes state information to the instruments 106, 108, and 110 by way of a state bus 120. In a
5 typical tester configuration, the instruments are arranged in several card cages, and the sequencer 102 is included on a board in one of the card cages. Further, the state bus 120 and the TC bus 122 are connected to the card cages in a daisy chain fashion.

Although the daisy chain bus connection used in the tester 100 effectively distributes state information from the sequencer 102 to the instruments 106, 108, and
10 110, we have recognized that it would not be as effective in a tester with more sequencers. This is because having more sequencers would typically require more state busses, thereby increasing the number of bus connections to the instruments and complicating the clocking required for deterministic and adjustable delays throughout the system. It would therefore be more difficult to ensure that state information was
15 communicated to the instruments 106, 108, and 110 at proper and predictable times.

Further, having daisy chain bus connections in a tester generally means that state information is distributed through a pipeline with each card cage in the tester at a different level in the pipeline. Such a configuration is generally difficult to implement and not easily adapted to testing high-speed, high-density systems-on-a-chip.

20 It would therefore be desirable to have a tester that can test complex, high-speed, high-density, mixed-signal semiconductor devices. This tester would have a way of distributing state and other information to all parts of the test system in a manner that provides deterministic and adjustable delays. It would also be desirable to have a tester that has a general purpose and scalable architecture.

AMENDED SHEET

three (3) pairs of links communicating with it. However, once again there are trade-offs related to performance and manufacturability.

For example, state data passing between the sequencer 402 and the sequencer 403 passes through the two (2) link interfaces 422 and 423. However, state data
5 passing between the sequencer 402 and the sequencer 405 passes through the three (3)
link interfaces 422, 423, and 424. This constitutes the worst-case delay through the
network 420.

Because data generally passes through three (3) link interfaces in the network
220 of the test system 200, the test system 400 can sometimes have less pipeline delay
10 to the DUT than the test system 200. Nevertheless, timing considerations are
generally simpler and more deterministic in the test system 200 because data generally
passes through the same number of link interfaces in the network 220.

Therefore, the invention should be limited only by the scope of the appended
claims.

APPENDED SHEET

What is claimed is

(61)

- 1 1. Automatic test equipment (200), used to determine whether a semiconductor
2 device (218) is defective, comprising:
3 a test computer (204);
4 a plurality of sequencers (e.g., 202, 203, 205); and
5 a network of nodes (e.g., 221-225) interconnecting the test computer and the at
6 least one sequencer,
7 wherein the delay through each node is adjustable, and the test computer and
8 the plurality of sequencers are coupled to respective nodes by way of a
9 pair of uni-directional links (e.g., 230, 231).
- 1 2. The automatic test equipment as recited in claim 1,
2 wherein each of the plurality of sequencers controls at least one particular
3 instrument (e.g., 206, 208, 210).
- 1 3. The automatic test equipment as recited in claim 1,
2 wherein the nodes are arranged in a star configuration.
- 1 4. The automatic test equipment as recited in claim 1,
2 wherein the respective nodes are coupled to a central node (e.g., 223).
- 1 5. The automatic test equipment as recited in claim 1,
2 wherein each node includes circuitry for synchronizing data (e.g., 223)
3 exchanged between the test computer and the plurality of sequencers
4 with a system clock.
- 1 6. The automatic test equipment as recited in claim 5,
2 wherein the synchronizing circuitry includes a FIFO (e.g., 245).
- 1 7. The automatic test equipment as recited in claim 1,
2 wherein the nodes are arranged in a serial configuration.
- 1 8. The automatic test equipment as recited in claim 1,
2 wherein the nodes are arranged in a ring configuration.

AMENDED SHEET

1 9. The automatic test equipment as recited in claim 1,
2 wherein each node includes circuitry (e.g., 252-255) for enabling passage of
3 data through the node.

1 ~~10. The automatic test equipment as recited in claim 9,~~
2 wherein the enabling circuitry is programmable.

1 11. The automatic test equipment as recited in claim 10,
2 further comprising means for programming the enabling circuitry at the start
3 of a test cycle.

1 12. The automatic test equipment as recited in claim 1,
2 wherein each node includes at least one programmable pipeline delay element
3 (e.g., 248-251), the delay through each node being adjustable by
4 programming the at least one pipeline delay element, and
5 wherein each programmable pipeline delay element delays a digital input
6 signal by a programmable number of clock cycles.

1 13. The automatic test equipment as recited in claim 14,
2 wherein each node includes circuitry (e.g., 252-256), coupled to the at least
3 one programmable pipeline delay element, for combining data.

1 14. The automatic test equipment as recited in claim 13,
2 wherein an output of the combining circuitry is used for indicating a halt-on-
3 fail condition.

1 15. The automatic test equipment as recited in claim 13,
2 wherein an output of the combining circuitry is used for indicating a branching
3 condition.

1 16. A tester (200), used to determine whether an electronic circuit (218) is
2 functioning properly, comprising:
3 a test computer (204);
4 a plurality of sequencers (e.g., 202, 203, 205); and

5 a plurality of point-to-point links (e.g., 221-225) interconnecting the test
 6 computer and the plurality of sequencers,
 7 wherein each point-to-point link has a programmable delay, each point-to-
 8 point link including at least one programmable pipeline delay element
 9 (e.g., 248-251) for programming the delay, and
 10 wherein each programmable pipeline delay element delays a digital input
 11 signal by a programmable number of clock cycles.

1 17. The tester as recited in claim 16,
 2 wherein each point-to-point link includes circuitry (e.g., 252-256) for
 3 inhibiting the passage of data bits through the link.

1 18. The tester as recited in claim 17,
 2 wherein the inhibiting circuitry is programmable, and
 3 wherein the inhibiting circuitry is programmed at the start of a test cycle.

1 19. The tester as recited in claim 16,
 2 wherein each point-to-point link carries a plurality of data bits in parallel, and
 3 ~~wherein each point-to-point link includes circuitry for combining (e.g., 256) at~~
 4 ~~least a portion of the plurality of data bits.~~

1 20. A method of operating a tester (200), used to determine whether a device
 2 under test (218) is functioning properly.
 3 the tester including a test computer (204), a plurality of sequencers (e.g., 202,
 4 203, 205), a network of nodes (e.g., 221-225) interconnecting the test
 5 computer and the plurality of sequencers, and a least one instrument
 6 (e.g., 206, 208, 210) coupled between each of the plurality of
 7 sequencers and the device under test,
 8 wherein each node includes at least one programmable pipeline delay element
 9 (e.g., 248-251) for adjusting delay time through the network and for
 10 enabling and disabling passage of data through the network,
 11 comprising the steps of:
 12 (a) programming the at least one programmable pipeline delay element to
 13 specify the delay time through the network, thereby delaying a digital
 14 input signal by a programmable number of clock cycles;

- 15 (b) setting up the enabling circuitry for passing selected data to the at least
16 one sequencer;
17 (c) operating the at least one instrument to send test signals to the device
18 under test in accordance with the selected data;
19 (d) operating the at least one instrument to receive signals produced by the
20 ~~device under test in response to the test signals; and~~
21 (e) comparing the received signals with expected values, thereby
22 determining whether the device under test is functioning properly.
-