Description

This invention relates to the manufacture of complementary metal-oxide-semiconductor (CMOS) integrated circuit devices.

The manufacture of CMOS integrated circuit devices involves a large number of processing steps of which probably the most critical are the various photolithographic operations used to form the masks that serve to localize the various implantation steps by which ions, used as dopants, are introduced into the semiconductor (usually silicon) substrate to define the electronic structure of the substrate and to impart the desired electronics properties to the final device. These are commonly referred to as masking steps and a continuing aim in manufacture has been to reduce the number of masking steps to simplify the process, thereby increasing the manufacturing yield and reducing the cost.

In EP-A-0111099 is disclosed a method of making CMOS integrated circuit transistors wherein complementary p-type and n-type transistors are formed on respectively n-type and p-type wells, said wells being formed on lightly doped epitaxial silicon. The fabrication process involves forming a gate oxide and gate electrodes. Thereafter selective implantation is required to create the n-type transistor source/drain regions and a technique of differential oxide growth is used to selectively implant the p-type transistor source/drain regions.

In EP-A-0169600 is disclosed a method of fabricating CMOS integrated circuit transistors wherein complementary P-type and N-type transistors are formed in N-type and P-type wells directly on the substrate. A first implantation step is used to form the N-type transistor source/drain regions and a second implantation step is used (wtih high temperature oxide as a mask), to create the P-type transistor source/drain regions.

The present invention is a process for manufacturing CMOS integrated circuit devices with fewer masking steps than previously used for making comparable devices.

To this end, in an illustrative embodiment of the invention, to reduce the number of masking steps, greater use is made of blanket, or non-selective, implantation steps that do not require an added mask to introduce donor and acceptor ions as dopants into the substrate. We have found that such non-selective implantation steps may be effectively substituted in particular steps for selective, or masked implantation steps by appropriately tailoring later selective implantation steps.

The present invention provides in one aspect a process for manufacturing CMOS integrated circuit devices including N-type and P-type transistors comprising the steps of:

preparing a silicon wafer on whose active surface are included contiguous P-type and N-type wells in which are to be formed N-type and P-type transistors, respectively;

blanket implanting the active surface of this wafer relatively shallowly with acceptor ions for establishing the voltage threshold for the transistors to be formed;

selectively implanting the N-type wells relatively deeply with donor ions for providing punch-through protection to the P-type transistors to be formed in such wells;

forming a gate oxide layer over the active surface of the wafer;

forming gate electrodes separately over the gate oxide layer on the P-type and N-type wells;

blanket implanting the wafer with donor ions for use in forming lightly doped source/drain regions for the N-type transistors, and in providing doped regions in the n-wells where the source/drain halo regions for the P-type transistors are to be formed;

forming dielectric spacers at the side edges of the gate electrodes;

selectively implanting the N-type wells with both donor and acceptor ions at accelerating voltages and dosages for forming the source/drain regions and associated halos of the P-type transistors; and

selectively implanting the P-type wells with donor ions at an accelerating voltage and dosage for forming source/drain regions of the N-type transistors.

The final step of selective implantation of the P-type wells can be carried out in one embodiment with both donor and acceptor ions to form not only the source/drain regions of the N-type transistors but also associated halo regions.

The selective implantation of the P-type wells can be carried out by forming oxide layers which have a different thickness over the N-type wells than over the P-type wells by differential oxide growth resulting from the faster growth of oxide in the more heavily doped silicon.

For a better understanding of the invention, an embodiment of the invention is illustrated by way of example only with reference to Figures 1-8 show in cross section a portion of a silicon water in successive stages of its manufacture into CMOS integrated circuit devices in accordance with an illustrative embodiment of the invention.

With reference now to the drawings, Figure 1 shows a monocrystalline silicon wafer in which a large number of integrated circuit devices are formed in parallel for subsequent dicing into discrete chips, each of which includes one or more CMOS integrated circuit devices. Because of the small sizes involved, particularly in the vertical direction, it is not practical to show the Figures to

scale.

The substrate 10 is shown including along the top or active surface where the devices are to be formed a first well 12 of N-type conductivity adjacent a second well 14 of the opposite or P-type conductivity, for forming a PN junction 15 therebetween. Additionally, at the intersection of the PN junction with the surface, a field oxide layer 18 overlies the surface. At the interface between the field oxide and the silicon substrate, it is usual to include localized more heavily doped N-type and P-type layers, 19 and 20, respectively, to serve as channel stop.

The wells typically are several microns deep, for example between three and four microns, and vary widely in lateral extent. Some wells are of a size to accomodate only a single transistor, others of a size to include dozens of transistors. In the illustrative embodiment being described, the wells are each shown of a size to include only a single transistor.

Various techniques are known for forming such a two-well substrate and the particular one chosen is not critical to the invention. One technique involves starting with a silicon substrate on one surface of which is grown an epitaxial layer that is only lightly doped and then doing a first selective implantation of a dopant of one type to form the first well and then, after masking this implanted region, implanting again with a dopant of the opposite type to form the second well.

This technique permits the most accurate control of the doping levels in each well and so is now generally preferred for state of the art devices. Typically, each of these wells has doping levels in the range of between about 10^{16} and 10^{17} ions per cubic centimeter.

Alternatively, there may simply be prepared a substrate of the desired doping level for one of the wells and a selective implantation then done to form the second well localized with the first well. This has the advantage of saving one masking step at the expense of reduced control of the doping level in the second well because of the need to compensate for a higher background level of the dopant of opposite type used to dope the initial substrate.

Moreover, after preparation of the two well substrates, there can be formed the channel stops and the field oxide in any known fashion. Generally this involves separate selective implantations to form each of the two channel stops followed by a localized oxidation step.

Once the two well structure described has been formed there is a blanket or non-selective implantation of a P-type impurity, over the entire active surface of the substrate 10, that serves primarily to fix the threshold voltage of the MOS transistors to be formed in the respective wells. In the past, it has been the practice usually to employ selective implantation for this purpose to custom tailor the threshold voltage of each well individually. In the present invention, there is employed a blanket implantation only of acceptor ions and suitable adjustments are made in subsequent implantations. Typically, boron fluoride is used as the source to implant a relatively light dosage of 10^{12} boron ions per square centimeter at an accelerating voltage of about fifty thousand electron volts to form a shallow P-type layer, denoted by the broken line 22 in Figure 2. To avoid cluttering the drawing unnecessarily, the channel stops 19, 20 shown in Figure 1 are not being shown in the subsequent Figures 2-7, although they remain under the field oxide regions 18 to the end and are shown in Figure 8.

Next, the active surface is covered with a layer of a suitable masking material, for example, a photoresist, that is patterned photolithographically in the usual fashion to expose selectively the N-well region and this is followed by an N-type implantation, typically a donor, such as phosphorous at a dosage of about 10^{12} ions per square centimeter at an accelerating voltage of about seventy five thousand electron volts. This forms a phosphorous-rich layer denoted by the dot-dash line 24 in Figure 3 which underlies the layer 22 in N-well 12. This implantation is used to control the punch-through voltage of P-channel transistors to be formed in this well. Also shown is the mask portion 25 overlying the P-type well 14. After the implantation, the mask 25 is removed.

Similary, to avoid cluttering the drawing unnecessarily, in the subsequent figures the boron-rich layer 22 and the phosphorous-rich layer 24 are not shown since their effects are confined closely to the surface and primarily influence conductivity rather than the conductivity type.

At this stage, it is convenient to form the gate oxide over the active surface of the substrate in conventional fashion, typically by heating the wafer in an oxidizing atmosphere for a time suitable to form the desired thickness of oxide typically between 15 and 17.5 nm. This thickness is generally small enough not to impede significantly in any subsequent ion implantations. There is then deposited over the gate oxide a layer of a material suitable for use as the gate electrode. Typically this may either consist of polysilicon doped to be N-type conductive or a composite of an underlying layer of N-doped polysilicon and overlying layer of a silicide, such as titanium or tantalum silicide, to insure high conductivity to the layer. This layer is thereafter suitably patterned to leave separate portions suitable as gate electrodes 26, 28 over the wells. The resultant is shown in Figure 4 with gate electrodes 26 and 28, overlying the gate oxide

layer 30.

After the gate electrodes have been defined, there follows a blanket implantation of donor ions, such as phosphorous, typically at a dosage of about 10^{13} ions per square centimeter, at an accelerating voltage of about fifty thousand electron volts. This layer will provide the lightly doped drain effect desired in the N-channel device to be formed in the P-type well and will also provide doped regions in the n-well which will ultimately form the source/drain halo regions for the P-channel device.

Next, it is desirable to form dielectric spacer 32 seen in Figure 5 on each side edge of the gate electrodes to insure isolation from the source and drain electrodes eventually to be provided and also to insure that the source and drain regions subsequently to be formed do not extend below the gate electrodes, which would undesirably increase the gate capacitances.

The usual technique can also be used to form these dielectric spacers. Typically there is deposited a conformed layer of silicon oxide deposited at low temperature over each electrode of a thickness comparable to the widest width desired of the spacer. Thereafter this silicon oxide layer is etched anisotropically in an etchant that etches vertically much faster than horizontally so that after the layer portion over the top surface of each gate electrode has been removed there remains the edge portions 32 as shown. Typically reactive ion etching (RIE) is used to achieve the desired anisotropic etching.

At this point, as shown in Figure 6, there is again deposited a layer of masking material, such as a photoresist, that is patterned to cover selectively one of the two wells, leaving the other exposed. As shown, a P-type well is covered with a layer 35, and N-type well 12 is essentially exposed where covered by the gate electrode 26 and its dielectric spacers 32. As previously mentioned, the gate oxide layer 30 is too thin to have any significant masking effect.

There then follows a pair of implantation steps, the order of which is not critical. One is an implantation of an N-type impurity, such as phosphorous, at a dosage of about 10^{13} ions per square centimeter and accelerating voltage of between one hundred thousand and one hundred and twenty thousand electron volts to form a deep implanted layer of phosphorous. The other is an implantation of boron fluoride at a dosage of about 10^{13} boron ions per square centimeter at an accelerating voltage of about fifty thousand electron volts to form a shallower implanted layer of boron that will form the source and drain regions of the P-type channel MOS transistor formed in the N-well. The deeper layer of phosphorous will eventually form in known fashion a halo region underlying the source and drain regions and extending between the source and drain regions at the interface with the channel region underlying the gate electrodes as will be discussed later in connection with Figure 8. After the two successive implantations, the masking layer 35 is removed.

There remains to be formed the source and drain regions of the N-channel transistor to be formed in the P-type well 14. These can be formed in conventional fashion in a manner analogous to that used to form the source and drain regions of the P-channel transistor. This would involve masking the N-type well 12, leaving P-type well 14 exposed in implanting an N-type ion, such as phosphorous or arsenic to form an implanted layer of such ions on opposite sides of the gate electrode, where not blocked by the gate electrode 28 and its dielectric spacers 32.

To avoid the need for the masking step that such selective implantation involves, the preferred embodiment of the invention uses a differential oxide growth technique. This technique depends on the known fact that on a silicon substrate a thermal oxide will grow faster, and so thicker for a given exposure, the more doped the substrate. As a consequence, if the wafer is exposed to an oxidizing ambient in the form that results after completion of the steps illustrated in Figure 6, the N-type well portion 12 will grow a surface oxide thicker where the silicon is exposed than will the surface of P-type well portion 14 where similarly exposed.

As a result, by suitably heating the wafer in an oxidizing ambient, there can be formed over the exposed silicon of the N-well a layer 40 of oxide about 70 nm thick while growing a layer 42 only about 20 nm thick over exposed silicon of the P-type well. Heating the wafer for about an hour at 900 degrees C in an ambient of oxygen that has been bubbled through water to pick up water vapor will produce such results.

Thereafter, without need for providing any additionnal masking, arsenic of a dose of about 10^{13} ions per square centimeter implanted at an accelerating voltage of about sixty thousand electron volts will satisfactorily penetrate the relatively thin oxide layer 42 on the P-type well while being substantially blocked by the thicker oxide layer 40 over the N-type well, as shown by the dashed lines in Figure 7. As a consequence, there is formed an implanted layer of arsenic denoted by the dot-dash line 44 in the substrate on opposite sides of the gate electrode 28, as is shown in Figure 7.

Thereafter, the wafer is heated to a suitable temperature for activating the implanted ions so that they can serve to affect the conductivity type where they are located. The resultant structure in the wafer is depicted in Figure 8. The earlier implanted layer for affecting threshold voltages and

punch-through typically are overcompensated by the later heavier dosages of implanted ions as far as affecting conductivity type in the source and drain regions, but they do influence the properties of the gate electrode-gate oxide interface in the desired fashion.

As shown in Figure 8, the N-type well 12 includes the P-channel transistor comprising heavily doped P-type source/drain regions 101 and 102 provided by the boron implantation step shown in Figure 6. Associated with each of these regions are the halo regions 103, 104 that are less heavily doped P-type because of the compensating effect of the phosphorous implant shown in Figure 6. Underlying the gate electrode 26 is the channel region that includes a thin P-type surface layer 106 resulting from the first boron implant shown in Figure 2. Because of this implant and because the gate electrode includes N-type polysilicon at the interface with the gate electrode, the transistor formed in the N-type well is of the type described as a buried channel P-type transistor. The channel region will also include a deeper more heavily doped N-type layer (not shown) produced by the phosphorous implant depicted in Figure 2 to provide punch-through protection.

In the P-type well 14 there is formed the N-channel transistor comprising heavily doped N-type source/drain regions 110, 112 produced by the arsenic implant shown in Figure 7. Associated with these are the less heavily doped N-type halos 114, 115 resulting from the phosphorous implant shown in Figure 4 before the formation of the spacers on the edges of electrode 28.

It should be apparent that if, instead of the differential oxide growth technique followed by the blanket donor implant used to form the source/drain regions of the N-type transistors, there be employed the double implant technique described in connection with Figure 6, there would be avoided the need for the blanket donor implant discussed in connection with Figure 4 for forming the halos of the N-type transistors. Alternatively, if this blanket implant step were retained, there is avoided the need for the later acceptor implant to form the halos in the N-type transistors.

At this point, the various source and drain electrodes to the source and drain regions and the metallization for connecting such electrodes are provided in conventional fashion so the discussion thereof will be omitted.

Moreover, as mentioned earlier, it is consistent with the invention to form more than a single transistor in any one well.

Claims

1. A process for manufacturing CMOS integrated circuit devices including N-channel and P-channel transistors comprising the steps of:

preparing a silicon wafer (10) on whose active surface are included contiguous P-type and N-type wells (14,12) in which are to be formed N-channel and P-channel transistors, respectively;

blanket implanting the active surface of this wafer relatively shallowly with acceptor ions for establishing the voltage threshold for the transistors to be formed;

selectively implanting the N-type wells (12) relatively deeply with donor ions for providing punch-through protection to the P-channel transistors to be formed in such wells;

forming a gate oxide layer (30) over the active surface of the wafer;

forming gate electrodes (28,26) separately over the gate oxide layer on the P-type and N-type wells;

blanket implanting the wafer with donor ions for use in forming lightly doped source/drain regions (114,115) for the N-channel transistors, and in providing doped regions in the N-wells where source/drain halo regions (103,104) for the P-channel transistors are to be formed;

forming dielectric spacers (32) at the side edges of the gate electrodes (28,26);

selectively implanting the N-type wells (12) with both donor and acceptor ions at accelerating voltages and dosages for forming the source/drain regions (101,102) and associated halo regions (103,104) of the P-channel transistors;

forming oxide layers which are thicker over the N-type wells than over the P-type wells by differential oxide growth resulting from the faster growth of oxide in the more heavily doped silicon; and

blanket implanting donor ions for selectively penetrating the thinner oxide layers over the P-type wells for forming the source/drain regions (110,112) of the N-channel transistors.

2. A process for manufacturing CMOS integrated circuit devices including N-channel and P-channel MOS transistors comprising the steps of:

preparing a silicon wafer (10) on whose active surface are included contiguous P-type and N-type wells (14,12) in which are to be formed N-channel and P-channel transistors, respectively;

blanket implanting the active surface of

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punch-through typically are overcompensated by the later heavier dosages of implanted ions as far as affecting conductivity type in the source and drain regions, but they do influence the properties of the gate electrode-gate oxide interface in the desired fashion.

As shown in Figure 8, the N-type well 12 includes the P-channel transistor comprising heavily doped P-type source/drain regions 101 and 102 provided by the boron implantation step shown in Figure 6. Associated with each of these regions are the halo regions 103, 104 that are less heavily doped P-type because of the compensating effect of the phosphorous implant shown in Figure 6. Underlying the gate electrode 26 is the channel region that includes a thin P-type surface layer 106 resulting from the first boron implant shown in Figure 2. Because of this implant and because the gate electrode includes N-type polysilicon at the interface with the gate electrode, the transistor formed in the N-type well is of the type described as a buried channel P-type transistor. The channel region will also include a deeper more heavily doped N-type layer (not shown) produced by the phosphorous implant depicted in Figure 2 to provide punch-through protection.

In the P-type well 14 there is formed the N-channel transistor comprising heavily doped N-type source/drain regions 110, 112 produced by the arsenic implant shown in Figure 7. Associated with these are the less heavily doped N-type halos 114, 115 resulting from the phosphorous implant shown in Figure 4 before the formation of the spacers on the edges of electrode 28.

It should be apparent that if, instead of the differential oxide growth technique followed by the blanket donor implant used to form the source/drain regions of the N-type transistors, there be employed the double implant technique described in connection with Figure 6, there would be avoided the need for the blanket donor implant discussed in connection with Figure 4 for forming the halos of the N-type transistors. Alternatively, if this blanket implant step were retained, there is avoided the need for the later acceptor implant to form the halos in the N-type transistors.

At this point, the various source and drain electrodes to the source and drain regions and the metallization for connecting such electrodes are provided in conventional fashion so the discussion thereof will be omitted.

Moreover, as mentioned earlier, it is consistent with the invention to form more than a single transistor in any one well.

Claims

1. A process for manufacturing CMOS integrated circuit devices including N-channel and P-channel transistors comprising the steps of:

preparing a silicon wafer (10) on whose active surface are included contiguous P-type and N-type wells (14,12) in which are to be formed N-channel and P-channel transistors, respectively;

blanket implanting the active surface of this wafer relatively shallowly with acceptor ions for establishing the voltage threshold for the transistors to be formed;

selectively implanting the N-type wells (12) relatively deeply with donor ions for providing punch-through protection to the P-channel transistors to be formed in such wells;

forming a gate oxide layer (30) over the active surface of the wafer;

forming gate electrodes (28,26) separately over the gate oxide layer on the P-type and N-type wells;

blanket implanting the wafer with donor ions for use in forming lightly doped source/drain regions (114,115) for the N-channel transistors, and in providing doped regions in the N-wells where source/drain halo regions (103,104) for the P-channel transistors are to be formed;

forming dielectric spacers (32) at the side edges of the gate electrodes (28,26);

selectively implanting the N-type wells (12) with both donor and acceptor ions at accelerating voltages and dosages for forming the source/drain regions (101,102) and associated halo regions (103,104) of the P-channel transistors;

forming oxide layers which are thicker over the N-type wells than over the P-type wells by differential oxide growth resulting from the faster growth of oxide in the more heavily doped silicon; and

blanket implanting donor ions for selectively penetrating the thinner oxide layers over the P-type wells for forming the source/drain regions (110,112) of the N-channel transistors.

2. A process for manufacturing CMOS integrated circuit devices including N-channel and P-channel MOS transistors comprising the steps of:

preparing a silicon wafer (10) on whose active surface are included contiguous P-type and N-type wells (14,12) in which are to be formed N-channel and P-channel transistors, respectively;

blanket implanting the active surface of

this wafer relatively shallowly with acceptor ions for establishing the voltage threshold for the transistors to be formed;

selectively implanting the N-type wells (12) relatively deeply with donor ions for providing punch-through protection to the P-channel transistors to be formed in such wells;

forming a gate oxide layer (30) over the active surface of the wafer;

forming gate electrodes (28,26) separately over the gate oxide layer on the P-type and N-type wells;

blanket implanting the wafer with donor ions for use in forming lightly doped source/drain regions (114,115) for the N-channel transistors and in providing doped regions in the N-wells where source/drain halo regions (101,102) for the P-channel transistors are to be formed;

forming dielectric spacers (32) at the side edges of the gate electrodes;

selectively implanting the N-type wells (12) with both donor and acceptor ions at accelerating voltages and dosages for forming the source/drain regions (101,102) and associated halo regions (103,104) of the P-channel transistors; and

selectively implanting the P-type wells (12) with donor ions at an accelerating voltage and dosage for forming source/drain regions (110,112) of the N-channel transistors.

3. A process for manufacturing CMOS integrated circuit devices including N-channel and P-channel transistors comprising the steps of:

preparing a silicon wafer (10) on whose active surface are included contiguous P-type and N-type wells (14,12) in which are to be formed N-channel and P-channel transistors, respectively;

blanket implanting the active surface of this wafer relatively shallowly with acceptor ions for establishing the voltage threshold for the transistors to be formed;

selectively implanting the N-type wells (12) relatively deeply with donor ions for providing punch-through protection to the P-channel transistors to be formed in such wells;

forming a gate oxide layer (30) over the active surface of the wafer;

forming gate electrodes (28,26) separately over the gate oxide layer on the P-type and N-type wells;

blanket implanting the wafer with donor ions for use in forming lightly doped source/drain regions (114,115) for the N-channel transistors and in providing doped regions in the N-wells which will form source/drain halo regions (101,102) for the P-channel transistors;

forming dielectric spacers (32) at the side edges of the gate electrodes;

selectively implanting the N-type wells (12) with both donor and acceptor ions at accelerating voltages and dosages for forming the source/drain regions (101,102) and associated halo regions of the P-channel transistors; and

selectively implanting the P-type wells (14) with both donor and acceptor ions at accelerating voltages and dosages for forming source/drain regions (110,112) and associated halo regions (114,115) of the N-channel transistors.

4. A process according to claim 1, 2 or 3, in which each of the gate electrodes (28,26) includes a donor-doped silicon layer at its interface with the gate oxide layer.

Patentansprüche

1. Verfahren zur Herstellung von CMOS-integrierten Schaltungseinrichtungen, die N-Kanal- und P-Kanal-Transistoren enthalten, mit den folgenden Schritten:

eine Siliziumscheibe (10) bzw. ein Siliziumwafer (10), an dessen aktiver Oberfläche aneinander angrenzende P-Typ- und N-Typ-Wannen (14, 12) enthalten sind, in welchen jeweils N-Kanal- und P-Kanal-Transistoren ausgebildet werden sollen, wird vorbereitet;

die aktive Oberfläche der Scheibe wird relativ flach mit Akzeptor-Ionen überdeckend implantiert, um die Schwellspannung für die auszubildenden Transistoren einzurichten;

die N-Typ-Wannen (12) werden relativ tief mit Donor-Ionen selektiv implantiert, um einen Druchgreifschutz für die P-Kanal-Transistoren, die in derartigen Wannen auszubilden sind, zur Verfügung zu stellen;

eine Gate-Oxidschicht (30) wird über der aktiven Oberfläche der Scheibe ausgebildet;

Gate-Elektroden (28, 26) werden getrennt über der Gate-Oxidschicht auf den P-Typ- und N-Typ-Wannen ausgebildet;

der Wafer wird mit Donor-Ionen überdekkend implantiert zur Verwendung beim Ausbilden leicht dotierter Source-/Drain-Bereiche (114, 115) für die N-Kanal-Transistoren, und um dotierte Bereiche in den N-Wannen zur Verfügung zu stellen, wo Source-/Drain-Halo- bzw. Hofbereiche (103, 104) für die P-Kanal-Transistoren ausgebildet werden sollen;

an den Seitenkanten der Gate-Elektroden (28, 26) werden dielektrische Zwischenbereiche (32) ausgebildet;

die N-Typ-Wannen (12) werden sowohl mit

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Donor- als auch Akzeptor-Ionen bei Beschleunigungsspannungen und Dosierungen selektiv implantiert, um die Source-/Drain-Bereiche (101, 102) und verbundenen Halo- bzw. Hof-Bereiche (103, 104) der P-Kanal-Transistoren auszubilden;

Oxidschichten, welche über den N-Typ-Wannen dicker sind als über den P-Typ-Wannen, werden durch differentielles Oxidwachstum ausgebildet, das durch das schnellere Wachstum von Oxid in stärker dotiertem Silizium resultiert; und

Donor-Ionen werden zum selektiven Durchdringen der dünneren Oxidschicht über den P-Typ-Wannen zur Ausbildung der Source-/Drain-Bereiche (110, 112) der N-Kanal-Transistoren überdeckend implantiert.

2. Verfahren zur Herstellung von CMOS-integrierten Schaltungseinrichtungen, die N-Kanal- und P-Kanal-MOS-Transistoren enthalten, mit den folgenden Schritten:

eine Siliziumscheibe (10) bzw. ein Siliziumwafer (10), an dessen aktiver Oberfläche aneinander angrenzende P-Typ- und N-Typ-Wannen (14, 12) enthalten sind, in welchen jeweils N-Kanal- und P-Kanal-Transistoren ausgebildet werden sollen, wird vorbereitet;

die aktive Oberfläche der Scheibe wird relativ flach mit Akzeptor-Ionen überdeckend implantiert, um die Schwellspannung für die auszubildenden Transistoren einzurichten;

die N-Typ-Wannen (12) werden relativ tief mit Donor-Ionen selektiv implantiert, um einen Druchgreifschutz für die P-Kanal-Transistoren, die in derartigen Wannen auszubilden sind, zur Verfügung zu stellen;

eine Gate-Oxidschicht (30) wird über der aktiven Oberfläche der Scheibe ausgebildet;

Gate-Elektroden (28, 26) werden getrennt über der Gate-Oxidschicht auf den P-Typ- und N-Typ-Wannen ausgebildet;

der Wafer wird mit Donor-Ionen überdekkend implantiert zur Verwendung beim Ausbilden leicht dotierter Source-/Drain-Bereiche (114, 115) für die N-Kanal-Transistoren, und um dotierte Bereiche in den N-Wannen zur Verfügung zu stellen, wo Source-/Drain-Halo- bzw. Hofbereiche (101, 102) für die P-Kanal-Transistoren ausgebildet werden sollen;

an den Seitenkanten der Gate-Elektroden werden dielektrische Zwischenbereiche (32) ausgebildet;

die N-Typ-Wannen (12) werden sowohl mit Donor- als auch Akzeptor-Ionen bei Beschleunigungsspannungen und Dosierungen selektiv implantiert, um die Source-/Drain-Bereiche (101, 102) und verbundenen Halo- bzw. Hof-Bereiche (103, 104) der P-Kanal-Transistoren auszubilden; und

die P-Typ-Wannen (12) werden selektiv mit Donor-Ionen bei Beschleunigungsspannungen und Dosierungen implantiert, um Source-/Drain-Bereiche (110, 112) für die N-Kanal-Transistoren auszubilden.

3. Verfahren zur Herstellung von CMOS-integrierten Schaltungseinrichtungen, die N-Kanal- und P-Kanal-Transistoren enthalten, mit den folgenden Schritten:

eine Siliziumscheibe (10) bzw. ein Siliziumwafer (10), an dessen aktiver Oberfläche aneinander angrenzende P-Typ- und N-Typ-Wannen (14, 12) enthalten sind, in welchen jeweils N-Kanal- und P-Kanal-Transistoren ausgebildet werden sollen, wird vorbereitet;

die aktive Oberfläche der Scheibe wird relativ flach mit Akzeptor-Ionen überdeckend implantiert, um die Schwellspannung für die auszubildenden Transistoren einzurichten;

die N-Typ-Wannen (12) werden relativ tief mit Donor-Ionen selektiv implantiert, um einen Druchgreifschutz für die P-Kanal-Transistoren, die in derartigen Wannen auszubilden sind, zur Verfügung zu stellen;

eine Gate-Oxidschicht (30) wird über der aktiven Oberfläche der Scheibe ausgebildet;

Gate-Elektroden (28, 26) werden getrennt über der Gate-Oxidschicht auf den P-Typ- und N-Typ-Wannen ausgebildet;

der Wafer wird mit Donor-Ionen überdekkend implantiert zur Verwendung beim Ausbilden leicht dotierter Source-/Drain-Bereiche (114, 115) für die N-Kanal-Transistoren, und um dotierte Bereiche in den N-Wannen zur Verfügung zu stellen, welche Source-/Drain-Halo- bzw. Hofbereiche (101, 102) ausbilden werden für die P-Kanal-Transistoren;

an den Seitenkanten der Gate-Elektroden werden dielektrische Zwischenbereiche (32) ausgebildet;

die N-Typ-Wannen (12) werden sowohl mit Donor- als auch Akzeptor-Ionen bei Beschleunigungsspannungen und Dosierungen selektiv implantiert, um die Source-/Drain-Bereiche und verbundenen Halo- bzw. Hof-Bereiche der P-Kanal-Transistoren auszubilden; und

die P-Typ-Wannen (14) werden sowohl mit Donor- als auch mit Akzeptor-Ionen bei Beschleunigungsspannungen und Dosierungen selektiv implantiert, um die Source-/Drain-Bereiche (110, 112) und verbundene Halo- bzw. Hof-Bereiche (114, 115) der N-Kanal-Transistoren auszubilden.

* C L M S *

4. Verfahren nach einem der Ansprüche 1, 2 oder 3, in welchem jede der Gate-Elektroden (28, 26) eine Donor-dotierte Siliziumschicht an seiner Grenzschicht zu der Gate-Oxidschicht enthält.

Revendications

1. Un procédé de fabrication de dispositifs à circuits intégrés CMOS comportant des transistors à canal N et à canal P, comprenant les étapes suivantes :

on prépare une tranche de silicium (10) dont la surface active contient des caissons contigus de type P et de type N (14, 12) dans lesquels doivent être formés respectivement des transistors à canal N et à canal P;

on implante dans la totalité de la surface active de cette tranche des ions accepteurs, avec une profondeur de pénétration relativement faible, pour établir la tension de seuil pour les transistors à former;

on implante sélectivement dans les caissons de type N (12) des ions donneurs, de façon relativement profonde, pour procurer une protection contre le percement aux transistors à canal P devant être formés dans de tels caissons;

on forme une couche d'oxyde de grille (30) sur la surface active de la tranche;

on forme séparément des électrodes de grille (28, 26) sur la couche d'oxyde de grille, sur les caissons de type P et de type N;

on implante dans la totalité de la tranche des ions donneurs, pour l'utilisation dans la formation de régions de source/drain faiblement dopées (114, 115), pour les transistors à canal N, et dans la formation de régions dopées dans les caissons N dans lesquels on doit former des régions de halo de source/drain (103, 104) pour les transistors à canal P;

on forme des éléments d'espacement diélectriques (32) sur les bords latéraux des électrodes de grille (28, 26);

on implante sélectivement dans les caissons de type N (12) à la fois des ions donneurs et accepteurs, avec des tensions d'accélération et des doses appropriées pour la formation des régions de source/drain (101, 102) et des régions de halo associées (103, 104) des transistors à canal P;

on forme des couches d'oxyde qui sont plus épaisses sur les caissons de type N que sur les caissons de type P, par croissance d'oxyde différentielle résultant de la croissance plus rapide de l'oxyde dans le silicium plus fortement dopé; et

on effectue une implantation générale d'ions donneurs pour qu'ils pénètrent sélectivement dans les couches d'oxyde plus minces se trouvant sur les caissons de type P, pour former les régions de source/drain (110, 112) des transistors à canal N.

2. Un procédé de fabrication de dispositifs à circuits intégrés CMOS comportant des transistors MOS à canal N et à canal P, comprenant les étapes suivantes :

on prépare une tranche de silicium (10) dont la surface active contient des caissons contigus de type P et de type N (14, 12) dans lesquels doivent être formés respectivement des transistors à canal N et à canal P;

on implante dans la totalité de la surface active de cette tranche des ions accepteurs, avec une profondeur de pénétration relativement faible, pour établir la tension de seuil pour les transistors à former;

on implante sélectivement dans les caissons de type N (12) des ions donneurs, de façon relativement profonde, pour procurer une protection contre le percement aux transistors à canal P devant être formés dans de tels caissons;

on forme une couche d'oxyde de grille (30) sur la surface active de la tranche;

on forme séparément des électrodes de grille (28, 26) sur la couche d'oxyde de grille, sur les caissons de type P et de type N;

on implante dans la totalité de la tranche des ions donneurs, pour l'utilisation dans la formation de régions de source/drain faiblement dopées (114, 115), pour les transistors à canal N, et dans la formation de régions dopées dans les caissons N dans lesquels on doit former des régions de halo de source/drain (101, 102) pour les transistors à canal P; et

on implante sélectivement des ions donneurs dans les caissons de type P (12), avec une tension d'accélération et une dose appropriées pour former des régions de source/drain (110, 112) pour les transistors à canal N.

3. Un procédé de fabrication de dispositifs à circuits intégrés CMOS comportant des transistors à canal N et à canal P, comprenant les étapes suivantes :

on prépare une tranche de silicium (10) dont la surface active contient des caissons contigus de type P et de type N (14, 12) dans lesquels doivent être formés respectivement des transistors à canal N et à canal P;

on implante dans la totalité de la surface active de cette tranche des ions accepteurs,

avec une profondeur de pénétration relativement faible, pour établir la tension de seuil pour les transistors à former;

on implante sélectivement dans les caissons de type N (12) des ions donneurs, de façon relativement profonde, pour procurer une protection contre le percement aux transistors à canal P devant être formés dans de tels caissons;

on forme une couche d'oxyde de grille (30) sur la surface active de la tranche;

on forme séparément des électrodes de grille (28, 26) sur la couche d'oxyde de grille, sur les caissons de type et de type N;

on implante des ions donneurs dans la totalité de la tranche pour l'utilisation dans la formation de régions de source/drain faiblement dopées (114, 115) pour les transistors à canal N, et dans la formation de régions dopées dans les caissons N qui formeront des régions de halo de source/drain (101, 102) pour les transistors à canal P;

on forme des éléments d'espacement diélectriques (32) sur les bords latéraux des électrodes de grille;

on implante sélectivement dans les caissons de type N (12) à la fois des ions donneurs et accepteurs, avec des tensions d'accélération et des doses appropriées pour former les régions de source/drain (101, 102) et les régions de halo associées des transistors à canal P; et

on implante sélectivement dans les caissons de type P (14) à la fois des ions donneurs et accepteurs, avec des tensions d'accélération et des doses appropriées pour former des régions de source/drain (110, 112) et des régions de halo associées (114, 115) des transistors à canal N.

4. Un procédé selon la revendication 1, 2 ou 3, dans lequel chacune des électrodes de grille (28, 26) comprend une couche de silicium dopée avec des donneurs à son interface avec la couche d'oxyde de grille.