

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
a substrate;
a plurality of structures that are vertically spaced apart from each other in a stack on the substrate, wherein one of the plurality of structures comprises:
a semiconductor pattern that comprises a first impurity region, a channel region, and a second impurity region; and
a first electrode of a capacitor that is connected to the second impurity region, and
wherein each of the plurality of structures extends horizontally in a first direction that is parallel to a top surface of the substrate.
2. The semiconductor memory device of claim 1,
wherein the semiconductor pattern and the first electrode comprise respective surfaces that are coplanar, and
wherein the semiconductor pattern and the first electrode comprise respective extension axes that are parallel to the first direction and are coaxial.
3. The semiconductor memory device of claim 1, wherein the plurality of structures overlap each other in a vertical second direction that is perpendicular to the top surface of the substrate.
4. The semiconductor memory device of claim 1, further comprising:
a first conductive line connected to the first impurity region of the semiconductor pattern; and
a second conductive line that surrounds a periphery of the channel region of the semiconductor pattern,
wherein the first conductive line extends horizontally in a second direction that crosses the first direction,
wherein the channel region comprises one among a plurality of channel regions of the plurality of structures, and

wherein the second conductive line extends vertically in a third direction that is perpendicular to the top surface of the substrate, to surround peripheries of the plurality of channel regions.

5. The semiconductor memory device of claim 4, further comprising a back-gate line,

wherein the back-gate line extends parallel to the second conductive line in the third direction, to surround the peripheries of the plurality of channel regions.

6. The semiconductor memory device of claim 1,

wherein the capacitor further comprises:

a dielectric layer that is on the first electrode; and

a second electrode that is on the dielectric layer,

wherein the first electrode comprises one among a plurality of first electrodes of the plurality of structures,

wherein the capacitor comprises one among a plurality of capacitors of the semiconductor memory device, and

wherein the second electrode comprises a common electrode of the plurality of capacitors.

7. The semiconductor memory device of claim 1, further comprising a supporting layer that is connected to an end portion of the first electrode, wherein the supporting layer is configured to structurally support the plurality of structures.