Process for packaging components, and packaged components

Description

Field of the invention

The invention relates to a process for packaging components and to a component packaged in this way in general, and to a wafer level packaging process and a component packaged in this way in particular.

Background of the invention

For many technical applications, there is a need for hermetically packaged chips, since it is in this way possible, for example, to protect the sensitive integrated circuits on a semiconductor substrate. However, the packaging is at least equally important for optical or micro-mechanical components.

There are known processes in which the chips are first of all divided from the wafer assembly and then packaged individually. This is an extremely complex process which is scarcely suitable for the mass production of sensitive components. In particular, the integrated circuits or other components are not (yet) protected when they are being divided from the wafer, and consequently they can become soiled and/or be destroyed during the sawing operation.

There are also known processes in which the components are first of all packaged at wafer level and then divided. These processes are known as wafer level packaging (WLP).

The prior art disclosed a number of such processes.

However, with wafer level packaging it is difficult to contact-connect the integrated circuits, since any connection contacts are typically covered by a covering substrate. This will be illustrated on the basis of the process described below.

The known processes generally work on the assumption that the connections to the contact regions on the chips or at the integrated circuits can be produced directly, as can be achieved without problems, for example, in the case of memory chips.

However, this takes no account of the fact that, for example in the case of chips with an integrated sensor or optical component, the optically active surface in the mounted state, for example on a printed circuit board, has to remain uncovered.

In this respect, WO 99/40624 has disclosed a process in which it is attempted to eliminate the problems outlined above by the connection contacts which are present at the active component being routed from the active side onto the opposite underside of the wafer or chip. The further contact-connection of the connection contacts routed downwards can then be carried out in a known way.

Moreover, a similar process is described in "Wafer Level Chip Scale Packaging: Benefits for Integrated Passive Devices", Clearfield, H.M.; Young, J.L.; Wijeyesekera, S.D.; Logan, E.A.; IEEE Transactions on Advanced Packaging, Vol. 23, No. 2, pages 247-251.

The abovementioned process is distinguished by the fact that, after a glass covering has been applied to the optically active front surface of a wafer, trenches which divide the wafer into individual chip regions are produced along the underside of the wafer. During the production of the trenches, the connection contact locations located on the active side of the wafer, in each case on the transition region between two chips, are divided and thereby uncovered in the trenches. To completely package the wafer or chips, after the trenches have been produced, a piece of glass is adhesively bonded over the trenches and is then cut into in a suitable way such that the trenches in the wafer and the connection contact locations are once again freely accessible. This is followed by deposition of contact tracks in the trenches which have been produced, which is intended to effect contact-connection of the connection contact locations and to lay the contact location onto the back surface of the packaged chip.

Although the proposed process leads to what is known as through-contacting of the connection contacts from the active front surface of the chip or wafer to the passive back surface, this gives rise to a number of significant drawbacks, making chips which have been produced using the process under discussion disproportionately expensive.

One reason for this is the fact that the trenches which are to be produced in the known process are significantly wider than those which would be considered standard for normal dicing of a wafer. The result of this is that the distances between the chips or the integrated circuits have to be relatively great, and consequently there is space for fewer chips on a wafer.

If only for this reason, the known process already gives a relatively low chip yield from a semiconductor wafer. Furthermore, the proposed production process is also relatively slow. This is related in particular to the fact that the trenches have to be ground in sequentially and also that what is known as the dicing saw can only operate at a relatively slow advance rate during production of the trenches. Apart from all this, the wear to the saw blades is also high. The dicing saws which have to be used, for this reason and on account of the high demands imposed on the dimensional accuracy of the mechanical process described and also the considerable machine costs, are very expensive.

One significant problem of the process described in WO 99/40624 is also that the uncovering of the connection contacts when grinding the trenches is effected by a dicing operation. Dicing of the connection contacts of this type, as has been mentioned above, requires an extremely high dimensional accuracy, since otherwise at least part of the contact can be destroyed. However, even if accurate cutting of the connection contact is achieved, it is not easy to produce a contact connection using the connection contacts which have been uncovered in this way. The reasons for this are in particular that the contact-connection according to the prior art is to be effected by deposition of contact tracks on the oblique walls of the trenches in the wafer, but uniform and therefore targeted deposition is only possible at a steep to perpendicular angle to the deposition direction.

When sawing along the contacts, a further particular drawback is that a number of interfaces are at least temporarily uncovered, which can lead to corrosion and

diffusion and can therefore have a significant adverse effect on the service life of the components.

Further processes for the through-contacting of chips are also described in "Future Systems-on-Silicon LSI Chips", Koyanagi, M; Kurino, H; Lee, K.W.; Sakuma, K., IEEE Micro, July-August 1998, pages 17-22, WO 98/52225 and DE 197 46 641. However, these processes are not suitable for the packaging of, for example, optical chips.

A further improved wafer level packaging process is known from WO 03/019653 A2, which is hereby incorporated in its entirety by reference in the subject matter of the present disclosure.

In the process described in that document, the contacts, after packaging, are made accessible again through passages through which the contacts are then contact-connected, for example by means of what are known as ball grid arrays. The drawbacks described above can be substantially avoided in this process.

Nevertheless, under certain circumstances a problem may be presented by the fact that the ball grid arrays generally contain a lead-tin solder, the melting point of which is approximately 230°C, and consequently the thermal stability of a chip produced in this way is insufficient for certain applications, or sensitive components are subject to excessive thermal loading during mounting. Furthermore, thermomechanical coupling between the connections with ball grid array and the semiconductor components can lead to problems in sensitive components.

In any case, under certain circumstances it is desirable to be able to make do without lead-containing solder.

Furthermore, it is desirable for the efficiency and yield of the processes described to be improved further and for the range of applications for the chips produced to be widened.

General description of the invention

Therefore, the invention is based on the object of providing a process of the generic type which works efficiently and inexpensively.

A further object of the invention is to provide a process which ensures a high yield and is in particular also suitable for optical and/or micro-mechanical components.

Yet another object of the invention is to provide a process and a component which achieve improved thermomechanical decoupling of the connections from the functional regions.

Yet another object of the invention is to provide inexpensive and temperature-resistant components of a high quality and stability.

Yet another object of the invention is to provide a process and a component which avoid or at least alleviate the drawbacks of the prior art.

The object is achieved in a surprisingly simple way by the subject matter of the independent claims. Advantageous refinements of the invention are defined in the subclaims.

According to the invention, components undergo wafer level packaging and contact connection in the following way.

A base substrate, which has a functional side and a back surface on the opposite side from the functional side, is permanently joined, by means of the functional side, to a covering substrate at wafer level. The functional side is characterized in that a multiplicity of functional regions spaced apart from one another are arranged thereon. More specifically, there is one functional region per chip or die that is to be produced. A functional region is to be understood as meaning a region having functional elements, e.g. integrated circuits or other electronic, optical, electro-optical, micro-mechanical, micro-opto-mechanical or similar components.

For example, the functional region may, therefore, comprise an optical sensor. Also by way of example, the base substrate is, for example, a silicon semiconductor wafer with integrated circuits. However, other materials are also possible for the base substrate, such as for example gallium arsenide or indium phosphide.

The functional regions are now in each case encapsulated in a hermetically or quasi-hermetically sealed manner by the joining of the two substrates. One possible joining technique is adhesive bonding, for example using epoxy, but anodic bonding is also possible. For anodic bonding, it may be advantageous for a bonding layer (bond layer), e.g. in the form of a layer of evaporation-coating glass, to be applied to at least one of the two substrates prior to joining. A bonding layer created in this way can also be used for direct bonding.

With regard to joining using epoxy, it should also be noted that this only achieves a limited hermetic seal. Therefore,

in the context of the present description, a join of this nature is referred to as quasi-hermetic.

Furthermore, the base substrate has contact surfaces (known as contact pads) on its functional side, and these contact surfaces, after the substrates have been joined, are uncovered from a back surface of the base substrate, this back surface being on the opposite side from the functional side. For this purpose, contact-connection recesses are produced in the base substrate above the contact surfaces, in particular by etching. The contact-connection recesses are also known to the person skilled in the art as vias for making through-contact through the base substrate.

At a further subsequent stage, the wafer assembly formed at least from base substrate and covering substrate is diced into the chips or dies, in particular by sawing, along predefined cutting lines between the functional regions. If a suitable passivation is used, such as for example a patternable evaporation-coating glass layer with a thickness of preferably 0.01 μm to 100 μm, typically 8 μm, individual chips which are in each case packaged in a hermetically or quasi-hermetically sealed manner are formed. This encapsulation process which works at wafer level is much more efficient than individual encapsulation.

At a further, later stage, the component has a body region and connection regions, the connection regions being adjacent to the contact-connection recesses, and the component, in particular the base substrate, being thinned either in the body region or in the connection regions until different thicknesses have been reached in the connection regions and the body regions.

In other words, the base substrate is divided into body regions and connection regions, with the body regions in each case extending laterally over the functional regions and forming part of the respective package for the subsequent chip. The connection regions laterally adjoin the contact-connection recesses or vias. The particular feature now is that the base substrate is thinned to a greater extent in the connection regions than in the body regions, or vice versa.

This advantageously increases the space for contact-connection. Furthermore, the process according to the invention creates excellent thermo-mechanical decoupling between the connections and the functional region.

If appropriate, the base substrate is thinned down to a thickness of zero, i.e. is removed altogether.

At a further, subsequent stage, the chips are preferably inserted into a circuit carrier and the contact surfaces or contact redistribution elements, which are electrically conductively connected to the contact surfaces, are connected to corresponding contact elements of the circuit carrier by means of wire bonding on the back surface of the base substrate. Consequently, the etched-clear contact surfaces or the contact redistribution elements are in particular only contact-connected in the state in which the individual components have been diced.

In the case of wire bonding, electrically conductive, thin, substantially round wires, for example of aluminium or gold, are welded to the contact surfaces without the use of solder. For this purpose, the wire is preferably introduced into a ram and pressed onto the contact surfaces under the action of force. The actual welding is preferably carried

out cold and/or by means of ultrasound. This process is distinguished in particular by its reliability and the quality of the connection which is created. However, the application of ball grid arrays as contact elements for the contact connection of the contact surfaces or contact redistribution elements is also within the scope of the invention.

A further advantage of wire bonding is that this represents a very simple and inexpensive process and, furthermore, is more thermally stable than connections produced by means of solder balls or what are known as ball grid arrays formed from solder. Also, there is scarcely any thermal loading on the components during the wire bonding.

A further particular benefit of the invention is that the contact connection, in particular the wire bonding, is carried out on the back surface, so that the process, by way of example, can also be used for optical components with a transparent covering substrate, in particular made from glass. Of course, the process is not restricted to this, but rather the covering substrate may also consist of another material, such as metal or a semiconductor, depending on the particular application area. At any rate, it has been found that back-surface contact connection using the process according to the invention can be carried out in a simple and efficient way.

A further advantage is that the process produces particularly little dust. In particular, the under certain circumstances very sensitive functional regions are protected as early as by the first process step as a result of the application of the covering substrate.

It is optionally possible for enlargement elements, known as contact pad extensions, to be applied to the contact surfaces on the base substrate on the functional side before the base substrate is joined to the covering substrate. This increases the contact surface area and facilitates access using the bonding ram. In this case, the contact-connection recesses may if appropriate extend over the enlargement elements.

It is preferable for the base substrate to be thinned uniformly after it has been joined to the covering substrate, for example by mechanical grinding and/or etching, in order to reach a reduced component thickness.

The uncovering of the contact surfaces is carried out in particular by means of patterned etching of the base substrate, e.g. by means of a lithography process. Furthermore, etching can be carried out by wet-chemical means or by means of a plasma technique. Processes of this type are fundamentally known to the person skilled in the art.

Furthermore, it is advantageous for a passivation layer to be applied to the back surface of the base substrate. The passivation layer is in particular patterned, with the contact surfaces being substantially uncovered. This can be achieved either by the passivation layer being applied in ready-patterned form, e.g. using a mask, or by the passivation layer being applied uniformly to the back surface of the base substrate and then being patterned.

This has the advantage that the base substrate, and in particular the interfaces with the covering substrate and the silicon oxide layer which is present on the functional side in the case of silicon semiconductor substrates, are

protected from environmental influences, such as for example oxidation. Moreover, the silicon oxide layer can be used as an etching stop mask when etching the contact-connection recesses or contact-connection passages, but is then opened up on the back surface over the contact surface.

A suitable passivation layer is in particular a layer of glass applied by evaporation coating or a photographically patternable plastic layer, e.g. BCB. The passivation layer preferably extends as far as the edge region of the contact surfaces. Furthermore, still further passivation layers can be provided if required.

According to a particular embodiment, the contact surfaces and/or the contact redistribution elements, after they have been uncovered, are covered on the back surface with a metal layer, e.g. a layer of gold, by electroplating or electroless means. This improves the surface quality of the contact surfaces, so that the reliability of the wire bonding can be improved further.

Furthermore, it is advantageous for the base substrate to be etched on the back surface along the predefined cutting lines, so as to define trenches or what are known as sawing streets, which extend along both sides of the cutting lines and along which the wafer is sawn into the chips.

Furthermore, the thinning of the base substrate in the connection regions is carried out in particular before the contact surfaces have been joined to the contact elements of the circuit carrier by means of wire bonding.

This results in the advantage of more space being created to enable the wire bonding to be carried out from the back

surface using the bonding ram. This is because the openings that are present in known processes are typically so small that the wire bonding would at least be made more difficult if not altogether impossible.

According to a particularly simple embodiment, the contact-connection recesses or vias, the connection regions and/or the sawing streets are produced in a single step. This allows the process to be simplified still further.

It is preferable for the base substrate first of all to be thinned uniformly in a first step, for example by grinding, and then to be thinned still further in the connection regions or the body regions, e.g. by means of photolithographic patterned etching, in a second step which follows the first step, so that it becomes thinner in these regions than in the respective other regions, so that in addition to the contact-connection recesses further regions having a different thickness, in particular a lower thickness, of the base substrate than that produced by uniform thinning are produced.

In this context, the term thinning of the base substrate is fundamentally also to be understood as encompassing thinning down to a thickness of zero, i.e. complete removal in the corresponding region. However, it is also possible to produce at least three different thickness regions in the body region, connection region and at the contact-connection recess.

If the base substrate is thinned down to a thickness of zero in the connection regions, it is advantageous that the contact-connection of the connections can be particularly successfully mechanically decoupled from the functional region. Therefore, when connecting the connections or

connection wires, e.g. by means of wire bonding, no stress or only very little stress is transmitted to the functional region. This inter alia makes it possible to avoid an increased dark current in sensitive image sensors.

However, even if solder balls are used as contact element, the location of contact between the solder balls and the component is thermomechanically decoupled from the functional region, so that the mechanical stress during the thermal cycles encountered in use is not transmitted or is scarcely transmitted to the functional region.

Furthermore, it is particularly preferred to produce connection strips which extend parallel, in elongate form, to the predefined cutting lines. The base substrate is once again thinned to a greater extent in the connection strips than in the body regions. The advantage in this context is that there is no need to create a dedicated connection region for each contact-connection recess, but rather a plurality of contact-connection recesses adjoin the same connection strip. In particular, the connection strip extends substantially from one cutting line to the next, in particular over the entire wafer, so that a pattern of strips is produced over the wafer.

It is preferable for the connection regions to be produced in such a manner that they extend at least from the contact-connection recesses to the sawing streets or the predefined cutting lines. In other words, the sawing streets and the connection regions can form a single region, so that in particular the base substrate is completely removed between contact surfaces of adjacent chips. This makes it possible to save further working steps.

The process according to the invention is also particularly suitable for components having a functional region enclosed in a cavity, e.g. an MEMS or MOEMS component. In particular for this purpose, before the base substrate is joined to the covering substrate, the covering substrate is provided with recesses over the functional regions, so that after the base substrate has been joined to the covering substrate, cavities in which the functional regions are then enclosed are formed between these two substrates.

In addition to the process, a further subject matter of the invention is also the component producible by the process as a chip after the dicing operation, the intermediate product at wafer level prior to dicing and a circuit arrangement having a circuit carrier and the diced component which is installed therein and electrically connected to it by means of wire bonding.

The diced, packaged component, which is in particular an electronic, optical, electro-optical, micro-electro-mechanical or micro-opto-electro-mechanical component, accordingly comprises according to the invention:

a base substrate having a functional side, on which a functional region of the component is arranged, and a back surface on the opposite side from the functional side,

a covering substrate, which is permanently joined to the base substrate on the functional side of the latter, the covering substrate extending over the functional region, and the join between the base substrate and the covering substrate, or the joining layer, surrounding the functional region in such a manner that a hermetically or quasi-hermetically sealed housing is formed around the functional region, and

contact surfaces on the base substrate, which are electrically connected to the functional region in particular through the housing.

Furthermore, the base substrate comprises, in the region of the contact surfaces, contact-connection recesses through which the contact surfaces are or can be contact-connected from outside the housing and from the back surface of the base substrate or through the base substrate,

the base substrate being divided into a body region and connection regions, the body region extending laterally over the functional region and forming part of the housing, and the connection regions being laterally offset with respect to the contact-connection recesses, in particular adjoining the latter, and

the component, in particular the base substrate, having different thicknesses in the body region and the connection regions, or the base substrate being thinned to a greater extent in the body region or the connection regions, in particular, if appropriate, being removed altogether.

Furthermore, after dicing, the component has narrow sides at which it is separated out of the wafer assembly, and in this respect the connection regions extend at least from the contact-connection recesses to the narrow sides.

Otherwise, reference is also made to the process features.

In the text which follows, the invention is explained in more detail on the basis of exemplary embodiments and with reference to the drawings, in which identical and similar elements are in some cases provided with identical reference symbols and the features of the various exemplary embodiments can be combined with one another.

Brief description of the figures

In the figures:

Fig. 1 shows a diagrammatic cross section through an excerpt from an embodiment of the component according to the invention at wafer level,

Fig. 2 shows a diagrammatic cross section through the component from Fig. 1 after dicing and wire bonding,

Fig. 3 shows a diagrammatic cross section through an excerpt from an embodiment of the component according to the invention with a solder ball,

Fig. 4 shows a diagrammatic cross section through an excerpt from a further embodiment of the component according to the invention at wafer level,

Fig. 5 shows a diagrammatic cross section through an excerpt of a further embodiment of the component according to the invention with a contact element provided with a metal layer, and

Fig. 6 shows a diagrammatic plan view of an embodiment of the component according to the invention at wafer level.

Detailed description of the invention

Fig. 1 shows a base substrate 100 after processing, i.e. provided with functional regions 110, in this example integrated circuits 110. In this example, the base substrate is represented by a silicon semiconductor wafer 100.

Furthermore, in the case of CMOS applications or SOI circuits, the semiconductor wafer 100 has a dielectric interlayer 120, e.g. in the form of a silicon oxide layer. The interlayer 120 insulates the circuits 110 from the silicon wafer 100.

Furthermore, on its functional side 101, the semiconductor wafer 100 has contact surfaces or contact pads 130, the functional side 101 being defined by the fact that the circuits 110 are arranged thereon. The contact pads 130 are electrically connected (not shown) to the circuits 110. That side of the semiconductor wafer 100 which is the opposite side from the functional side is referred to as the back surface 102.

Then, a covering substrate or a covering wafer 200, in this example a Borofloat-33 glass wafer 200, is adhesively bonded onto the semiconductor wafer 100. It is particularly advantageous to use Borofloat-33 glass, since the coefficient of thermal expansion is matched to that of the semiconductor wafer 100.

The two wafers 100 and 200 are joined by means of a layer of adhesive 210, e.g. an epoxy or acrylate adhesive. This results in the quasi-hermetic packaging of the circuits 110.

As an alternative to the layer of adhesive 210, it is also possible to apply a layer of glass, in particular by evaporation coating, so that the base substrate is suitable for anodic or what is known as direct bonding. In this case, therefore, the two wafers are anodically or directly bonded.

After the joining operation, in a first step the semiconductor wafer 100 is thinned uniformly over the entire wafer, for example by mechanical grinding down to a thickness d_1. This is possible since the covering wafer 200 imparts the required stability to the assembly.

In a second step following the uniform thinning or grinding of the semiconductor wafer 100, the semiconductor wafer 100 is patterned in such a manner that, on the one hand, contact-connection recesses or contact-connection passages 301 are produced over the contact pads 130 and, on the other hand, connection regions 300 which laterally adjoin the contact-connection passages 301 are produced. This can be carried out in a single step or in two separate steps. It is preferable for this patterning to be carried out by means of a lithographic wet-etching process or a plasma etching process.

The contact-connection passages 301 will extend from the back surface 102 transversely through the semiconductor wafer 100 as far as directly to the contact pads 130.

The wafer is therefore divided into a multiplicity of body regions 104 and connection regions 300, the connection regions 300 being thinned to a greater extent than the body regions 104. In other words, the wafer material 100 is thinned to a thickness d_2 in the connection regions 300, d_2 being less than d_1. In this example, d_2 is not equal to zero.

In other words, after the uniform thinning of the semiconductor wafer 100, the wafer material is removed further in the region of the contact-connection passages 301, until the thickness d_2 has been reached.

Furthermore, the semiconductor wafer 100 also has a sawing street or a sawing trench 302 which extends laterally into the plane of the drawing and along which the wafer assembly 100, 200 is subsequently diced.

After the contact-connection passages 301 have been produced or etched and the connection regions 300 have been thinned, the back surface of the semiconductor wafer 100 is coated with a passivation layer 400, inter alia in order to protect the sensitive interfaces, e.g. between the semiconductor wafer 100 and the dielectric interlayer 120. The passivation layer 400 is, for example, a layer of evaporation-coating glass. The passivation layer 400 may also be in multilayer form (not shown in Fig. 1). Furthermore, the passivation layer 400, in particular if an evaporation-coating glass is used, also increases the hermetic sealing of the assembly.

The contact-connection passages 301 and the sawing streets or sawing tracks 302 have inclined side walls 303 and 304 in order to ensure a continuous passivation layer 400.

At the same time or in a separate step, the dielectric interlayer 120 which is present in this example and the passivation layer 400 are removed in patterned form over the contact pads 130 in order to uncover the latter for contact-connection from the back surface 102.

Then, a contact redistribution element, more specifically a contact redistribution layer 410 in the form of a metallization, e.g. electro-plated Cu based on Ti/W/Cu plating, is applied on the back surface, extending at least from the contact surface 130 to a secondary contact surface 132 in the connection region 300. Accordingly, the contact

redistribution layer 410 extends as far as into the connection region 300, where it forms the secondary contact surface 132. In other words, the contact redistribution layer 410 provides the secondary contact surface 132 in the connection region 300, and this secondary contact surface 132 is arranged laterally offset with respect to the contact pads 130 on the back surface of the semiconductor wafer 100. In this way, the secondary contact surface 132 is advantageously thermo-mechanically decoupled from the functional region 110.

The secondary contact surface 132 is also coated on the back surface with a bonding layer 410, an oxidation-resistant layer and/or a diffusion barrier.

Then, the wafer assembly 100, 200 is sawn, i.e. diced into chips 10, along the sawing streets 302 or along a centre line 600.

Fig. 2 illustrates a diced chip 10 with a functional region 110 which has been packaged in a hermetically sealed manner. After dicing, the chips 10 are processed further by means of wire bonding, for example to a circuit carrier (not shown).

Referring now to Fig. 3, a chip 10 is provided with a solder ball 501, which embodies an alternative contact-connection means to the circuit carrier. The solder balls 501 can be applied before or after dicing.

Fig. 4 shows the component at wafer level; in this embodiment, the semiconductor wafer 100, in the connection region 300, has been thinned all the way to the silicon oxide layer 120, i.e. down to a thickness of virtually zero. Therefore, the semiconductor material of the wafer

100 has been completely removed in the connection region 300. Therefore, the passivation layer 400, in the connection region 300, is applied direct to the silicon oxide layer 120.

In this example, therefore, the contact-connection passages 301, the connection regions 300 and the sawing streets 302 fuse together to a certain extent to form a common recess in the back surface of the semiconductor wafer 100.

The wire bondings 500 which are to be applied after dicing are indicated by dotted lines.

Furthermore, a second passivation layer 402, in particular made from the same material as the first passivation layer 400, has been applied to the first passivation layer 400. The second passivation layer 402 extends at least over that portion 412 of the contact redistribution layer 410 which is connected to the contact surfaces 130, and in this example extends over the sawing streets 302 in order also to passivate the latter. In other words, a continuous second passivation layer 402 is applied but remains clear or is uncovered over the secondary contact surfaces. A recess in the covering substrate 200 defines a cavity 201.

Fig. 5 shows a wafer assembly in which the thickness d_2 of the base substrate 100 is greater in the connection region than in the body region 104. For this purpose, the semiconductor wafer 100 is first of all ground down uniformly to a thickness d_2 and is then thinned further in patterned form in the body region 104, so that the thickness of the semiconductor wafer 100 is greater in the connection region 300 than in the body region 104.

With regard to the further process steps, reference is made to Fig. 1.

A bonding layer or gold layer 420 is applied to the connection region 300, which represents the thickest part of the wafer assembly, and then a solder contact 502 is applied to the bonding layer or gold layer 420. The solder contact 502 is, if appropriate, likewise coated by electroplating.

Fig. 6 shows the wafer assembly 100, 200 together with the contact-connection passages 301. Various forms of connection sections 300a, 300b, 300c are also illustrated.

The connection regions 300a form a common connection strip 304a which extends longitudinally along the sawing trench 302a over the entire chip 10. Furthermore, the connection strip 304a extends transversely with respect to its longitudinal axis, from the centre line 600 of the sawing trench to over the contact-connection passages 301, which are only partially covered.

The connection regions 300b are likewise combined to form a connection strip 304b which, however, extends, transversely with respect to its longitudinal axis, completely over the contact-connection passages 301.

Alternatively, a third variant of connection regions 300c is also provided, these connection regions in each case extending separately from one another around the contact-connection passages 301, with each contact-connection passage 301 being assigned a dedicated connection region 300c. In any case, a thinned region is provided around the contact-connection passages 301.

It will be clear to the person skilled in the art that the embodiments described above are to be understood as examples and that the invention is not restricted to these particular examples, but rather can be varied in numerous ways without departing from the scope of the invention.

Patent claims:

1. Process for packaging components,

in which a base substrate, on its functional side, has a multiplicity of functional regions spaced apart from one another and is permanently connected, by means of the functional side, to a covering substrate at wafer level, in such a manner that the functional regions are in each case packaged,

in which contact surfaces on the base substrate are uncovered from a back surface of the base substrate, which back surface is on the opposite side from the functional side, by the production of contact-connection recesses in the base substrate,

in which the base substrate is divided into body regions and connection regions, the body regions in each case extending over the functional regions and forming part of the packages for the functional regions, and the connection regions being offset with respect to the contact-connection recesses,

the component being thinned in the body regions or the connection regions until it has different thicknesses in the body regions and the connection regions, and

in which the wafer assembly formed at least from base substrate and covering substrate is diced into chips along predefined cutting lines between the functional regions.

2. Process according to Claim 1,

in which the chips are arranged on a circuit carrier and the contact surfaces or contact redistribution elements are connected to contact elements of the circuit carrier by means of wire bonding on the back surface of the base substrate.

3. Process according to Claim 2, characterized in that the wire bonding comprises welding of connection wires to the contact surfaces or the contact redistribution elements.

4. Process according to one of the preceding claims, characterized in that contact redistribution elements, which extend at least from the contact surfaces to the connection regions and can be contact-connected on the back surface in the connection regions, are applied to the back surface of the contact surfaces.

5. Process according to one of the preceding claims, characterized in that the covering substrate is thinned after the base substrate has been joined to the covering substrate.

6. Process according to one of the preceding claims, characterized in that the contact surfaces are uncovered by means of patterned etching of the base substrate from the back surface.

7. Process according to one of the preceding claims, characterized in that a passivation layer is applied in patterned form to the back surface of the base substrate, with the contact surfaces remaining substantially uncovered, or a passivation layer is applied to the back surface of the base substrate and is then patterned in such a manner that the contact surfaces are uncovered.

8. Process according to one of the preceding claims, characterized in that, after the contact surfaces have been uncovered, they are covered with a metal layer on the back surface by electroplating or electroless means.

9. Process according to one of the preceding claims, characterized in that the base substrate used is a semiconductor substrate with functional regions which comprise integrated circuits.

10. Process according to one of the preceding claims, characterized in that the base substrate used is a semiconductor substrate having optical, micro-mechanical or electronic functional elements or a combination thereof.

11. Process according to one of the preceding claims, characterized in that the base substrate is etched on the back surface along the predefined cutting lines in order to define sawing streets.

12. Process according to one of the preceding claims, characterized in that the connection regions directly adjoin the contact-connection recesses in the lateral direction.

13. Process according to one of the preceding claims, characterized in that the contact-connection recesses, the connection regions and the sawing streets are produced in a single step.

14. Process according to one of the preceding claims, characterized in that the thinning of the base substrate in the connection regions is carried out before the contact surfaces have been joined to the contact elements of the circuit carrier by means of wire bonding.

15. Process according to one of the preceding claims, characterized in that the base substrate is thinned uniformly in a first step and is thinned still further in

the connection regions or the body regions in a second step which follows the first step.

16. Process according to one of the preceding claims, characterized in that, in the second step, the base substrate is etched in patterned form in the connection regions or the body regions.

17. Process according to one of the preceding claims, characterized in that connection strips which run parallel to the predefined cutting lines are produced, the base substrate being thinned to a greater extent in the connection strips than in the body regions, and a plurality of contact-connection recesses adjoining the same connection strip.

18. Process according to one of the preceding claims, characterized in that connection regions which extend at least from the contact-connection recesses to the predefined cutting lines are produced.

19. Process according to one of the preceding claims, characterized in that, before the base substrate is joined to the covering substrate, a bonding layer is applied to the base substrate or the covering substrate.

20. Process according to one of the preceding claims, characterized in that, before the base substrate is joined to the covering substrate, the covering substrate is provided with recesses over the functional regions, so that after the base substrate has been joined to the covering substrate, cavities, in which the functional regions are enclosed, are formed between the two substrates.

21. Process for packaging components, in particular according to one of the preceding claims,

in which a base substrate, on its functional side, has a multiplicity of functional regions spaced apart from one another and is permanently joined, by means of the functional side, to a covering substrate at wafer level, in such a manner that the functional regions are each packaged,

in which contact surfaces on the base substrate are uncovered from a back surface of the base substrate, which back surface is on the opposite side from the functional side, by the production of contact-connection recesses in the base substrate,

in which the wafer assembly formed at least from base substrate and covering substrate is diced into packaged chips along predefined cutting lines between the functional regions, and

in which the chips are arranged on a circuit carrier and the contact surfaces are connected to contact elements of the circuit carrier by means of wire bonding on the back surface of the base substrate.

22. Packaged component, producible in particular by a process according to one of the preceding claims, comprising:

a base substrate having a functional side, on which a functional region of the component is arranged, and a back surface on the opposite side from the functional side,

a covering substrate, which is permanently joined to the base substrate on the functional side of the latter, the covering substrate extending over the functional region, and the join surrounding the functional region in such a manner that a housing is formed around the functional region, and

contact surfaces which are connected to the functional region,

the base substrate, in the region of the contact surfaces, comprising contact-connection recesses, through which the contact surfaces are or can be contact-connected from outside the housing and from the back surface of the base substrate,

the base substrate having a body region and connection regions, the body region extending over the functional region and forming part of the housing, the connection regions and the contact-connection recesses being offset, and

in which the component has different thicknesses in the body region and the connection regions.

23. Component according to Claim 22, characterized in that the base substrate is a semiconductor substrate and the functional region comprises integrated circuits.

24. Component according to one of the preceding claims, characterized in that the functional region comprises optical, micro-mechanical or electronic components or a combination thereof.

25. Component according to one of the preceding claims, characterized in that the component has narrow sides at which it is separated out of the wafer assembly, and the connection regions extend at least from the contact-connection recesses to the narrow sides.

26. Component according to one of the preceding claims, characterized in that a plurality of connection regions are combined to form a connection strip, and a plurality of

contact-connection recesses adjoin the same connection strip.

27. Component according to one of the preceding claims, characterized in that the contact surfaces are connected to contact redistribution elements which extend at least from the contact surfaces to the connection regions and can be contact-connected in the connection regions.

28. Component according to one of the preceding claims, characterized in that the base substrate and the covering substrate are joined by means of a bonding layer, in particular a layer of adhesive or a layer of evaporation-coating glass.

29. Component according to one of the preceding claims, characterized in that the covering substrate has a recess over the functional region, so that a cavity, within which the functional region is enclosed, is formed.

30. Component according to one of the preceding claims, characterized in that at least one passivation layer is applied to the back surface of the base substrate.

31. Component according to one of the preceding claims, characterized in that the contact surfaces are provided with a metallic covering applied by electroplating or electroless means.

32. Component according to one of the preceding claims, characterized in that connection wires are electrically conductively connected to the contact surfaces or the contact redistribution elements, the connection wires being connected to the contact surfaces by means of wire bonding.

33. Component according to one of the preceding claims, characterized in that the connection wires are welded to the contact surfaces or the contact redistribution elements without the use of solder.

34. Composite element comprising a multiplicity of components according to one of the preceding claims at wafer level.

35. Circuit arrangement having a circuit carrier and a component according to one of the preceding claims incorporated therein.