AN INTEGRATED CIRCUIT INCLUDING A STRESSED DIELECTRIC LAYER WITH STABLE STRESS

FIELD OF THE INVENTION

[0001] The present invention relates generally to integrated circuits (ICs), and more particularly to forming stressed dielectric layers in ICs.

BACKGROUND OF THE INVENTION

[0002] Integrated circuits (ICs) typically comprise numerous circuit components interconnected to perform the desired functions. Such circuit components include, for example, transistors such as field effect transistors (FETs). Dielectric materials have been employed to generate strain in the channel region of the transistor to enhance carrier mobility. For example, tensile stress may be applied to the channel region of n-type FETs to enhance carrier mobility. In the case of p-type FETs, compressive stress may be applied to the channel region.

[0003] It is desirable to provide enhanced strain generation in channel regions of transistors to enhance carrier mobility.

SUMMARY OF THE INVENTION

[0004] The present invention relates to forming stressed dielectric layers in ICs. In one aspect of the invention, an IC comprises a substrate having active and isolation regions. A transistor having a channel region is disposed on the substrate in the active region. In one embodiment, the isolation region comprises O_3 TEOS oxide having a stress retaining dopant, wherein the O_3 TEOS oxide induces a first stress in the channel region of the transistor. In another embodiment, the IC further comprises a dielectric layer disposed on the substrate and the transistor. At least one of the isolation region or the dielectric layer comprises O_3 TEOS having a stress retaining dopant, the O_3 TEOS oxide inducing a first stress in the channel region of the transistor.

[0005] In another aspect of the invention, a method of fabricating an IC comprises providing a substrate having an active region and an opening in the substrate adjacent to the active region.

In one embodiment, the opening is filled with O_3 TEOS oxide having a stress retaining dopant to form an isolation region in the substrate, and a transistor is formed on the substrate in the active region. In another embodiment, the opening is filled with a first dielectric material to form an isolation region in the substrate. A transistor is formed on the substrate in the active region. A pre-metal dielectric (PMD) layer is formed on the substrate and the transistor, wherein the PMD layer comprises a second dielectric material. At least one of the first or second dielectric materials comprises O_3 TEOS oxide having a stress retaining dopant.

[0006] These and other objects, along with advantages and feature of the present invention herein disclosed, will become apparent through reference to the following description and the accompanying drawings. Furthermore, it is to be understood that the features of the various embodiments described herein are not mutually exclusive and can exist in various combinations and permutations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

[0008] Fig. 1 shows a cross-section of portion of an IC in accordance with one embodiment of the invention;

[0009] Figs. 2a-f show a process for forming an IC in accordance with one embodiment of the invention; and

[0010] Fig. 3 shows the chemical reactions that occur during a chemical vapor deposition (CVD) process to form a N doped O_3-TEOS oxide film, in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0011] The present invention relates to ICs. More particularly, the present invention relates to stressed dielectric layers for strain generation in, for example, channel region of a transistor. The invention can be applied to various types of ICs, such as memory devices including dynamic random access memories (DRAMs), static random access memories (SRAMs), non-volatile memories including programmable read-only memories (PROM) and flash memories, optoelectronic devices, logic devices, communication devices, digital signal processors (DSPs), microcontrollers, system-on-chip, as well as other types of devices.

[0012] Fig. 1 shows a cross-sectional view of a portion of an IC 100 in accordance with one embodiment of the invention. The IC comprises a substrate 105. The substrate comprises a semiconductor material, such as silicon. Other types of semiconductor substrates are also useful. Defined on the substrate is an active region 108. The active region includes a doped well 111 of a first charge carrier type. In one embodiment, the first charge carrier type comprises p-type. For example, the doped well comprises p-type dopants such as boron (B), aluminum (Al) or a combination thereof.

[0013] A transistor 140 is disposed in the active region. The transistor, for example, comprises a FET. The FET comprises a second charge carrier type. In one embodiment, the second charge carrier type comprises n-type. The transistor includes a gate stack 145. The gate stack can be gate conductor which forms a plurality of transistors having a common gate. The gate stack comprises a gate electrode over a gate dielectric. The gate electrode, for example, comprises polysilicon while the gate dielectric comprises silicon oxide. Other types of gate electrode and gate dielectric materials are also useful. Dielectric spacers 154 are typically provided on sidewalls of the gate stack. First and second diffusion regions 147a-b are provided adjacent to the gate stack. The diffusion regions comprise second type or n-type dopants, such

as phosphorous (P), arsenic (As), antimony (Sb) or a combination thereof. Silicide contacts 158 can be provided on the top of the gate and diffusion regions to reduce sheet resistance.

[0014] Isolation regions 130 are provided to isolate the active region from other device regions. In one embodiment, the isolation regions comprise shallow trench isolations (STIs). STIs comprise trenches formed in the substrate and filled with a dielectric material. The depth of the STIs is generally about 1500 – 4500 Å. Other depths are also useful. The doped well typically overlaps the bottom of the STIs. A pre-metal dielectric (PMD) layer 190 is provided over the transistor. The PMD layer comprises a dielectric material. Optionally, a stress liner layer (not shown) can be provided over the transistor below the PMD layer. The stress liner applies a tensile stress on the channel region of the n-type transistor.

[0015] In accordance with one embodiment of the invention, the dielectric material of the STI and/or PMD induces a first stress. For example, either the STI trenches, PMD layer, or both, comprise a material which induces the first stress. In one embodiment, the first stress comprises tensile stress. The dielectric material, in a preferred embodiment, comprises an ozone-tetraethoxysilane (O_3-TEOS) oxide with a stress retaining dopant. The stress retaining dopant, in one embodiment, comprises nitrogen (N). Other types of dopants are also useful. Doping the O_3-TEOS oxide with N enhances its resistance to moisture absorption. This is because the N dopants react with Si in the O_3-TEOS oxide to form stable Si-N bonds, thereby preventing the Si from reacting with atmospheric moisture (to form the less stable Si-OH bonds). As moisture can lead to stress degradation in the O_3-TEOS oxide, providing N dopants enhances the ability of the O_3-TEOS oxide to retain its stress.

[0016] The dopant concentration of N should be sufficient to retard stress degradation of the silicon oxide film. In one embodiment, the N concentration in the O_3-TEOS oxide is about 1E6 – 1E15 c/s (using Secondary Ion Mass Spectrometry (SIMS) measurement). Other

concentrations are also useful. In general, the higher the N concentration in the O_3-TEOS, the higher its resistance to moisture absorption, thus forms more stable stress.

[0017] In one embodiment, the N doped O_3-TEOS oxide comprises an in-situ N doped O_3-TEOS oxide. For example, precursors for forming the dielectric material include O_3, TEOS and a N source. The N source, in one embodiment, can be selected from NH_3, N_2O or a combination thereof. Other types of N sources are also useful.

[0018] Figs. 2a-f show a process for forming an IC 200 in accordance with one embodiment of the invention. Referring to Fig. 2a, a substrate 205 is provided. The substrate, in one embodiment, comprises a p-type silicon substrate. Other types of substrates, such as a germanium-based, gallium arsenide, silicon-on-insulator (SOI), or sapphire substrate, are also useful.

[0019] A mask 280 is formed on the surface of the substrate. The mask is patterned to form openings corresponding to locations where STI trenches are to be formed. The mask, for example, comprises a soft mask such as photoresist. The photoresist can be patterned by conventional lithographic techniques. An antireflective coating (ARC) is typically provided beneath the photoresist.

[0020] Preferably, the mask comprises a hard mask and a soft mask. The hard mask can include a pad oxide layer under a silicon nitride layer. Other types of hard masks are also useful. An ARC can be disposed between the hard mask and soft mask. The soft mask is patterned using conventional lithographical techniques to form openings. The soft mask is then used to pattern the hard mask using, for example, an anisotropic etch such as reactive ion etch (RIE). The soft mask can be removed after patterning the hard mask.

[0021] Referring to Fig. 2b, the substrate is etched to form trenches 275 in regions unprotected by the mask. The trenches are etched using, for example, RIE. Other processes for

forming the trenches are also useful. Typically, the depth of the trenches is about 1500 – 4500 Å. Other depths are also useful and may depend on design requirements.

[0022] Referring to Fig. 2c, a dielectric layer 285 is deposited on the substrate to fill the trenches. The dielectric layer is sufficiently thick to ensure complete filling of the trenches. A dielectric liner layer can be formed to line the substrate and trenches prior to depositing the dielectric layer. The liner layer removes residual damage created during the etch process and provides corner rounding.

[0023] The dielectric layer, in one embodiment, comprises a dielectric material which applies a first stress. The dielectric material, in one embodiment, applies a tensile stress. Preferably, the dielectric material comprises O_3-TEOS doped with a stress retaining dopant. Other types of dielectric materials are also useful. The stress retaining dopant, in one embodiment, comprises N. The concentration of N should be sufficient to retard stress degradation of the silicon oxide film. The N concentration in the O_3-TEOS oxide is, for example, about 1E6 – 1E15 c/s (using SIMS measurement). Other N concentrations are also useful. In general, the higher the N concentration in the O_3-TEOS, the higher its resistance to moisture absorption, thus forms more stable stress.

[0024] Chemical vapor deposition (CVD) process is used to form the O_3-TEOS oxide. In one embodiment, the O_3-TEOS oxide is formed by sub-atmospheric CVD (SACVD) process. The O_3-TEOS oxide, in one embodiment, is in-situ doped with N. To form the N doped O_3-TEOS oxide, gaseous precursors including O_3, TEOS, TEOS carrier gas, and a nitrogen source are provided in the deposition chamber. The nitrogen source, in one embodiment, comprises NH_3, N_2O, or both. Other nitrogen-containing species such as N_2, NO_2, NCl_3, NF_3, I_3N and N_2O_3 are also useful. The carrier gas can comprise, for example, He, N_2, Ar, or any other useful inert gas.

[0025] In one embodiment, the N doped O_3-TEOS oxide is deposited at a temperature of about 350 - 600°C. Preferably, the deposition temperature is about 400 - 550°C. The deposition pressure is about 50 - 600 Torr, and preferably about 100 - 500 Torr. The TEOS flow rate is about 1000sccm - 30000 sccm. Preferably, the TEOS flow rate is about 3000 – 25000 sccm. The TEOS carrier gas flow rate is about 1000 - 50000 sccm and preferably about 3000 - 30000 sccm. The O_3 flow rate is about 5000 - 40000 sccm. Preferably, the O_3 flow rate is about 10000 - 35000 sccm. In one embodiment, the concentration of O_3 is about 5 - 20% and preferably about 10 -15%. As for nitrogen source, the flow rate is about 200 – 5000 sccm and preferably about 500 - 3000 sccm.

[0026] Referring to Fig. 2d, excess dielectric material is removed. In one embodiment, the excess dielectric material is removed by, for example, chemical mechanical polishing (CMP). Other processes for removing excess dielectric materials are also useful. The CMP removes the excess dielectric material and form a planar substrate surface, forming STIs 230. Typically, a polish stop layer is provided on the substrate surface. The polish stop layer, for example, comprises silicon nitride or a material which the dielectric layer can be polished selective thereto. The polish stop layer can be the hard mask layer used to form the trenches.

[0027] A doped well 211 is formed after the STIs are formed. The doped well comprises first type dopants. In one embodiment, the first type dopants comprise p-type dopants which forms a p-type doped well. The p-type dopants can include, for example, B. Typically, the dopant concentration of the doped well is about 1E10 – 1E14 /cm^2. Conventional ion implantation techniques, such as implantation with a mask can be used to form the doped well. Other techniques are also useful. Optionally, the doped well can be formed prior to forming the STIs.

[0028] Referring to Fig. 2e, the process continues to form a transistor 240 in the active region 208 defined by the STIs. To form the transistor, gate stack layers are formed on the

substrate. The gate stack layers generally comprise a polysilicon gate electrode layer over a thermal oxide gate dielectric layer. Other types of gate stack layers are also useful. The gate layers are patterned using conventional mask and etch techniques to form a gate stack 245. The gate stack can be a gate conductor which is a common gate for a plurality of transistors.

[0029] Source/drain diffusion regions 247a-b are then formed in the active region of the substrate adjacent to the gate. In one embodiment, the source/drain diffusion region comprises dopants of second carrier type. For example, the source/drain diffusion region comprises n-type dopants to form n-type transistor. The n-type diffusion regions are formed by implanting n-type dopants, such as P, As, Sb or a combination thereof.

[0030] Dielectric spacers 254 are formed on the sidewalls of the gate stack. The dielectric spacers, for example, comprise silicon nitride. Other types of dielectric materials are also useful to form the spacers. To form the spacers, a spacer layer is deposited on the substrate which covers the gate and substrate surface. An etch removes the horizontal components of the spacer layer, leaving spacers on the sidewalls of the gate stack.

[0031] The diffusion regions can include shallow source/drain extensions (not shown) and deep source/drain portions. The source/drain extensions can be formed before the formation of sidewall spacers while the deep source/drain portions are formed after the spacers are formed. Metal silicide contacts 258 can be formed on the gate and diffusion regions. The metal silicide contacts, for example, comprise nickel silicide contacts. Other types of metal silicide contacts are also useful. To form the metal silicide contacts, a metal layer is formed on the substrate and annealed to cause a reaction with the silicon substrate. Unreacted metal are removed, leaving the silicide contacts.

[0032] In Fig. 2f, a PMD layer 290 is formed on the substrate. In one embodiment, prior to forming the PMD layer, a dielectric stress inducing liner layer (not shown) can be formed on the substrate. The liner conformally lines the substrate and transistor and applies a first stress on the

channel region of the transistor beneath the gate. The first stress, for example, comprises a tensile stress for a n-type transistor. The stress liner, in one embodiment, comprises silicon nitride.

[0033] The PMD layer covers the substrate and transistor. The PMD layer can be planarized by, for example, CMP. Other methods for planarizing the PMD layer are also useful. In one embodiment, the PMD layer applies the first stress. Preferably, the dielectric material comprises O_3-TEOS doped with a stress retaining dopant, as previously described. Other types of dielectric materials are also useful. The stress retaining dopant, in one embodiment, comprises N.

[0034] The process continues by forming interconnections to the contacts of the transistors. For example, the PMD layer is patterned to create contact holes. The contact holes are then filled with conductive material, such as tungsten, to form interconnects. Additional processes are performed to complete the IC, for example, additional interconnect levels, final passivation, dicing, and packaging.

[0035] Providing a high tensile PMD layer increases electron mobility, leading to improved nFET performance. Alternatively, a compressive layer can be used to enhance hole mobility and pFET performance. As described, introducing dopants into the high tensile silicon oxide film, according to one embodiment of the invention, retards moisture absorption of the film to prevent degradation of its tensile stress characteristics.

[0036] The process continues to complete fabricating the IC. For example, the process continues to form interconnects, additional interconnect levels, passivation layer, dicing, assembly and packaging.

[0037] Fig. 3 shows the chemical reactions that occur during the CVD process to form the N-doped high tensile O_3-TEOS oxide film. First, O_3 and TEOS react to form silanol ($Si(OH)_4$). Some of the hydroxyl (OH) groups in the silanol are replaced by nitrogen (N) derived from the nitrogen source, forming N doped silanol. Thereafter, N doped O_3-TEOS oxide is formed from

condensation between N doped silanol molecules. By replacing OH groups with N atoms, there are less number of OH groups. This reduces the potential for OH groups to bond with O atoms from O_3 to form H_2O (or water) molecules. As a result, the N doped O_3-TEOS has improved resistance against moisture absorption, which can degrade the stress retention of the layer.

[0038] As described, the doped O_3-TEOS oxide applies a tensile stress to the channel of n-type transistors to enhance carrier mobility of electrons. The doped O_3-TEOS oxide can be used to form STIs and/or PMD. We have also found that the tensile doped O_3-TEOS oxide can be used on p-type transistors without adversely affecting their performance. The p-type transistors may be narrow-width or wide-width p-type transistors. Therefore, the doped O_3-TEOS oxide can advantageously be used for both n-type and p-type transistors.

[0039] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments, therefore, are to be considered in all respects illustrative rather than limiting the invention described herein. Scope of the invention is thus indicated by the appended claims, rather than by the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

CLAIMS

1. An integrated circuit (IC) comprising:

a substrate having active and isolation regions; and

a transistor disposed on the substrate in the active region, the transistor having a channel region,

wherein the isolation region comprises O_3 TEOS oxide having a stress retaining dopant, the O_3 TEOS oxide induces a first stress in the channel region of the transistor.

2. The IC of claim 1 wherein the stress retaining dopant comprises nitrogen.

3. The IC of claim 2 wherein the nitrogen comprises a concentration of about 1E6-1E15 c/s.

4. The IC of claim 1 wherein the transistor comprises n-type transistor and the first stress is tensile stress.

5. The IC of claim 1 wherein the transistor comprises p-type transistor and the first stress is tensile stress.

6. An integrated circuit (IC) comprising:

a substrate having active and isolation regions;

a transistor disposed on the substrate in the active region, the transistor having a channel region; and

a dielectric layer disposed on the substrate and the transistor,

wherein at least one of the isolation region or the dielectric layer comprises O_3 TEOS oxide having a stress retaining dopant, the O_3 TEOS oxide induces a first stress in the channel region of the transistor.

7. The IC of claim 6 wherein the dielectric layer comprises a pre-metal dielectric (PMD) layer.

8. The IC of claim 7 wherein the stress retaining dopant comprises nitrogen.

9. The IC of claim 8 wherein the nitrogen comprises a concentration of about 1E6-1E15 c/s.

10. The IC of claim 6 wherein the transistor comprises n-type transistor and the first stress is tensile stress.

11. The IC of claim 6 wherein the isolation region comprises shallow trench isolation region.