IMPROVED BUFFER FOR SEMICONDUCTOR STRUCTURES

Field of the Invention

The invention relates to an improved buffer for a semiconductor structure and method of fabricating the buffer. More particularly the invention relates to an improved InAs buffer for releasing lattice strain between a GaAs substrate and a high indium content epilayer for a semiconductor structure, such as structures used in high speed devices and long wavelength devices, eg. field effect transistors (FET's), high election mobility transistors (HEMT's), hall elements, long wavelength detector and laser, etc.

Background of the Invention

In this specification, where a document, act or item of knowledge is referred to or discussed, this reference or discussion is not an admission that the document, act or item or knowledge or any combination thereof was at the priority date:

(i) part of common general knowledge; or

(ii) known to be relevant to an attempt to solve any problem with which this specification is concerned.

Whilst the following discussion relates mainly to FET's or HEMT's, it is to be understood that the invention is not so limited but may extend to other semiconductor and transistor structures.

Microprocessors are essential to many of the products we use every day such as televisions, cars, radios, home appliances and computers. Transistors are the basic elements in microprocessors.

Transistors are miniature electronic switches. Transistors have no moving parts and are turned on and off by electrical signals. The on/off switching of transistors facilitates the work performed by microprocessors. A transistor regulates current or voltage flow and acts as a switch or gate for electronic signals.

Transistors are formed by semiconductor materials, the conductivity of which semiconductor materials can be given special properties by a chemical process called *doping*. A semiconductor is doped by adding certain types of impurities to change the crystalline structure of the semiconductor and enhance its ability to conduct electricity. Doping either adds extra electrons to the material (which is then called *N-type* for the extra negative charge carriers) or creates "holes" in the material's crystal structure

(which is then called *P-type* because it results in more positive charge carriers). Transistors typically have a three-layer structure containing an N-type semiconductor layer sandwiched between P-type layers (a PNP configuration) or a P-type layer between N-type layers (an NPN configuration).

As the current or voltage is changed in one of the outer semiconductor layers, it effects a larger current or voltage in the inner layer resulting in the opening or closing of an electronic gate. Today's computers use circuitry made with complementary metal oxide semiconductor (CMOS) technology. CMOS uses two complementary transistors per gate (one with N-type material; the other with P-type material). When one transistor is maintaining a logic state, it requires almost no power.

Field-effect transistor (FET)

A field-effect transistor is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless signals). The structure can amplify analog or digital signals. It can also switch DC or function as an oscillator.

In the FET, current flows along a semiconductor path called the *channel*. At one end of the channel, there is an electrode called the *source*. At the other end of the channel, there is an electrode called the *drain*. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the *gate*. The conductivity of the FET depends, at any given instant in time, on the electrical diameter of the channel. A small change in gate voltage can cause a large variation in the current from the source to the drain. This is how the FET amplifies signals.

Field-effect transistors exist in two major classifications. These are known as the *junction FET (JFET)* and the *metal-oxide- semiconductor FET (MOSFET)*, which are characterized by whether the active region is n type (current carried by electrons) or p type (carried by holes). In so-called complementary logic circuits, pairs of n- and p-type FETs work side by side, an arrangement whose advantages include low power consumption, robustness and simple circuit designs.

The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material. The gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called *holes*. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate.

Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate.

In the MOSFET, the channel can be either N-type or P-type semiconductor. The gate electrode is a piece of metal whose surface is oxidized. The oxide layer electrically insulates the gate from the channel. Because the oxide layer acts as a dielectric, there is essentially never any current between the gate and the channel during any part of the signal cycle. This gives the MOSFET an extremely large input impedance.

Field-effect transistors are preferred for weak-signal work, for example in wireless communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-effect transistors are able to be fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes.

High Electron Mobility Transistory (HEMT)

High Electron Mobility Transistors are semiconductor devices in which the channel is the two-dimensional electron gas in a quantum well.

Manufacture of FET's & HEMT's

FET devices are constructed on a substrate of doped semiconductor material. Most FETS are constructed with silicon. In order to achieve a higher gain-bandwidth product, other materials have been used. Gallium arsenide (GaAs) has electron mobility and drift velocities that are far higher than the standard doped silicon. Amplifiers designed with GaAs FET devices have much higher frequency response and lower noise factor at VHF and UHF than those made with standard FET's.

The inclusion of other elements such as indium (In) has further improved the characteristics of HEMT's. Many HEMT's and FET's consist of high indium composition InGaAs/InAlAs structures on InP substrates. Those having structures lattice-matched to the InP substrate exhibit higher mobility and higher saturation velocity and high quality $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ epilayers can be grown on the InP substrate without

lattice-mismatch. Hence an InGaAs channel layer having In content as high as about 53% can be obtained based on the InP substrate.

High indium (In) content InGaAs/InAlAs structures on InP substrates exhibit excellent gain and linearity, very high f_T, and very low noise. By increasing the indium content in the $In_xGa_{1-x}As$ channel layer, a smaller channel electron effective mass and larger conduction band discontinuity ΔE_c can be obtained, which improves the performance of these semiconductor devices. However, InP substrates have many disadvantages compared with GaAs substrates, such as higher cost, smaller size and greater fragility. Therefore, in the last few years, there has been considerable interest in the development of InGaAs/InAlAs metamorphic HEMT's and FET's based on GaAs substrates.

A major problem associated with growing high indium composition semiconductors on GaAs substrates lies in the large lattice mismatch between the GaAs substrate and high indium content epilayers. Lattice-mismatch in semiconductor materials causes dislocation which degrades the performance of the devices.

Efforts have been made to reduce the strain between the GaAs substrate and high indium content epilayers by introducing a buffer. An effective buffer should carry out two functions:

(1) accommodation of the lattice mismatch by formation of misfit dislocations; and

(2) trapping of the misfit dislocations and prevention of their propagation into the epilayer grown on the buffer.

These efforts to reduce the strain between GaAs substrate and high indium content epilayers have included the use of a linearly graded InGaAs or InAlAs buffer layer. The thickness of such a buffer layer is generally greater than 1 μm. Several publications have also reported the use of step-graded InGaAs or InAlAs buffer layers to improve the quality of the channel layer. However, the thickness of such buffer layers is generally greater than 500 nm. In such systems, the indium content is generally no more than about 53%.

US Patent 5,770,868 describes the use of a GaAs substrate with AlGaAsSb buffer layer having graded As and Sb compositions for the fabrication of high indium content FET's. While the graded buffer composition reduces strain, the disadvantages are that very accurate control of the graded composition is required during its fabrication and the buffer thickness is relatively large (i.e. greater than 1 μm).

Clearly there is a need for improved buffer layer growth technology for high electron mobility semiconductors in order to provide effective reduction or release of the strain between a GaAs substrate and the high indium content layers. This would enable use to be made of high indium content (up to almost 100%) epilayers, resulting in structures having very high electron mobility. Ideally, the buffer layer is as thin as possible in order to reduce growth time and cost.

Summary of the Invention

According to a first aspect of the invention, there is provided a semiconductor structure having high electron mobility, for use in high speed devices and long wavelength devices, said structure comprising:

- a GaAs substrate;
- an epilayer of a high indium content material; and
- an InAs buffer layer located intermediate the substrate and the epilayer,

wherein the GaAs substrate has a first lattice constant, the epilayer has a second lattice constant different from the first lattice constant, and the InAs buffer layer is adapted to release strain caused by mismatch of said different lattice constants.

Preferably, the GaAs substrate has a GaAs buffer layer formed thereon. The GaAs buffer layer typically has a thickness of between 100 and 300 nm. A thickness of about 200 nm is generally preferred.

Preferably, the high indium content epilayer is formed of material chosen from the group comprising InAs, InGaAs and InAlAs. InAs is a particularly preferred material.

Such a structure may allow for an In-contained epilayer having an indium content of greater than about 90%. Such high levels of indium are highly desirable in practical applications of the above devices.

Where the epilayer is InGaAs or InAlAs, and the indium content of the epilayer is about 90% or more, no additional buffer needs to be inserted. This is because the lattice mismatch in such cases is generally less than about 1%. However, in situations where the indium content of the epilayer is less than about 90%, the lattice mismatch between the InAs buffer layer and the epilayer is greater and additional buffer is generally required. This additional buffer layed is required to release the lattice mismatch between the top epilayer and the InAs buffer layer. The additional buffer layer should possess the same, or substantially the same (eg within about 1%), lattice

constant as that of the top epilayer. For instance, when the epilayer is InAlAs, the additional buffer layer may be formed of InAlAs or, alternatively, InGaAs (where the lattice constant of InAlAs is substantially the same as that of InGaAs).

Similarly, when the epilayer is InGaAs, the additional buffer layer may be formed of InGaAs. However, in this case, the additional buffer layer may alternatively be formed of InAlAs (where the lattice constants of the materials are substantially the same)

The additional InGaAs or InAlAs buffer layer is a graded buffer accommodating the lattice mismatch between the InAs buffer and the In-contained epilayer with In content less than 90%.

It is further preferred that, in the above semiconductor structure, the InAs buffer layer is relatively thin. For instance, the thickness of the InAs buffer layer may be less than about 100 nm. It is further preferred that the thickness of the InAs buffer layer is less than about 20 nm. In a preferred embodiment of the invention, the thickness of the InAs buffer layer is less than about 10 nm (for instance, it can be about 7nm thick).

The surface of the InAs buffer layer is relatively smooth which is one of the reasons why it is suitable for growing an epilayer on top of it. Preferably the surface of the InAs buffer layer has a root mean square roughness of less than about 1 nm. Preferably, the root mean square roughness is less than about 0.500 nm or, more preferably, less than about 0.400 nm.

In a preferred embodiment of the invention, the GaAs substrate of the semiconductor structure is formed of GaAs (100).

According to a second aspect of the invention, there is provided a method of producing a semiconductor structure according to the first aspect of this invention, said method comprising the steps of:

(a) growing an InAs buffer layer on a GaAs substrate; and

(b) growing an epilayer of a high indium content material on the InAs buffer layer.

It is preferred that, prior to step (a), a GaAs buffer layer is formed on the GaAs substrate. In this case, the InAs buffer layer is formed on the GaAs buffer layer.

The buffer layers and the epilayer are typically grown by molecular beam epitaxy (MBE).

Preferably, the GaAs buffer layer is grown at a temperature of about 600°C and an As beam equivalent pressure of between about 1.0×10^{-5} Torr and 2.0×10^{-5} Torr. Preferably, the As beam equivalent pressure is about 1.5×10^{-5} Torr. Preferably, the InAs buffer layer is grown at a temperature of about 500°C.

In the above method, it is preferred that the InAs buffer layer and the epilayer are grown at a temperature of between about 250°C and 550°C. Preferably, the temperature is about 500°C. For the growth of the InAs buffer layer and the epilayer, the As beam equivalent pressure is between about 1.0×10^{-5} Torr and 2.0×10^{-5} Torr. Preferably, the As beam equivalent pressure is about 1.5×10^{-5} Torr.

The molecular beam epitaxy can be effected by a solid source RIBER™ 32 P MBE system.

It is further preferred that the InAs buffer layer is grown at low V/III ratio, typically less than 15. It is further preferred that, when growing the epilayer, the V/III ratio is up to about 50:1.

In the above method, the InAs buffer layer is typically grown for a period of between about 80 and 100 seconds.

Optimally, the above InAs buffer layer will not only accommodate the dislocations generated by lattice mismatch and release of the strain between epilayer and substrate, but also trap the dislocation and prevent their propagation in to the epilayer grown on the buffer.

Without wishing to be bound by theory, it appears that the improved atom migration-enhancement technology of the present invention improves the InAs dots size distribution as the InAs dots are grown on the surface of the GaAs type substrate. The size distribution of these InAs dots may be less than 10%. With further growth of InAs upon these giant InAs dots, the InAs dots start to dissolve and a very smooth InAs surface is formed without any cracks, which is evidence that the strain between the GaAs type substrate and the high indium content epilayer has been released.

Throughout this specification, unless the context requires otherwise, the word 'comprise' or variations such as 'comprises' or 'comprising', will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

Any discussion of documents, acts, materials, devices, articles or the like, which has been included in the present specification, is solely for the purpose of providing a

context for the present invention. It is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present invention as it existed before the priority date of each claim of this application.

Description of the Figures

The invention will now be further explained and illustrated by reference to the accompanying figures in which:

Figures 1A to 1F are six plan-view (5 x 5 micron) AFM micrographs of sample structures A, B, C, D, E and F, each having an InAs epilayer, grown on a GaAs (100) substrate for 20, 30, 40, 50, 60 and 80 seconds, respectively.

Figure 2 is a graph illustrating the time dependence of average lateral size of InAs dots formed from the InAs epilayer.

Figure 3 is a schematic illustration of the indium atom dynamic (migration) on a GaAs substrate surface,

Figure 4A is a 20 x 20 micron perspective AFM scan of the sample shown in Figure 1E.

Figure 4B is a 20 x 20 micron plan AFM scan of the sample shown in Figure 1E.

Figure 5 depicts the surface morphology of the InAs buffer layer, grown on a GaAs (100) substrate for 80 seconds.

Figures 6A to 6D show plan view AFM micrographs of the samples following periods I, II, III and IV and show schematic cross-sectional representations of the samples at these periods.

Figures 7A and 7B show reflective high energy electron diffraction (RHEED) patterns during evolution of the InAs buffer layer, as the growth mode of the layer transforms from 3D to 2D.

Figure 8 is a Micro-Raman spectra graph of the InAs strain released epilayer.

Figures 9A and 9B are CSTIM images showing mismatch dislocations in the crystal structure, at different scan ranges.

Figures 10A and 10B are Depth-resolved CCM images of the top 50nm of the InAs epilayer, at different scan ranges.

Figures 11A and 11B are cross-sectional TEM images of different magnifications, showing trapping of threading dislocations by the InAs buffer layer and showing less dislocation density in the InAs epilayer.

Figures 12A and 12B are HR-XRD graphs of InAs/InAs SRL buffer/GaAs.

The invention will now be further described with reference to the following non-limiting example.

Experimental results

Seven samples A, B, C, D, E, F and G were prepared as described below.

Firstly, six samples were grown on semi-insulating GaAs (100) substrates using a solid source RIBER 32P molecular beam epitaxy (MBE) system. A 200 nm thick GaAs buffer layer was grown on the GaAs (100) substrate at 600 °C with 1.5 x 10^{-5} Torr As beam equivalent pressure (BEP).

On this layer of each sample, an InAs layer was grown for different durations at 500°C with 2.0 x 10^{-5} Torr As beam equivalent pressure at V/III ratio of 10:1, namely for 20, 30, 40, 50, 60 and 80 seconds and the samples were labelled A, B, C, D, E and F respectively.

A seventh sample, Sample G, was prepared using the same growth conditions as for the above epilayers. An InAs buffer layer was grown on the GaAs buffer layer (which overlays the GaAs (100) substrate) for 80 seconds. This InAs strain release layer (SRL) was formed having a thickness of less than 10 nm. Upon this SRL (or InAs buffer layer), 180 nm thick a 2D InAs epilayer was grown at 500 °C with V/III ratio of 50:1 at As BEP of 1.5 x 10^{-5} Torr.

Once preparation of the samples was complete, the samples were cooled to 200°C under As atmosphere before being removed from the MBE chamber.

The surface morphology of the samples was characterised by ex-situ AFM operating on a contact mode of a silicon nitride tip. Figures 1A to 1F show 5 x 5 μm plan-view AFM micrographs of samples A to F.

Figure 2 illustrates the dependence of lateral size of InAs dots on growth time, the whole growth procedure being shown as divided into four regions.

After initial epitaxial growth of a 2D wetting layer (e.g. after about 20 seconds), the strain is induced by about 7% lattice mismatch between the substrate and this epilayer. This strain drives the InAs epilayer to form islands in the Stranski-Krastanov

(S-K) growth mode in period I (from 0 to 20 s) as shown in Figure 1A. These islands coalesced and are not completely separated.

In period II (from 20 s to 50 s) the islands coalesce further and separate, as shown in Figures 1A to 1D. These figures show the growth of numerous InAs dots being over 400 nm in lateral size.

The size of InAs dots is controlled by the surface dynamics of In atoms on the substrate. At growth temperature of 500 °C, with low As BEP (2×10^{-7} Torr) and low V/III ratio (10:1), the indium atom migration length is enhanced. With In-As bond energy of 58.8 kJ/mol, an indium atom is not easy to combine with an arsenic atom. The indium atom can surmount the surface potential and easily migrate towards stable kink position as illustrated in Fig. 3. The indium atom surface migration length becomes longer compared to the case of higher V/III ratio growth condition. On the other hand, the nucleation area is proportional to the indium atom migration length. Therefore, long In atom migration length results in the formation of giant (over 400 nm) InAs islands in this region II. During such a growth it is also noticed that the lateral size, height and density of the InAs islands remain almost the same. The wetting layer is unstable and becomes thicker during this procedure. It has been reported that the wetting layer thickness might increase even after the nucleation of InAs/GaAs quantum dots.

It has been found that, with the further increase in growth time (beyond about 50 seconds), the InAs islands coalescence and this is evident from the existence of a uniform contrast as shown in Figure 1F. In this growth period III (from about 50 to 60 seconds), the strain between the InAs epilayer and the GaAs buffer layer becomes larger with increase in the growth time and the InAs epilayer becomes metastable.

In this period III, uniform giant InAs dots in sample E (see Figure 1E) are formed on the surface at about 60 s. The lateral size along the [110] orientation and the height of the dots are about 1.57 micron and 80 nm respectively. This is exemplified in Figure 4 which shows a 20 x 20 micron AFM scan of sample E. The plan-view micrograph shows that the density of InAs dots is about 5×10^{7} cm^{-2} and the distribution of lateral size and height is well within 10%. It is calculated that the volume of the InAs dots is almost the same as the total amount of InAs deposited. This means that the strain drives the adjacent dots along the wetting-layer to coalesce and the adatom detached from wetting layer to form giant dots. Recent theoretical models for InAs/GaAs quantum dots formation show that the strain leads to an increased number of adatoms detaching from the wetting layer and attaching to the InAs/GaAs quantum dots to cause a total increase in dot volume.

In the present case, almost all of the 2D wetting layer coalesced to form giant 3D InAs dots to release the strain between the InAs epilayer and the GaAs buffer layer. Such a process leads to the formation of giant size InAs dots, three to four times larger than the lateral size of InAs islands formed in region II. The lateral size deviation of these InAs dots is well within 10%.

In the region IV, after 80 s growth, the giant InAs dots disappear in sample F and the surface becomes flat as evident from the AFM micrograph (see Figure 1F). Longer In atom surface migration length leads to adjacent InAs dots to coalescing continuously and the strain between the InAs epilayer and the GaAs buffer layer is released. Thus an InAs strain release layer is created. This is also exhibited by Figures 7A and 7B which show a RHEED pattern being firstly spotty during the InAs growth (at 500°C growth temperature) and then these spots gradually diminish, and finally the RHEED pattern becomes streaky after 80 s of epitaxial growth.

From Figures 1F and 5, it can be seen that the root mean square (RMS) roughness of the InAs surface is only 0.369 nm, which can be compared with that of epi-ready wafers. It also means that the InAs surface turned out to be completely flat and is enough for further regrowth of a high indium composition layer. Figures 6A to 6D are AFM micrographs which schematically illustrate the growth and subsequent coalescing of giant InAs dots during the periods I-IV.

Figure 6A shows a sample structure after period I (i.e. 20 seconds). As can be seen, giant (over 450 nm) self-organised dots form due to long In atom surface migration length. Bright spots a and b represent two giant InAs dots forming on the surface.

Figure 6B shows a sample structure after period II (i.e. about 50 seconds). Dark spots a and d represent adatoms detaching from previous positions. Such adatoms coalesce to form InAs dusters (see bright spots b and c). Meanwhile, the wetting layer becomes thicker and the strain between the InAs epilayer and the GaAs buffer layer increases.

Figure 6C shows a sample structure after period III (i.e. about 60 seconds). Giant (over 1 nm) InAs dots have formed on the buffer layer.

Figure 6D shows a sample structure after period IV (i.e. about 80 seconds). As can be seen, the giant dots have dissipated having a relatively flat epilayer and the strain between the epilayer and the buffer layer appears to have been released.

During the InAs SRL growth, observation of in-situ RHEED pattern exhibits a change from spotty to streaky lines (see Figure 7B) and this shows the growth mode converting from 3D to 2D.

As mentioned above, an effective buffer should possess two functions:

(1) To accommodate the dislocations generated by lattice mismatch and release the strain between epilayer and substrate

(2) To trap the dislocation and prevent their propagation in to the epilayer grown on this buffer.

Accordingly, to prove such an InAs SRL is a good enough buffer for the epitaxial growth of high In content epilayer on top of it, a 180 nm InAs epilayer was grown above the InAs SRL under V/III ratio of 50:1 at As BEP 1.0 x 10^{-5} Torr (sample G). During the growth, observation of in-situ RHEED streaky pattern confirmed the 2D growth mode. The top InAs surface is substantially flat, as revealed by the AFM result, having a RMS roughness of 0.456 nm.

Figure 8 shows the micro-Raman spectra of sample G. The sample has been characterised by the spatially resolved Raman scattering using 514.5 nm line of an argon ion laser. The scattered light was dispersed through the JY-T64000 triple monochromator system attached to a liquid nitrogen cooled CCD detector. The accuracy during the Raman measurements was 0.2 cm^{-1} with a lateral spatial resolution of 1.2 μm. The scattered light was detected in several back scattering geometries, which correspond to either $z(xy)\bar{z}$ or the $z(xx)\bar{z}$ configurations. Raman spectra show InAs TO and LO phonons from the top strain free layer near 216.2 cm^{-1} and 235.2 cm^{-1} respectively. These values are very close to the values obtained from a LEC grown bulk InAs wafer (250 micron): LO: 215.6 cm^{-1} and 234.2 cm^{-1}. In the Raman spectra from this epilayer, we have observed a linewidth of 10.6 and 12.0 cm^{-1} for the TO and LO phonons, respectively. Such a narrow Raman linewidth of the epilayer suggests good crystalline quality. In addition, the spectra show consistency with the Raman selection rules and represent the (100) orientation. From these observations, it is apparent that the strain between the InAs epilayer and GaAs substrate has been released by InAs SRL buffer.

Beside the function of releasing the strain between the top InAs epilayer and GaAs substrate, InAs SRL buffer should also trap these mismatch dislocations and prevent their propagation into the epilayer grown on top of the buffer layer.

To prove that the mismatch dislocations can also be trapped by the InAs SRL buffer, the measurements of depth-resolved channelling contrast microscopy (CCM) and channelling scanning transmission ion microscopy (CSTIM) have been carried out which can be used to map variations in quality across a crystalline sample and to produce images of individual crystal dislocations. Top 50 nm InAs epilayer crystal quality was characterised by depth resolved CCM. The sample was thinned to 30 micron by removing most of the substrate for CSTIM analysis. CSTIM images are shown in Figurs 9A and 9B. Figure 9A shows a 500 x 500 nm scan range and Figure 9B shows a 50 x 50 nm scan range. The light coloured patterns indicate dechannelling ions and represent areas with mismatch dislocations in crystal. Depth-resolved CCM images are shown in Figures 10A and 10B. These images are of the top 50 nm of the InAs epilayer. Figure 10A shows a 200 x 200 nm scan range, and Figure 10B shows a 100 x 100 nm scan range. These images show a very uniform contrast which indicates very good crystal quality of the epilayer.

From the CSTIM images of Figures 9A and 9B, it can be seen that there is a layer, which is highly defective, as manifested by regions of alternate bright and dark contrast, indicating marked variations in adjacent crystal quality. From the CCM images shown in Figures 10A and 10B the distributions in signal, measured from a depth of up to 50 nm at the epilayer surface, show no change in contrast similar to that in the CSTIM results. Therefore, it is deduced that the contrast in the CSTIM images is located at a depth greater than 50 nm.

Cross-section transmission electron microscopy (TEM) images shown in Figures 11A and 11B confirm the efficient confinement of mismatch dislocations inside the InAs SRL buffer. The images show that the threading dislocations are trapped by InAs SRL and there is less dislocation density in the InAs epilayer. InAs SRL effectively accommodates the threading dislocations and prevents them from extending into the top InAs epilayer. The images confirm that the top InAs epilayer crystal quality is good. This is further confirmed from the narrow HR-XRD InAs peaks shown in Figure 12. On the other hand, the lattice constants calculated from (004) and from (022) and $(0\bar{2}2)$ orientation fit well with the theoretical value 0.606 nm adopted from Ioffe Institute Semiconductor materials properties sheet, which also imply that the strain has been fully released by the InAs SRL buffer.

It is concluded that the InAs SRL buffer described above is superior for the growth of strain-free epilayers for electronic and optical structures.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as described herein without departing from the spirit or scope of the invention. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive.

Claims

1. A semiconductor structure having high electron mobility, for use in high electron mobility transistors (HEMT's) or field effect transistors (FET's), said structure comprising:

   - a GaAs substrate;
   - an epilayer of a high indium content material; and
   - an InAs buffer layer located intermediate the substrate and the epilayer,

   wherein the GaAs substrate has a first lattice constant, the epilayer has a second lattice constant different from the first lattice constant, and the InAs buffer layer is adapted to release strain caused by mismatch of said different lattice constants.

2. A semiconductor structure according to claim 1, wherein the GaAs substrate includes a GaAs buffer layer formed thereon.

3. A semiconductor structure according to claim 2, wherein the GaAs buffer layer has a thickness of between about 100 nm and 300 nm.

4. A semiconductor structure according to claim 3, wherein the GaAs buffer has a thickness of about 200 nm.

5. A semiconductor structure according to any one of the claims 1 to 4, wherein the high indium content epilayer is chosen from the group comprising InAs, InGaAs and InAlAs.

6. A semiconductor structure according to any one of the claims 1 to 5, wherein the epilayer has an indium content of more than about 90%.

7. A semiconductor structure according to any one of the claims 1 to 5, wherein the epilayer has an indium content of less than about 90% and said structure further includes an additional buffer layer located between the InAs buffer layer and the epilayer.

8. A semiconductor structure according to claim 7, wherein the lattice constant of the additional buffer layer is substantially the same as the lattice constant of the epilayer.

9. A semiconductor structure according to claim 8, wherein the lattice constants of the additional buffer layer and the epilayer differ by about 1% or less.

10. A semiconductor structure according to claim 9, wherein the epilayer is formed of InAlAs and the additional buffer layer is formed of InAlAs or InGaAs.

11. A semiconductor structure according to claim 10, wherein the epilayer is formed of InGaAs and the additional buffer layer is formed of InGaAs or InAlAs.

12. A semiconductor structure according to any one of the claims 1 to 11, wherein the thickness of the InAs buffer layer is less than about 100 nm.

13. A semiconductor structure according to claim 12, wherein the thickness of the InAs buffer layer is less than about 20 nm.

14. A semiconductor structure according to claim 13, wherein the thickness of the InAs buffer layer is less than about 10 nm.

15. A semiconductor structure according to claim 14, wherein the thickness of the InAs buffer layer is about 7 nm.

16. A semiconductor structure according to any one of the claims 1 to 15, wherein the surface of the InAs buffer layer has a root mean square roughness of less than about 1 nm.

17. A semiconductor structure according to claim 16, wherein the surface of the InAs buffer layer has a root mean square roughness of less than about 0.500 nm.

18. A semiconductor structure according to claim 17, wherein the surface of the InAs buffer layer has a root mean square roughness of less than about 0.400 nm.

19. A semiconductor structure according to any one of claims 1 to 18, wherein the GaAs substrate is formed of GaAs (100).

20. A method of producing the semiconductor structure of any one of claims 1 to 19, said method comprising the steps of:

(a) growing an InAs buffer layer on a GaAs substrate, and;

(b) growing an epilayer of a high indium content material on the InAs buffer layer.

21. A method according to claim 21, wherein, prior to step (a), the method includes the further step of growing a GaAs buffer layer on the GaAs substrate, in which case said InAs buffer layer is then formed on the GaAs buffer layer.

22. A method according to claim 20 or 21, wherein the buffer layers and the epilayer are grown by molecular beam epitaxy (MBE).

23. A method according to any one of the claims 20 to 22, wherein the InAs buffer layer and the epilayer are grown at a temperature of between about 250°C and 550°C.

24. A method according to claim 23, wherein the InAs buffer layer and the epilayer are grown at an As beam equivalent pressure of between about 1.0×10^{-5} and 2.0×10^{-5} Torr.

25. A method according to any one of the claims 20 to 24, wherein the GaAs buffer layer is grown at a temperature of about 600°C and at an As beam equivalent pressure of about 1.5×10^{-5} Torr.

26. A method according to claim 22, wherein the molecular beam epitaxy is effected by a solid source RIBER™ 32 P MBE system.

27. A method according to claim 22, wherein the InAs buffer layer is deposited by molecular beam epitaxy at a low V/III ratio of less than about 15.

28. A method according to claim 22, wherein the epilayer is deposited by molecular beam epitaxy at a V/III ratio up to about 50:1.

29. A method according to any one of the claims 20 to 28, wherein the InAs buffer layer is grown for between about 70 and 100 seconds.

30. A semiconductor structure fabricated according to the method of any one of claims 20 to 29.

31. A semiconductor structure having high electron mobility, substantially as hereinbefore described with reference to the examples and any one or more of the Figures.

32. A method of producing the semiconductor structure of claim 31, said method being substantially as hereinbefore described with reference to the examples.