

Methods for variable tilt angle etching, pattern improvement, cyclic surface conditioning, and etching sidewalls of features

Field

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This technology relates to the field of semiconductor manufacturing, specifically the area of processes for sidewall roughness control, structural defect reduction of features on a substrate, etching sidewalls of features on a substrate, and methods for improving the smoothness and uniformity of various surfaces, such as semiconductor, metal, dielectric, and 2D material surfaces. This is a crucial process in the manufacturing of integrated circuits, microelectromechanical systems (MEMS), and other micro- and nano-scale devices.

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Background

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In the field of semiconductor processing, it is often desirable to create precise patterns, structures, and features on a substrate surface. These structures are typically formed using photolithography techniques, where a pattern is defined in a light-sensitive material called a resist. The resist is then used as a mask to transfer the pattern onto the substrate by etching or deposition.

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One of the main challenges in semiconductor processing is the reduction of line edge roughness (LER). LER is quantified as the root-mean-square deviation of the line edge profile shape from the ideal straight line in the horizontal plane. The LER is one of the most critical indicators of fabrication process performance, and thus obtaining a substantial LER value is a well-known challenge in modern, leading-edge semiconductor processing. The LER is caused by several effects in the fabrication processes. When LER becomes comparable with the Critical Dimensions (CDs) of the semiconductor devices, it becomes increasingly difficult to control processes and achieve well-defined, repeatable structures. As the feature size is reduced well below 100 nm, the LER will eventually become the resolution-limiting factor in lithography since LER does not scale with the feature size. Therefore, minimizing the LER to achieve the highest resolution possible is essential.

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Reduced sidewall roughness is important not only for lines, for which it is typically referred to as LER, but for all different structures on the substrate, such as dots, holes, fins, and other structures, including those used in microelectromechanical systems (e.g., resonators). In this case, it is important to reduce the sidewall profile deviations from the sidewall tangent plane. We will refer to all this further in the text as the sidewall roughness reduction. In a more general

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sense, this will be referred to as the sidewall roughness control, which implies that the sidewall surface is conditioned to the desired roughness level on different specific surfaces. Furthermore, it is important to be able to reduce structural defects efficiently, such as sidewall striations, bows, and scallops, horizontal top surface roughness, and minimize different layers and areas damaged during previous processing. We will refer to this further in the text as structural defect reduction.

In view of the foregoing, it would be desirable to provide a method for reducing LER and sidewall roughness control of different features on the substrate and a method for structural defects reduction, which overcomes the shortcomings of the prior art. The present disclosure addresses these and other objectives.

Summary

In a first aspect, the present invention provides a method for sidewall roughness control and structural defect reduction of features on a substrate. The method includes adjusting the tilt angle of a particle beam for angled particle beam etching of at least one sidewall of the features.

In some embodiments, the method further comprises a combination of conformal deposition and variable tilt angle etching to achieve the sidewall roughness control and structural defect reduction. The method may also include alternating deposition and etching steps to achieve the sidewall roughness control and structural defect reduction.

Optionally, the method may further comprise a self-limiting reaction, such as chemisorption, deposition, extraction, oxidation, nitridation, or conversion. The particle beam used in the method may comprise neutrals, radicals, photons, ions, electrons, or a combination thereof. The tilt angle of the particle beam can range from 0-85 degrees from the angle of the normal of the substrate.

In some embodiments, the sidewall roughness control results in line edge roughness (LER) reduction of at least 50%. The sidewall roughness control and defect reduction may comprise adjusting the tilt angle of the particle beam during angled etching or self-limiting reaction, or a combination thereof. The deposition or etching or self-limiting reactions or their combination may be selectively applied to specific areas.

In certain embodiments, the deposition is performed with atomic layer deposition (ALD). The substrate with its patterned 2-dimensional and 3-dimensional features and particle beam may be rotated with respect to each other during the angled etching. The sidewall roughness control may result in sidewall roughness reduction. The angled etching may be performed using atomic layer etching (ALE).

In some embodiments, the etch process is selective to silicon or silicon oxide. The particle beam tilt can also be 0 degrees from the angle of the normal to the substrate, and therefore the process can be performed without adjusting the tilt angle of a particle beam during particle beam etching. The deposited material may be amorphous or glass-like.

Optionally, at least some of the beam particles have a lower atomic mass than at least one of the components of the exposed surface. The method may further include rapid surface temperature cycling. The deposited material may be the same as the material being etched.

According to a second aspect of the disclosure, a method is provided for sidewall roughness reduction of features on a substrate. The features are spaced apart and have respective field regions and sidewalls. The field regions (*<- to be removed, kept to not erase comments*). The method comprises forming a patterned and selectively protecting masking layer so that at least part of the field regions are masked and the sidewalls are unmasked. The method also comprises performing dry etching in a process chamber enclosing the substrate. This involves creating a horizontal component of a direction of the etching by setting a pressure in the process chamber to exceed a defined pressure threshold for a sidewall etching. The horizontal component etches the unmasked sidewalls for said roughness reduction of the sidewalls. This method allows for precise etching of the sidewalls, and thus reducing the roughness of the sidewalls, without requiring on tilting of the substrate or particle beam to target the sidewalls with directional etching. The process is thus less complex than previous solutions to implement.

Optionally in some examples, the defined pressure threshold for sidewall etching is 40 mTorr. This specific pressure threshold has been found to be particularly effective in creating the desired horizontal component of the etching direction, leading to a more efficient and effective roughness reduction.

Optionally in some examples, the dry etching is self-limiting, whereby the dry etching stops when the sidewall roughness is reduced with a threshold amount. The plasma energy is lower than the binding energy of the bulk of the material of the original features. This allows the etch

process to stop after the roughness is removed and the applied plasma has lower energy than the remaining material, preventing over-etching.

5 Optionally in some examples, the sidewall roughness is reduced by at least 50%. This significant reduction in roughness can greatly improve the performance and reliability of the features on the substrate.

10 Optionally in some examples, a line edge roughness of the sidewalls is reduced to a value below 1 nm root mean square (RMS). The line edge roughness (LER) here quantified as the root-mean-square (RMS) deviation of the line edge profile shape from the straight line in the horizontal plane. This extremely low level of roughness can further enhance the performance of the features, particularly in applications where very high precision is required.

15 Optionally in some examples, the method further comprises a self-limiting reaction. A self-limiting reaction is a reaction that slows down or stops as a function of time or, equivalently, as a function of species dosage. Self-limiting reactions may include, but are not limited to chemisorption, deposition, conversion (e.g., oxidation, nitridation), and extraction. Chemisorption is a chemical adsorption process, caused by a reaction on an exposed surface, which creates an electronic bond between the surface and the adsorbate with a binding energy
20 greater than 0.5 eV per adsorbed species. During the chemical reaction, a distinct chemical species is created on the adsorbent surface, which causes the bond to be created. In the extraction case, the original material is a compound, with the modification removing one element preferentially from the surface, while the other element is removed in the subsequent removal step. These reactions can provide additional control over the etching process, further
25 enhancing the precision and effectiveness of the roughness reduction.

30 Optionally in some examples, the self-limiting reaction or dry etching is selectively applied to specific areas of the substrate. This selectivity means that processes are applied preferentially on some specific surfaces or materials while being suppressed on other surfaces or materials, i.e. the suppressed processes have a substantially reduced process rate. This selective application allows for even greater control over the etching process, enabling the roughness reduction to be tailored to the specific needs of different areas of the substrate.

35 Optionally in some examples, the dry etching is performed using atomic layer etching (ALE). ALE is a highly precise etching technique that can further enhance the effectiveness and precision of the roughness reduction.

Optionally in some examples, the dry etching is a cyclic etching process. This cyclic process can provide additional control over the etching, allowing for more precise and effective roughness reduction.

- 5 Optionally in some examples, the dry etching is selective to a material comprising any of silicon, silicon oxide, silicon nitride, hafnium oxide, aluminium oxide. This selectivity can be particularly beneficial in applications where the features on the substrate are made of these materials, as it allows for precise and effective roughness reduction without damaging other materials on the substrate.

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Optionally in some examples, the method further comprises rapid surface temperature cycling. Rapid surface temperature cycling here is defined as rapid heating and cooling of surfaces which can be done once or repeated multiple times. The process of heating takes less than 5 min in some examples, typically less than 30 s. This can enhance the effectiveness of the etching process, leading to more efficient and effective roughness reduction.

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Optionally in some examples, the rapid surface temperature cycling is done through surface exposure to plasma. This can provide a highly effective means of rapidly cycling the surface temperature, further enhancing the effectiveness of the etching process.

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Optionally in some examples, the rapid surface temperature cycling is assisted with flashlight. This can provide a convenient and effective means of rapidly cycling the surface temperature, further enhancing the effectiveness of the etching process.

- 25 Optionally in some examples, the rapid surface temperature cycling assisted with flashlight is done using a laser light source. This can provide a highly precise and effective means of rapidly cycling the surface temperature, further enhancing the effectiveness of the etching process.

30 Optionally in some examples, the features on the substrate comprises any of micro- and nano-scale devices, waveguides, transistors, fins, ridges, trenches, holes, and/or pillars. This method can be applied to a wide range of different features, making it highly versatile and applicable to a wide range of different applications.

35 According to a third aspect of the disclosure, a method for surface conditioning based on cyclic processing is provided. The method includes activating a surface, removing excess materials from the surface and surrounding environment, applying a low-energy particle treatment to the surface, and repeating the above steps until the surface has a desired smoothness. Optionally,

the low-energy particle treatment uses ions, and may be atomic layer etching (ALE) or atomic layer etching with molecular activation. The cyclic processing may also comprise deposition steps, which can result in an atomic layer deposition (ALD).

- 5 The method may include a combination of etching and deposition, and may involve alternating etching and deposition. The repeating of the steps can be performed until the process has no further effect on different processed surfaces. The method may further comprise ion beam shaping technology and angled particle beam etching.
- 10 The surface treated by the method can be a side wall surface or an inclined surface, and may be selected from the group consisting of semiconductor surfaces, metal surfaces, dielectric surfaces, and 2D material surfaces. The surface can be a patterned surface or a non-patterned surface.
- 15 The activation of the surface may comprise applying a gas exposure to the surface, exposing the surface to a chemical solution, heating the surface to a specific temperature, or applying a particle beam to the surface. The low-energy particle treatment may comprise a low-energy particle beam with a particle energy between 10 eV and 100 eV, or a low-energy plasma treatment with a plasma power between 1 W and 50 W.
- 20 A surface conditioned by the method is also provided.

According to a fourth aspect of the disclosure, a method for etching sidewalls of features on a substrate is provided. The features are spaced apart and have respective field regions and sidewalls. The method comprises providing a compound masking layer on the features. This compound masking layer comprises a first masking layer and a second masking layer over the first masking layer. At least part of the field regions is masked and the sidewalls are unmasked by the compound masking layer. The method further comprises etching the sidewalls. During this process, the second masking layer prevents etching of the first masking layer so that a height of the features and the first masking layer with respect to the substrate is maintained. The method comprises removing the first masking layer, whereby any remaining part of the second masking layer is removed. This method ensures that the features are left on the substrate with their original intended height, thus preventing height reduction of the features during sidewall etching.

35 Optionally in some examples, the first masking layer has the same etch properties as the features on the substrate. This means that etching of the sidewalls of the features removes

material of sidewalls of the first masking layer at least at the same rate as for the material of the features. This ensures that the first masking layer and features on the substrate can be removed at the same rate upon the sidewall etching.

- 5 Optionally in some examples, the second masking layer is formed of a material with a lower etch rate than the material of the first masking layer. This prevents etching of the first masking layer during the sidewall etching, maintaining the height of the features and the first masking layer with respect to the substrate.
- 10 Optionally in some examples, the first masking layer is selectively removed after etching of the sidewalls. This ensures that a height of the features after the sidewall etching is the same as before the sidewall etching. It also removes any remaining part of the second masking layer and any residual material, leaving the features on the substrate with their original intended height.
- 15 Optionally in some examples, the first masking layer separates the features from residual material after the etching of the sidewalls. This separation allows the features to have an essentially uninterrupted vertical sidewall with respect to the substrate after sidewall etching, and thus providing for a subsequent facilitated removal of the residual material.
- 20 Optionally in some examples, the residual material is attached to the first and/or second masking layer and is thereby removed with the removal of the first masking layer. This ensures that the features are left on the substrate with their original intended height, and the residual material is instead attached to the first masking layer and/or second masking layer to facilitate
- 25 its removal without affecting the features.
- 30 Optionally in some examples, the compound masking layer comprises a third masking layer. The third masking layer is arranged between the features and first masking layer. The material of the third masking layer is different from the material of the features. This is advantageous when it is difficult to find an appropriate material for the first masking layer. The third masking layer separates the features from residual material after sidewall etching, providing for the features to have an essentially uninterrupted vertical sidewall with respect to the substrate after sidewall etching. Selective removal of the third masking layer results in removal of the entire compound masking layer after sidewall etching, leaving the features with the originally
- 35 intended height on the substrate.

Optionally in some examples, the thickness of the third masking layer is less than the thickness of the first masking layer. This ensures that the third masking layer is thin enough to be effectively etched at least at the same rate as the sidewalls of the features while separating the features from the first masking layer.

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Optionally in some examples, the thickness of the third masking layer is less than 10 nm.

Optionally in some examples, an etch rate of sidewalls of the third masking layer corresponds at least to an etch rate of the sidewalls of the features, upon said etching of the sidewalls of the features. This ensures that the third masking layer and the features on the substrate can be removed at the same rate upon the sidewall etching.

Optionally in some examples, the material of the first masking layer is the same as the material of the features. The first masking layer can be provided as a soft mask with the same material as the features, thereby exhibiting the same etch properties as the features, while it can be readily removed when being separated from the features by a third masking layer.

Optionally in some examples, the method includes removing the third masking layer whereby the first masking layer and any remaining part of the second masking layer is removed. This ensures that the entire compound masking layer is removed after the etching of the sidewalls, leaving the features on the substrate with their original intended height.

Optionally in some examples, the third masking layer separates the features from residual material after the etching of the sidewalls so that the features have an essentially uninterrupted vertical sidewall with respect to the substrate. This ensures that the features are left on the substrate with their original intended height, and the residual material is instead attached to any of the masking layers.

Optionally in some examples, the third masking layer separates the first masking layer from the features so that the features and the third masking layer have an essentially uninterrupted vertical sidewall with respect to the substrate after the sidewall etching. This ensures that the features are left on the substrate with their original intended height, and the residual material is instead attached to the first and/or second masking layer.

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Brief Description of the Drawings

The disclosure will now be described in more detail with reference to the accompanying drawings. The figures should not be considered limiting; instead, they are used for explaining and understanding:

5 Figures 1a-1f illustrate the cyclic sidewall roughness and defect reduction process using self-limiting reaction and angled particle beam etching, resulting in a final structure with the desired sidewall roughness. Two cycles are exemplified in this case.

Figures 2a-d illustrate the cyclic sidewall roughness and structural defect reduction process using a combination of atomic layer deposition (ALD) and variable tilt angle etching. One cycle is exemplified in this case.

10 Figure 3 is a block diagram illustrating an execution process flow of a method combining ALD and variable tilt angle etching for sidewall roughness control.

Figure 4 is a schematic representation of the desired size and profile of the patterned features on a substrate.

15 Figure 5 is an illustration of the real surface of the features before completing the method for sidewall roughness reduction, also known as Atomic Level Improvement.

Figure 6 shows a large structure after lithography and before Atomic level Pitch Splitting (APS).

Figure 7 depicts the structure after APS and before completing the method for sidewall roughness reduction.

20 Figure 8 illustrates the structure after APS and after completing the method for sidewall roughness reduction.

Figure 9 shows an example of the surface conditioning method based on cyclic processing.

Figure 10 shows another example of the surface conditioning method based on cyclic processing.

25 Figure 11 shows another example of the surface conditioning method based on cyclic processing.

Figure 12 is a flowchart illustrating the method for surface conditioning based on cyclic processing according to an example of the present disclosure.

Figure 13 is an atomic force microscopy (AFM) micrograph of the initial surface and a final surface after the cyclic process according to an example.

30 Figures 14A-B are cross-sectional views of a substrate at various intermediate stages of angled particle beam etching without any masking layer, where both the width and the height of the features are reduced.

35 Figures 15A-C are cross-sectional views of a substrate at various intermediate stages of angled particle beam etching with a hard mask layer 4300 and after the masking layer and the unwanted structure 4131 removal, showing the formation of artifact features during the etching process.

Figures 16A-C are cross-sectional views of a substrate at various intermediate stages of angled particle beam etching with a compound masking layer comprising the first masking layer 4400 and the second masking layer 4300, where the original vertical size of the features is maintained after the removal of the compound masking layer.

- 5 Figures 17A-C are cross-sectional views of a substrate at various intermediate stages of angled particle beam etching with a compound masking layer comprising a third masking layer 4500, the first masking layer 4400, and the second masking layer 4300, illustrating the preservation of the original vertical size of the features after the removal of the masking layers.

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Definitions of terms

- Angled particle beam etching – surface etching operating in a specific regime when etching occurs only when driven by particle beam impingement. The particle beam may comprise
15 neutrals, radicals, photons, ions, electrons, or a combination thereof. The particle beam tilt angle may range between 0 and 85 degrees from perpendicular to the surface plane.

- Perpendicular to the surface plane – perpendicular to any 2 intersecting lines in the surface plane.

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- Variable tilt angle etching - adjusting the tilt angle of a particle beam for angled particle beam etching.

- Particle beam – a plurality of incoming particles having an angular velocity distribution less
25 than 10 degrees Full Width at Half Maximum (FWHM).

- Sidewall roughness control – the sidewall surface conditioning to the desired roughness level of the sidewall surface. The sidewall surface roughness is quantified as the root-mean-square of the sidewall profile deviations from the sidewall tangent plane.

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- Structural defect reduction – the reduction of such structural surface defects as sidewall striations, bows, point defects, scallops, and roughness of horizontal surfaces. This defect reduction also includes the minimization of different surface layers and areas damaged during previous processing, for instance, during previous etching processes.

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- Atomic layer etching (ALE) – defined as an etching technique that uses sequential half-reactions resulting in layer-by-layer material subtraction. The ALE implementation consists of

at least two sequential steps: surface modification (reaction A) and removal (reaction B). These reactions can be cycled, and at least one step is at least partly self-limiting. The modification step forms a thin reactive surface layer with a well-defined thickness that is subsequently more easily removed than the unmodified material. The layer is characterized by a sharp gradient in chemical composition. Removal methods include thermal desorption, particle bombardment, and chemical reaction. Here in the ALE processes, we also include quasi-atomic layer etching processes, which may include quasi-self-limiting reactions and non-self-limiting reactions.

- Self-limiting reactions – reactions that slow down or stop as a function of time or, equivalently, as a function of species dosage. Self-limiting reactions may include, but are not limited to chemisorption, deposition, conversion (e.g., oxidation, nitridation), and extraction. In the extraction case, the original material is a compound, with the modification removing one element preferentially from the surface, while the other element is removed in the subsequent removal step.

- Chemisorption - a chemical adsorption process, caused by a reaction on an exposed surface, which creates an electronic bond between the surface and the adsorbate with a binding energy greater than 0.5 eV per adsorbed species. During the chemical reaction, a distinct chemical species is created on the adsorbent surface, which causes the bond to be created.

- Physisorption - the adsorption in which the molecular interactions between the adsorbate molecules and the adsorbent are primarily governed by Van der Waals forces, and the binding energy between the surface and the adsorbate per adsorbed species is 0.5 eV or less.

- Atomic layer deposition (ALD) – defined as a deposition technique that uses sequential half-reactions resulting in layer-by-layer material addition. These reactions can be cycled, and at least one step is at least partly self-limiting. Here in the ALD processes, we also include quasi-atomic layer deposition processes, which may include quasi-self-limiting reactions and non-self-limiting reactions.

- Exposed surface – the substrate surface which is being subjected to the treatment.

- Rapid surface temperature cycling – rapid heating and cooling of surfaces which can be done once or repeated multiple times. The process of heating takes less than 5 min, typically less than 30 s.

- Line edge roughness (LER) - quantified as the root-mean-square deviation of the line edge profile shape from the straight line in the horizontal plane.
- Selective process – process applied preferentially on some specific surfaces or materials while being suppressed on other surfaces or materials.
- Suppressed process – a process with a substantially reduced process rate.
- Conformal deposition – a deposition that has the same rate on all surfaces irrespective of their geometrical orientation. ALD is one example of conformal deposition.

Detailed Description

The present disclosure will now be described in detail with reference to example embodiments. It should be understood that these example embodiments are provided for illustrative purposes only and are not intended to limit the scope of the present disclosure.

A. Variable Tilt Angle Etching

According to an embodiment shown in Figure 1, a sidewall roughness control method is provided for improving the sidewall roughness of the features on a substrate. Substrate 100 has features 110 with sidewalls 111 and 112, which have an initial sidewall roughness. The method includes the step of the self-limiting reaction 300, shown in Figures 1b and d, and the step of angled particle beam 200 etching, shown in Figures 1c and e, so as to modify sidewalls 111 to sidewalls 113 and 114 to reduce the sidewall roughness of the features 110.

As shown in Figures 1a-1f, the following steps may occur during the sidewall roughness reduction process utilizing angled particle beam etching of the sidewalls of the features:

- In Figure 1a, the initial structure with the sidewall roughness is shown, where features 110 are formed on substrate 100. The sidewalls 111 and 112 of the features 110 have an initial surface roughness that needs to be reduced to improve the sidewalls.
- In Figures 1b and d, the initial structure is processed with a self-limiting reaction 300. This self-limiting reaction slows down or stops as a function of time or, equivalently, as a function of species dosage. Self-limiting reactions may include, but are not limited to chemisorption, deposition, conversion (e.g., oxidation, nitridation), and extraction. In the extraction case, the

original material is a compound, with the modification removing one element preferentially from the surface, while the other element is removed in the subsequent removal step. In the case of chemisorption, a reaction on an exposed surface creates an electronic bond between the surface and the adsorbate.

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- In Figures 1c and e, a particle beam source (not shown in the figure) generates an angled particle beam 200 adjusted to an appropriate tilt angle to create an angled particle beam etching of the sidewalls 111 and 113 of features 110.

10 • In Figure 1f, a post-processed structure is shown after the angled particle beam etching process. The original sidewalls 111 are now converted to sidewalls 114, which exhibit a new surface roughness, which is less than the initial surface roughness, while the sidewalls 112, which were not exposed to the angled particle beam etching, remain the same or have only a minimal modification. The now-smoothed sidewall surfaces lead to a reduction in sidewall
15 roughness of the features 110 only on one side in this case.

In a variation, as shown in Figures 2a-2d, the sidewall roughness reduction process can involve a combination of conformal deposition, preferably ALD, and variable tilt angle etching.

20 • In Figure 2a, the initial structure with sidewall roughness, which is the same as shown in Figure 1a.

- In Figure 2b, the initial structure is processed with a conformal thin film 400 deposition, preferably ALD, resulting in new sidewalls 115 of the features 110.

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- In Figure 2c, a variable tilt angle particle beam 501 and 502 assisted etching performs angled particle beam etching of sidewalls 115, which results in smoothing the initial surface roughness of these sidewalls.

30 • In Figure 2d, the final structure is shown, with the desired sidewall surface 114 and reduced sidewall roughness of features 110 while preserving the original critical dimensions of the features 110.

A1. Apparatus

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In one example, the apparatus for sidewall roughness control and structural defect reduction of features on a substrate comprises a particle beam source, a wafer, a substrate holder, and

a vacuum chamber or a few separate vacuum chambers. The apparatus may be designed to provide a controlled environment for etching and deposition processes, ensuring precise control over the tilt angle of the particle beam, and enabling the reduction of sidewall roughness and defects in the features on the substrate.

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A1.1. Particle Beam Source

In some examples, the particle beam source generates the ion beam for surface irradiation purposes, which may include ion beam-assisted etching and deposition processes. The particle beam source may comprise a variable tilt angle mechanism that adjusts the ion beam tilt angle for optimized processing, including etching and deposition. The variable tilt angle mechanism may have a tilt angle range of 0-85 degrees from the angle of the normal of the wafer and a tilt angle precision of within 10 degrees, preferably within 1 degree. The particle beam may comprise different species such as neutrals, radicals, ions, electrons, photons, or a combination thereof. Examples of ion species include helium (He), argon (Ar), nitrogen (N), oxygen (O), fluorine (F), chlorine (Cl), bromine (Br), gallium (Ga), hydrogen (H), neon (Ne), krypton (Kr), xenon (Xe), iodine (I) and astatine (At). The ion energy range may be below 5000 eV, with an example ion energy range of 0-2000 eV. The ion beam may be line focused with a length of greater than 10 mm, with examples of ion beam lengths of over 200 mm and up to 400 mm. The ion beam divergence angle may be tunable and less than 10 degrees FWHM, and the ion beam uniformity may be within 2% over the wafer surface. The particle beam may also comprise neutral beams, radical beams, photon beams, electron beams, or a combination of particle beams. The apparatus may include an angled particle beam 200 adjusted to an appropriate tilt angle to create an angled particle beam etching, or a variable tilt angle particle beam 501 and 502 for variable tilt angle etching.

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A1.2. Wafer

In some examples, the wafer is the substrate that is supported and positioned during processing by the substrate holder in the vacuum chamber. The wafer may be made of various materials, such as silicon, aluminum oxide, or other semiconductor, metallic or dielectric materials, and may have various sizes and shapes depending on the specific application. Typically, the wafers have a round shape with some flats and notches on the side.

35 A1.3. Substrate Holder

In one example, the substrate holder supports and positions the substrate during processing. The substrate holder may be designed to hold the substrate securely and accurately, ensuring proper alignment and positioning of the substrate during the processes. The substrate holder may also be designed to allow for easy loading and unloading of the substrate, facilitating efficient processing, and minimizing the risk of damage to the substrate.

A1.4. Vacuum Chamber

In some examples, the vacuum chamber provides a controlled environment for processes. The vacuum chamber may have a base vacuum pressure of 10^{-6} Torr or better, and a process pressure control range of 10^{-9} to 1 Torr, with accuracy within 25% of the process pressure. An example of process pressure control within a range of 10^{-5} to 10^{-1} Torr may be used. The vacuum chamber may also have a substrate holder temperature control within a temperature range of -196°C to 500°C , with an accuracy of 2°C or better, and the chamber wall temperature control within a temperature range of 25°C to 350°C , with an accuracy of 2°C or better. The vacuum chamber may be designed to maintain a stable and controlled environment during the processes, ensuring consistent and accurate results.

The advantages of the apparatus and its components include precise control over the tilt angle of the particle beam, enabling control of sidewall roughness, and reduction of structural defects in the features on the substrate. The apparatus may also provide a controlled environment for etching and deposition processes, ensuring consistent and accurate results. The apparatus may further comprise optional features, such as additional self-limiting reactions or rapid surface temperature cycling, which can enhance the sidewall roughness control and structural defect reduction capabilities of the apparatus.

A2. Sidewall roughness control and structural defect reduction

In one example, the sidewall roughness control may comprise line edge roughness (LER) reduction. The walls of features, where the walls have the LER, may have a wall aspect ratio of up to 1:10, a wall angle that is preferably perpendicular to the substrate but can vary plus or minus 60 degrees (or plus or minus 30 degrees), a wall surface roughness between 0.5-5.0 nm RMS, and a wall shape that is concave or convex. The method may achieve a line edge roughness (LER) reduction of at least 50%, or alternatively, the resulting line edge roughness may be below 2 nm, or the method may achieve sub-1 nm LER.

A3. Angled particle beam etching

In one embodiment, the angled particle beam etching process involves etching at least one sidewall of the features on a substrate. This process can be used to control sidewall roughness and reduce structural defects, resulting in improved device performance and yield.

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A3.1 Atomic Layer Etching (ALE) and Selectivity

In some examples, the angled particle beam etching process may comprise atomic layer etching (ALE). ALE is a self-limiting etching process that allows for precise control of the etch depth and selectivity. The process may involve alternating steps of self-limiting reactions and angled particle beam etching, which can be selective to specific materials, such as silicon or silicon oxide. This selectivity can be advantageous in achieving precise etching of the desired material while minimizing damage to underlying unetched material and to other materials present in the device structure.

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A3.2. Variable and fixed tilt angle etching

In one example, the angled particle beam etching process may involve adjusting the tilt angle of the particle beam during the etching process. The tilt angle can be varied within a range of 0-85 degrees from the angle of the normal of the substrate, with a precision of within 10 degrees, preferably within 1 degree. This variable tilt angle etching allows for optimized etching of the sidewalls of the features as well as their horizontal top surfaces, resulting in improved sidewall roughness control and structural defect reduction.

In another example, the angled particle beam etching process may involve fixing the tilt angle of the particle beam during the etching process.

A3.3. Rotation of Features and Particle Beam

In some examples, the substrate with its patterned 2-dimensional and 3-dimensional features and the particle beam may be rotated with respect to each other during the angled particle beam etching process. This rotation can be of varying speed and can help to ensure a desired etching of the sidewalls of the features, further improving sidewall roughness control and structural defect reduction.

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A4. Conformal Deposition and Atomic Layer Deposition (ALD)

In one embodiment, the sidewall roughness control and structural defect reduction process may comprise conformal deposition, which is a deposition technique that allows for the uniform deposition of a thin film on a substrate with complex topography. Conformal deposition may be particularly advantageous for depositing thin films on high aspect ratio features, as it can provide a uniform coverage of the film on all surfaces of the features, thereby reducing the sidewall roughness and reducing structural defects if followed with the angled particle beam etching.

In some examples, the conformal deposition may be performed using atomic layer deposition (ALD), which is a self-limiting deposition technique that allows for the precise control of the film thickness at the atomic level. ALD may comprise a sequence of alternating and self-limiting surface reactions, which can result in the formation of a highly uniform and conformal thin film on the substrate. The use of ALD for conformal deposition may provide several advantages, such as improved film quality, precise control of the film thickness, and excellent coverage on high aspect ratio features and three-dimensional structures and features.

A4.1. Alternating angled particle beam etching and conformal deposition

In some examples, the sidewall roughness control and structural defect reduction process may comprise alternating steps of angled particle beam etching and conformal deposition. The angled particle beam etching may be used to selectively remove material from the sidewalls of the features, while the conformal deposition may be used to deposit a thin film on the etched sidewalls, thereby smoothing the sidewall roughness and reducing structural defects while preserving critical dimensions (CDs). The alternating steps of angled particle beam etching and conformal deposition may be repeated multiple times to achieve the desired sidewall roughness control and structural defect reduction. Either angled particle beam etching or conformal deposition may be the starting step in this process.

A4.2. Further options

In some examples, the conformal deposition process may comprise depositing a material that is the same as the material being etched by the angled particle beam etching process. This may be advantageous for preserving the original critical dimensions of the features while reducing the sidewall roughness and structural defects. In this case, it may be especially advantageous to do the angled particle beam etching at an optimized set of angles for the specific material and structure in such a way that the etch rate of the horizontal surfaces and the sidewalls are equal or at least partly compensated, this way preserving at least some CDs

for the features undergoing processing, and at the same time enabling the sidewall roughness control and structural defects reduction for the features.

In some examples, the conformal deposition process may comprise depositing an amorphous or glass-like material on the structures. This may be advantageous for providing a smooth, stress-free, and continuous film on the sidewalls, which can further help to control the sidewall roughness and reduce structural defects.

In one example, the temperature used for the angled particle beam etching process may be lower than the temperature for the conformal deposition process. This may be advantageous for minimizing the thermal budget of the process and reducing the risk of thermal damage to the substrate and the features.

In some examples, the conformal deposition process may be performed at a pressure that is different from the pressure used for the angled particle beam etching process. This may be advantageous for optimizing the process conditions for each step and achieving the desired sidewall roughness control and structural defect reduction.

A5. Self-limiting reaction

In some examples, the method for sidewall roughness control and structural defect reduction may comprise a self-limiting reaction. A self-limiting reaction is a reaction that slows down or stops as a function of time or, equivalently, as a function of species dosage. Self-limiting reactions may include, but are not limited to chemisorption, deposition, conversion (e.g., oxidation, nitridation), and extraction. In the extraction case, the original material is a compound, with the modification removing one element preferentially from the surface, while the other element is removed in the subsequent removal step. In the case of chemisorption, a reaction on an exposed surface creates an electronic bond between the surface and the adsorbate.

A5.1. Use with ALE

In some examples, the self-limiting reaction may be used in combination with atomic layer etching (ALE). The self-limiting reaction may be applied during the ALE process to achieve a more controlled and precise etching process. The self-limiting reaction may be selective to specific materials or areas, allowing for a more targeted etching process. This can result in

improved sidewall roughness control and structural defect reduction, as well as better preservation of the original critical dimensions of the features.

A5.2. Use with ALD

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In some examples, the self-limiting reaction may be used in combination with atomic layer deposition (ALD). The self-limiting reaction may be applied during the ALD process to achieve a more controlled and precise deposition process. The self-limiting reaction may be selective to specific materials or areas, allowing for a more targeted deposition process. This can result in improved sidewall roughness control and structural defect reduction, as well as better preservation of the original critical dimensions of the features.

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A5.3. Independent step

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In some examples, the self-limiting reaction may be an independent step in the sidewall roughness control and structural defect reduction process. The self-limiting reaction may be applied independently of the angled particle beam etching or conformal deposition steps. This can provide additional flexibility in the process, allowing for further optimization of the sidewall roughness control and structural defect reduction.

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A6. Rapid Surface Temperature Cycling in Sidewall Roughness Control and Structural Defect Reduction

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In some examples, the method for sidewall roughness control and structural defect reduction may comprise one or a few additional steps of rapid surface temperature cycling. The rapid surface temperature cycling can be applied independently of all other steps and at any point in the process. This section describes the rapid surface temperature cycling process, its advantages, and its potential integration with other process steps.

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A6.1. Rapid Surface Temperature Cycling Process

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In some examples, rapid surface temperature cycling involves quickly changing the temperature of the substrate and the features thereon during the process. This can be achieved by various methods, such as using a substrate holder with integrated temperature control, applying external or cooling heating sources, such as flash lamps, or using a combination of both. The temperature cycling can be performed within a wide range of

temperatures, depending on the materials and process requirements. For example, the temperature range may be from -196°C to 500°C, with an accuracy of 2°C.

5 The rapid surface temperature cycling process may comprise a series of temperature ramps, plateaus, and cooling steps. The temperature ramps can be performed at different rates, depending on the desired process outcome. The temperature ramps typically range from a few °C/second to over 100°C/second. The plateaus may be maintained for a specific duration to allow for certain reactions or processes to occur. The cooling steps can also be performed at different rates, depending on the desired process outcome. The cooling step rates typically
10 range from a few °C/second to over 100°C/second.

A6.2. Integration with Other Process Steps

15 The rapid surface temperature cycling process may be integrated with other process steps in various ways. For example, it may be combined with angled particle beam etching, conformal deposition, self-limiting reactions, or any combination thereof. The rapid surface temperature cycling process may be performed before, during, or after any of these process steps, depending on the desired process outcome.

20 In some examples, the rapid surface temperature cycling process may be performed during the angled particle beam etching step, to enhance the etching process and improve sidewall roughness control and structural defect reduction. In other examples, the rapid surface temperature cycling process may be performed during the conformal deposition step, to enhance the deposition process and improve sidewall roughness control and structural defect
25 reduction. In yet other examples, the rapid surface temperature cycling process may be performed during the self-limiting reaction step, to enhance the reaction process and improve sidewall roughness control and structural defect reduction.

30 In some examples, the rapid surface temperature cycling process may be performed in an alternating manner with other process steps, such as angled particle beam etching, conformal deposition, or self-limiting reactions. This can provide additional process control and optimization, leading to improved sidewall roughness control and structural defect reduction.

35 B. Pattern improvement

B1. Method for Sidewall Roughness Reduction of Features on a Substrate

Figure 4 shows a schematic representation of the desired size and profile of the patterned features on a substrate 2100. The features are also referred to as structures and could be anything including micro- and nano-scale devices, waveguides or transistors. The features can be of various types, such as ridges, trenches, holes, pillars, and more, and can be made from a variety of materials, including semiconductors, metals, dielectrics, and polymers.

The features have field regions 2110 and sidewalls 2200. The desired or ideal profile of the features is smooth and uniform, with minimal roughness on the sidewalls. The field regions 2110 are defined here as regions with horizontal surfaces, i.e. surfaces which are parallel or close to parallel ($<20^\circ$ deviation) to the main surface of the substrate 2100 or coincide with the main surface of the substrate 2100. The field regions are shown as, for example, features 2110 in Figures 4 and 5.

However, due to Line Edge Roughness (LER), the actual profile is looking like Figure 5. Instead of the surfaces 2200 of the sidewalls in Figure 4, the sidewalls have surfaces 2210, which have features that make the profile slightly larger as compared to the desired profile. Figure 5 is thus an illustration of the real surface of the features before completing the method for sidewall roughness reduction, also known as Atomic Level Improvement, as described below. The sidewalls 2210 of the features exhibit roughness, which can negatively impact the performance of the features in their intended applications. The sidewall roughness is defined here as profile deviations from the sidewall tangent plane. The sidewall surface roughness is quantified as the root-mean-square (RMS) of the sidewall profile deviations from the sidewall tangent plane.

The method for sidewall roughness reduction comprises forming a patterned and selectively protecting masking layer so that at least part of the field regions 2110 are masked and the sidewalls 2210 are unmasked. This masking layer is thus designed to protect certain areas of the substrate during the etching process, while leaving other areas, specifically the sidewalls of the features, exposed, i.e. being subjected to the treatment. The method comprises performing dry etching in a process chamber enclosing the substrate 2100. The dry etching comprises creating a horizontal component of a direction of the etching by setting a pressure in the process chamber to exceed a defined pressure threshold for a sidewall etching. The horizontal component thus etches the unmasked sidewalls 2210 for said roughness reduction of the sidewalls 2210. Figure 5 illustrates a direction of the plasma ions which has a horizontal component, created by the high pressure dry etching. As the roughness of the sidewalls 2210 is reduced with the present method the line edge roughness will approach the ideal pattern as illustrated in Figure 4.

The method can be implemented in currently available equipment, and no need for significant change in the fabrication line is required, which makes this method a cost effective and sustainable approach. This is in contrast to previous solutions for roughness reduction which are more complex, such as relying on tilting of the substrate or particle beam to target the sidewalls with directional etching. This process is thus versatile and applicable to a wide range of materials, including polymers, semiconductors, dielectrics, and metals. As compared to some available methods this method has the advantage that it does not need any hardware modification to provide the inclined etching to attack the sidewalls. In addition, this method is applicable to all process steps of semiconductor manufacturing, making it a versatile approach compared to other counterparts.

Figures 6 and 7 show an implementation of the present method during a so-called Atomic level Pitch Splitting (APS). Any structure including a fin could be fabricated by first, forming a large structure, such as exemplified in Figure 6, and then using APS to divide it into 2 or several fins or any other smaller structures. Figure 6 shows a substrate (surface 2300) which could be any material including but not limited, metal, semiconductor, dielectric and polymer. The large structures are made any means of lithography and have field regions 2310 and sidewalls 2320.

Using APS and as shown in Figure 7, field region 2310 can be splitted in 2 or several parts forming new structures. An example of such a structure could be finFET. The new structure forms several surfaces such as 2411 as top surface and 2410 and 2420 as sidewalls. Sidewalls 2410 and 2420 could have roughness that makes the profile deviates from the desired size. To reduce this roughness, the top surface 2411 is covered with a mask and the sidewalls 2410 and 2420 are exposed to a low power plasma either in a continuous or cyclic scheme under high pressure to create the horizontal etching component to reduce the roughness. Figure 8 shows an example of a result after this method where all sidewalls (including 2410 and 2420) have significantly reduced roughness and reached the ideal size and profile which consequently improves device performance. Figure 8 accordingly illustrates the structure after APS and after completing the method for sidewall roughness reduction.

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B1.1. Protecting Masking Layer

The selective masking allows the etching process to specifically target the sidewalls of the features, which is where the roughness reduction is needed. In some examples, the protective mask is formed using selective deposition methods. These methods allow for the precise deposition of the masking material on the substrate, ensuring that only the desired areas are masked. The masking layer can be formed using any selective deposition methods, such as

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Chemical Vapor Deposition (CVD). Both methods allow for the deposition of thin, uniform layers of material on the substrate, but they differ in their mechanisms and the types of materials they can deposit.

- 5 The protecting masking layer can be made from a variety of materials, depending on the material of the features and the specific requirements of the etching process. The composition of the protecting masking layer can vary depending on the material of the features and the specific requirements of the etching process. The material used for the masking layer can be different from the material to be etched, which allows for better control over the etching process.
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B1.2. Substrate with Features

- 15 In some configurations, the substrate with features is the material on which the method for sidewall roughness reduction is performed. The substrate can be made from various materials, such as semiconductors, metals, dielectrics, and polymers. The features formed on the substrate can have various shapes, such as ridges, trenches, holes, pillars, and more. The features also have different aspect ratios, up to 1:10, and their sidewall roughness can be in the range of 0.5-5.0 nm RMS before the roughness reduction process.
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B1.3. High Pressure Dry Etching Process

- 25 In some implementations, the method for sidewall roughness reduction involves a high pressure dry etching process. This process is performed in a process chamber that encloses the substrate. The pressure in the chamber is set to exceed a defined pressure threshold for sidewall etching. This high pressure creates a horizontal component of the etching direction, which is responsible for etching the unmasked sidewalls of the features, thereby reducing their roughness.

30 B1.3.1. Setting the Pressure Threshold for Sidewall Etching

- 35 In some configurations, the pressure threshold for sidewall etching is a parameter in the high pressure dry etching process. This threshold is set to a value that allows for the creation of a horizontal component of the etching direction. In some examples, a pressure above 40 mTorr is particularly advantageous for this purpose. The pressure in the process chamber is carefully controlled and monitored to ensure that it remains above this threshold during the etching process.

B1.3.2. Impact of High Pressure on Ion Path and Etching Direction

5 In some examples, the high pressure in the process chamber has a significant impact on the path of the ions and the direction of the etching. The high pressure reduces the ions' mean free path, which results in a higher probability of collisions between the ions and the substrate. This, in turn, creates a horizontal component of the etching direction, which is responsible for etching the unmasked sidewalls of the features.

10 B1.3.3. Setting and Monitoring of Pressure Threshold

In some configurations, the setting and monitoring of the pressure threshold is a part of the high pressure dry etching process. The pressure in the process chamber is carefully controlled and monitored to ensure that it remains above the defined pressure threshold for sidewall etching. This ensures that the horizontal component of the etching direction is maintained, which is necessary for the reduction of the sidewall roughness.

B2.1. Reduction of Line Edge Roughness and Preservation of Critical Feature Dimensions

20 In some implementations, the sidewall etching process offers several benefits. Firstly, it reduces the line edge roughness of the features, which can improve the performance of the features in their intended applications. This roughness is defined as the profile deviations from the sidewall tangent plane. By reducing this roughness, the method improves the uniformity and smoothness of the features. In some examples, the line edge roughness can be reduced by at least 50%. In some examples, the line edge roughness can be reduced to a value below 1 nm RMS. The line edge roughness can be reduced to a value in the range 5-10 Angstrom (Å) RMS in some examples. Secondly, the sidewall etching process preserves the dimensions of the features, ensuring that the features retain their desired shape and size.

30 In some examples, another benefit of the sidewall etching process is the preservation of the dimensions of the features. Despite the etching of the sidewalls, the process does not significantly alter the overall size and shape of the features. This ensures that the features retain their desired dimensions, which is for their functionality.

35 B2.2. Low Energy Dry Etch Process

In some implementations, the method for sidewall roughness reduction involves a low energy dry etch process. This process is designed to etch the unmasked sidewalls of the features without significantly affecting the bulk of the material. The energy of the plasma used in the etching process can be set lower than the binding energy of the bulk of the material, which helps to preserve the dimensions of the features.

The low energy dry etching process can thus be self-limiting in some examples. This means that the etching process stops when the sidewall roughness is reduced below a certain threshold. This self-limiting nature of the etching process helps to prevent over-etching of the sidewalls, which could potentially damage the features or alter their dimensions.

B3. Post-Etching Processes

In some examples, after the high pressure dry etching process, further post-etching processes can be performed. These processes comprise rapid surface temperature cycling and self-limiting reaction processes. These processes are configured to further enhance the results of the etching process and to ensure the preservation of the dimensions of the features.

B3.1. Rapid Surface Temperature Cycling

In some examples, rapid surface temperature cycling is performed after the high pressure dry etching process. This process involves rapidly changing the temperature of the substrate surface, which can help to further reduce the roughness of the sidewalls. The rapid surface temperature cycling can be achieved through various methods, such as surface exposure to plasma or the use of a flashlight or a laser light source.

B3.2. Self-Limiting Reaction Processes

In some examples, the method for sidewall roughness reduction can involve self-limiting reactions. These processes involve reactions that are self-limiting, meaning they stop when a certain condition is met. These reactions can comprise chemisorption, deposition, extraction, oxidation, nitridation, or conversion. Self-limiting reaction processes can be performed during or after the high pressure dry etching process. These self-limiting reactions can further enhance the results of the etching process by providing additional control over the etching process.

In some examples, the etching or self-limiting reactions can be selectively applied to specific areas of the substrate. This selective application allows for the targeted reduction of sidewall roughness in specific areas, while preserving the dimensions of the features in other areas.

5 B4. Description of further Examples of the Disclosure

In one example, the method for sidewall roughness reduction can comprise the use of atomic layer etching, and particle beam etching selective to silicon oxide and silicon. The method can also comprise a cyclic etching process.

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B4.1. Use of Atomic Layer Etching

In some implementations, atomic layer etching (ALE) is used in the method for sidewall roughness reduction. Atomic layer etching (ALE) is defined as an etching technique that uses sequential half-reactions resulting in layer-by-layer material subtraction. The ALE implementation consists of at least two sequential steps: surface modification (reaction A) and removal (reaction B). These reactions can be cycled, and at least one step is at least partly self-limiting. The modification step forms a thin reactive surface layer with a well-defined thickness that is subsequently more easily removed than the unmodified material. The layer is characterized by a sharp gradient in chemical composition. Removal methods include thermal desorption, particle bombardment, and chemical reaction. ALE processes may also include quasi-atomic layer etching processes, which may include quasi-self-limiting reactions and non-self-limiting reactions. This provides a high level of control over the etching process, which can help to achieve a high level of roughness reduction.

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ALE is defined as an etching technique that uses sequential half-reactions resulting in layer-by-layer material subtraction. The ALE implementation consists of at least two sequential steps: surface modification (reaction A) and removal (reaction B). These reactions can be cycled, and at least one step is at least partly self-limiting. The modification step forms a thin reactive surface layer with a well-defined thickness that is subsequently more easily removed than the unmodified material. The layer is characterized by a sharp gradient in chemical composition. Removal methods include thermal desorption, particle bombardment, and chemical reaction. The above-described ALE method can comprise quasi-atomic layer etching processes, which may include quasi-self-limiting reactions and non-self-limiting reactions.

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B4.1.1. Particle Beam Etching Selective to Silicon Oxide and Silicon

In some configurations, particle beam etching selective to silicon oxide and silicon is used in the method for sidewall roughness reduction. This type of etching process involves the use of a particle beam that is selective to silicon oxide and silicon, meaning it preferentially etches these materials. This selectivity can help to preserve the dimensions of the features while
5 reducing the roughness of the sidewalls. In further examples, the etching is selective to a material comprising silicon nitride, hafnium oxide, and/or aluminium oxide.

B4.2. Cyclic Etching Process

10 In some examples, the method for sidewall roughness reduction comprises a cyclic etching process in which the material is removed in an atomic level in each cycle. Each cycle may thus remove a small amount of material from the sidewalls. This cyclic process can help to achieve a high level of control over the etching process, which can result in a high level of roughness reduction. The method can comprise rapidly changing the temperature of the substrate surface
15 between each etching cycle. This can help to further enhance the results of the etching process by providing additional control over the etching process.

Further, each of the etching cycles could have a step that could help lowering the binding energy of the surface atoms. The applied gas phase material reacts with the sidewall
20 and lowers the energy of its material so that a low energy plasma (another step in a cycle) can remove it. An example of such a process could be as following. A semiconductor, metal, dielectric or polymer surface is patterned by any type of lithography and then it moves to an ALD chamber where the top surface is covered with mask then it moves to another chamber, ICP-RIE, where it is exposed to a cyclic etching. The etching comprises a step in which
25 surfaces are exposed to a reactive gas such as Cl-gas. Excess Cl may be removed and a low power plasma, 10-20 eV may be applied to sputter away the roughness. The sputtering plasma could be a neutral gas like Ar or any other gases like SF₆ and C₄F₈. The chamber pressure may be 60 mTorr. As a result, the roughness can be significantly improved, such as a line edge roughness in the range 5-10 Angstrom (Å) to less than 1-10 Å.

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B5. Potential Applications

In one example, the method for sidewall roughness reduction can be applied in atomic level pitch splitting. This is a process where a larger structure on the substrate is divided into two or
35 more smaller structures. The method can also be used with various material types, including semiconductors, metals, dielectrics, and polymers.

B5.1. Application in Atomic Level Pitch Splitting

In some implementations, the method for sidewall roughness reduction can be used in atomic level pitch splitting (APS). This process involves dividing a larger structure on the substrate into two or more smaller structures. In some configurations, the use of the method for sidewall roughness reduction in atomic level pitch splitting can have a significant impact on the size and profile of the smaller structures. The method can help to reduce the roughness of the sidewalls of the smaller structures, which can result in smoother and more uniform structures. This can improve the performance of the structures in their intended applications.

B5.2. Application in Semiconductors, Metals, Dielectrics, and Polymers

In some configurations, the method for sidewall roughness reduction can be applied to features made from a variety of materials, including semiconductors, metals, dielectrics, and polymers. The method can help to reduce the roughness of the sidewalls of features made from these materials, which can improve their performance in their intended applications. The method can be adapted to suit the specific properties of each material type, ensuring that the roughness of the sidewalls is effectively reduced without damaging the material or altering its properties. This versatility makes the method suitable for use in a wide range of applications, from semiconductor manufacturing to the production of polymer-based devices.

B5.3. Impact on Different Feature Shapes

In some examples, the method for sidewall roughness reduction can be used on features of various shapes. These can include ridges, trenches, holes, pillars, and more. The method can be adapted to suit the specific shape of each feature, ensuring that the roughness of the sidewalls is effectively reduced without altering the shape of the feature. This flexibility makes the method suitable for use in a wide range of applications, from the production of complex semiconductor devices to the fabrication of intricate polymer-based structures. The method can be particularly beneficial in applications where the shape of the feature is to its performance, as it allows for the reduction of sidewall roughness without compromising the shape of the feature.

C. Cyclic Surface Conditioning Method

Figure 9 shows an example of the surface conditioning method based on cyclic processing. In Figure 9a, a substrate 3100 with an initial surface roughness 3110 is illustrated. The substrate

3100 can be made of various materials, such as semiconductor materials, metal materials, dielectric materials, or 2D materials. The surface of the substrate 3100 can be patterned or non-patterned.

- 5 In Figure 9b, the final surface is shown, where the substrate 3100 has a desired surface 3111 with reduced surface roughness while preserving the original thickness of the substrate 3100. This reduction in surface roughness is achieved through the cyclic processing method, which includes activating the surface, removing excess materials, applying a low-energy particle treatment, and repeating these steps until the desired smoothness is achieved. This surface
10 conditioning is achieved through the cyclic processing method as described earlier, which can involve any cyclic process, including atomic layer etching (ALE) or atomic layer deposition (ALD).

- Figure 10 shows another example of the surface conditioning method based on cyclic
15 processing. In Figure 10a, the initial structure 3110 with surfaces 3111, 3112, and 3122, which have roughness, is illustrated. In addition, substrate 3100 has another feature 3210, with a different height than 3110. The feature 3210 has different surfaces, 3211, 3212, and 3222 with roughness as illustrated.

- 20 In Figure 10b, the final structure is shown, with feature 3110 having the desired surfaces 3311, 3312, and 3322 and reduced surface roughness of features 3110 while preserving the original dimensions of the features 3110. Furthermore, Figure 10b shows feature 3210 with the desired surfaces 3411, 3412, and 3422 and reduced surface roughness of features 3210 while preserving the original critical dimensions of the features 3210. This surface conditioning is
25 achieved through the cyclic processing method as described earlier, which can involve any cyclic process, including atomic layer etching (ALE) or atomic layer deposition (ALD).

- Figure 11 shows another example of the surface conditioning method based on cyclic
30 processing. In Figure 11a, the initial structure 3110 with surfaces 3111, 3112, and 3122, which have roughness, is illustrated.

- In Figure 11b, the final structure is shown, with the desired surfaces 3222, 3212, and 3211 and reduced surface roughness of features 3110 while preserving the original critical dimensions of the features 3110. This surface conditioning is achieved through the cyclic processing
35 method as described earlier, which can involve any cyclic process, including atomic layer etching (ALE) or atomic layer deposition (ALD).

Figure 12 is a flowchart illustrating the method for surface conditioning based on cyclic processing according to an example of the present disclosure. The method includes activating the surface (step 3401), removing excess materials from the chamber (step 3402), applying a low-energy particle treatment to the surface (step 3403), and repeating the above steps until
5 the surface has the desired smoothness (step 3404). The low-energy particle treatment can be etching, deposition, or a combination of both. The method can also include ion beam shaping technology and angled particle beam etching.

Figure 13 shows atomic force microscopy (AFM) micrographs of the initial surface and a final
10 surface after the cyclic process according to an example. In Figure 13a, a micrograph of the scan area 3500 is shown, with an area of about $1 \mu\text{m}^2$. In the bottom graph, the roughness values 3501, 3502, and 3503 are measured in different places of the scan area, top, middle, and bottom, respectively. The roughness is measured to be around 0.11 nm.

15 In Figure 13b, results from AFM measurement of the final surface are shown. The top part, 3504, shows a micrograph of the scan area, where the area is about $1 \mu\text{m}^2$. In the bottom graph, the roughness values 3505, 5306, and 3507 are measured in different places of the scan area, top, middle, and bottom, respectively. The roughness is measured to be around 0.021 nm. This reduction in surface roughness is achieved through the cyclic processing
20 method as described earlier, which can involve any cyclic process, including atomic layer etching (ALE) or atomic layer deposition (ALD).

C1. Surface Activation Process

25 The surface activation process is a step in the surface conditioning method based on cyclic processing. In this process, the surface of a substrate is activated to facilitate the subsequent low-energy particle treatment, which can be etching, deposition, or a combination of both. The activation process can be performed using various techniques, such as gas exposure, chemical solution exposure, temperature-based activation, and particle beam activation. Each
30 of these techniques has its advantages and can be tailored to suit the specific requirements of the substrate material and the desired surface smoothness.

C1.1. Gas Exposure Activation

35 In some examples, the surface activation process may comprise exposing the surface to a gas or a mixture of gases. The gas exposure can modify the surface chemistry, making it more

susceptible to the low-energy particle treatment. The selection of appropriate gases is to achieve the desired surface activation and ensure compatibility with the substrate material.

C1.2. Chemical Solution Activation

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In some examples, the surface activation process may comprise exposing the surface to a chemical solution. The chemical solution can interact with the surface material, altering its properties and making it more amenable to the low-energy particle treatment. The selection of appropriate chemical solutions is crucial to achieve the desired surface activation and ensure compatibility with the substrate material.

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C1.3. Temperature-Based Activation

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In some examples, the surface activation process may comprise heating the surface to a specific temperature or within a specific temperature range. The temperature-based activation can cause thermal expansion or contraction of the surface material, leading to changes in the surface properties that can facilitate the low-energy particle treatment. The determination of the optimal temperature range is essential to achieve the desired surface activation and ensure compatibility with the substrate material.

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C1.3.1. Determining Optimal Temperature Range

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The optimal temperature range for the temperature-based activation process depends on the substrate material and the desired surface properties. In some examples, the temperature range may be selected to cause thermal expansion or contraction of the surface material, leading to changes in the surface roughness or other properties that can facilitate the low-energy particle treatment. In other examples, the temperature range may be selected to induce phase transitions or other structural changes in the surface material, which can alter its properties and make it more amenable to the low-energy particle treatment. The determination of the optimal temperature range can be based on factors such as the thermal properties of the substrate material, the desired surface properties, and the compatibility of the temperature range with the low-energy particle treatment process.

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C1.4. Particle Beam Activation

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In some examples, the surface activation process may comprise applying a particle beam to the surface. The choice of particle beams for the particle beam activation process depends on

the substrate material and the desired surface properties. In some examples, the particle beams may include ions, electrons, or neutral particles that can physically sputter or chemically react with the surface material to modify its properties. In other examples, the particle beams may include photons or other electromagnetic radiation that can induce electronic or vibrational excitations in the surface material, leading to changes in the surface properties that can facilitate the low-energy particle treatment. The selection of appropriate particle beams can be based on factors such as the reactivity of the particles with the substrate material, the desired surface properties, and the compatibility of the particle beams with the low-energy particle treatment process.

C2. Excess Material Removal Process

In one example, the excess material removal process is a step in the surface conditioning method based on cyclic processing. This process aims to remove any excess materials from the surface and the surrounding environment after the surface activation process. The removal of excess materials ensures that the subsequent low-energy particle treatment can be effectively applied to the surface without interference from unwanted materials. The excess material removal process may comprise various techniques, such as purging gases, pumping out gases, or a combination of pumping and purging.

C2.1. Purging Gases

In some examples, the excess material removal process may comprise purging gases. Purging gases involve introducing an inert gas, such as nitrogen or argon, into the processing chamber to displace and remove any excess materials, including reactive gases or byproducts from the surface activation process. The purging gas may be introduced at a controlled flow rate and pressure to ensure efficient removal of excess materials without causing damage to the surface or altering the surface properties. The use of purging gases in the excess material removal process offers the advantage of a simple and cost-effective technique for removing unwanted materials from the processing environment.

C2.2. Pumping Out Gases

In other examples, the excess material removal process may comprise pumping out gases. Pumping out gases involves using a vacuum pump to evacuate the processing chamber, thereby removing any excess materials, including reactive gases or byproducts from the surface activation process. The vacuum pump may be operated at a controlled pressure and

flow rate to ensure efficient removal of excess materials without causing damage to the surface or altering the surface properties. The use of pumping out gases in the excess material removal process offers the advantage of a more thorough removal of unwanted materials from the processing environment compared to purging gases alone.

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C2.3. Combination of Pumping and Purging

In some examples, the excess material removal process may comprise a combination of pumping and purging. This approach involves using both a vacuum pump to evacuate the processing chamber and an inert gas to displace and remove any excess materials, including reactive gases or byproducts from the surface activation process. The combination of pumping and purging may be performed in a sequential or simultaneous manner, depending on the specific requirements of the surface conditioning process. The use of a combination of pumping and purging in the excess material removal process offers the advantage of a more comprehensive removal of unwanted materials from the processing environment, ensuring that the subsequent low-energy particle treatment can be effectively applied to the surface without interference from excess materials.

The excess material removal process may be tailored to suit the specific requirements of the surface conditioning process, taking into account factors such as the type of surface being treated, the materials involved in the surface activation process, and the desired surface smoothness. By effectively removing excess materials from the surface and the surrounding environment, the excess material removal process plays a role in achieving the desired surface smoothness and ensuring the overall success of the surface conditioning method based on cyclic processing.

C3. Low-Energy Particle Treatment

In one example, the surface conditioning method based on cyclic processing includes a low-energy particle treatment step. This low-energy particle treatment can be applied to various types of surfaces, such as patterned and non-patterned surfaces, and can be used for different materials, including semiconductor surfaces, metal surfaces, dielectric surfaces, and 2D material surfaces. The low-energy particle treatment can be performed using a low-energy particle beam with a particle energy between 10 eV and 100 eV, or a low-energy plasma treatment with a plasma power between 1 W and 50 W.

C3.1. Low-Energy Particle Etching

In some examples, the low-energy particle treatment may comprise a low-energy particle etching process. This etching process can be used to selectively remove material from the surface, thereby reducing surface roughness and improving the overall surface quality. The
5 low-energy particle etching process can be performed using various techniques, such as ion beam etching, reactive ion etching, or plasma etching.

C3.1.1. Atomic Layer Etching (ALE) with Molecular Activation

10 In one example, the low-energy particle etching process may comprise atomic layer etching (ALE) with molecular activation. ALE with molecular activation is a highly controlled etching process that allows for the removal of material at the atomic level, resulting in a very smooth surface. This process involves the activation of the surface using a suitable activation method, such as gas exposure, chemical solution exposure, heating, or particle beam exposure,
15 followed by the application of a low-energy particle beam or plasma treatment to selectively remove material from the surface. The use of ALE with molecular activation can provide several advantages, such as improved control over the etching process, reduced surface roughness, and minimal damage to the underlying material.

20 C3.2. Low-Energy Particle Deposition

In some examples, the low-energy particle treatment may comprise a low-energy particle deposition process. This deposition process can be used to selectively deposit material onto the surface, thereby filling in any surface irregularities and improving the overall surface quality.
25 The low-energy particle deposition process can be performed using various techniques, such as atomic layer deposition (ALD), chemical vapor deposition (CVD), or physical vapor deposition (PVD).

C3.2.1. Atomic Layer Deposition (ALD)

30 In one example, the low-energy particle deposition process may comprise atomic layer deposition (ALD). ALD is a highly controlled deposition process that allows for the deposition of material at the atomic level, resulting in a very smooth surface. This process involves the sequential exposure of the surface to different precursor gases, which react with the surface
35 to form a thin layer of the desired material. The use of ALD can provide several advantages, such as improved control over the deposition process, reduced surface roughness, and the ability to deposit materials with high conformality and uniformity.

C3.3. Combination of Etching and Deposition

In some examples, the low-energy particle treatment may comprise a combination of etching and deposition processes. This can involve alternating between etching and deposition steps, or performing both etching and deposition simultaneously. The combination of etching and deposition can be used to selectively remove material from certain areas of the surface while depositing material in other areas, thereby reducing surface roughness and improving the overall surface quality.

C3.3.1. Alternating Etching and Deposition

In one example, the low-energy particle treatment may comprise alternating etching and deposition steps. This can involve performing an etching step to selectively remove material from the surface, followed by a deposition step to selectively deposit material onto the surface. By alternating between etching and deposition steps, the surface roughness can be reduced while maintaining the overall thickness of the material. This approach can provide several advantages, such as improved control over the surface conditioning process, reduced surface roughness, and the ability to selectively modify the surface without affecting the underlying material.

C4. Cyclic Processing and Surface Smoothness

In one example, the cyclic processing and surface smoothness section focuses on determining the desired surface smoothness, implementing a self-stopping cyclic process, and monitoring the reduction of surface roughness during the surface conditioning process. The cyclic processing method may comprise various optional features to achieve the desired surface smoothness and reduce surface roughness effectively.

C4.1. Determining Desired Surface Smoothness

In some examples, the desired surface smoothness is determined based on the specific application or requirements of the processed substrate. The surface smoothness may be quantified using various surface roughness parameters, such as root-mean-square (RMS) roughness, average roughness, or peak-to-valley roughness. The desired surface smoothness may be achieved by repeating the cyclic processing steps until the surface roughness

parameters reach the predetermined values or meet the specific requirements for the processed substrate.

C4.2. Self-Stopping Cyclic Process

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In one example, the cyclic processing method may comprise a self-stopping feature, where the process automatically stops when it has no further effect on the surface or when the surface roughness parameters reach a plateau. This self-stopping feature may be advantageous in preventing over-processing of the surface and preserving the original dimensions of the substrate or patterned features. The self-stopping cyclic process may be achieved by optimizing the process parameters, such as activation conditions, excess material removal methods, and low-energy particle treatment conditions, to ensure that the process has minimal or no impact on the surface once the desired smoothness is achieved.

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15 C4.3. Monitoring Surface Roughness Reduction

In some examples, the surface roughness reduction during the cyclic processing may be monitored using various in-situ or ex-situ metrology techniques. The in-situ metrology techniques may include optical monitoring, ellipsometry, or reflectometry, which can provide real-time feedback on the surface roughness parameters during the cyclic processing. The ex-situ metrology techniques may include atomic force microscopy (AFM), scanning electron microscopy (SEM), or transmission electron microscopy (TEM), which can provide high-resolution images and quantitative measurements of the surface roughness parameters after the cyclic processing.

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The monitoring of surface roughness reduction may be advantageous in determining the progress of the surface conditioning process and ensuring that the desired surface smoothness is achieved. Additionally, the monitoring may provide valuable information for optimizing the process parameters and improving the efficiency of the cyclic processing method.

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C5. Integration with Ion Beam Shaping Technology

In one example, the surface conditioning method based on cyclic processing can be integrated with ion beam shaping technology to further enhance the surface smoothing process. Ion beam shaping technology can be used to modify the surface topography by controlling the ion beam parameters, such as ion energy, ion species, ion incidence angle, and ion flux. This integration

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can provide additional control over the surface conditioning process, enabling more precise and efficient surface smoothing.

C5.1. Angled Particle Beam Etching

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In some examples, the integration of ion beam shaping technology with the surface conditioning method may comprise angled particle beam etching. Angled particle beam etching can be used to selectively remove material from specific areas of the surface, such as the peaks of surface roughness features, while preserving the valleys. This can result in a more uniform surface topography and reduced surface roughness.

In one example, the angled particle beam etching can be performed by directing an ion beam at an angle relative to the surface normal. The angle can be adjusted to optimize the etching process for the specific surface features and material properties. By controlling the ion beam parameters, such as ion energy, ion species, ion incidence angle, and ion flux, the etching process can be tailored to achieve the desired surface smoothing effect.

C5.2. Optimizing Ion Beam Parameters

In some examples, the ion beam parameters can be optimized to achieve the desired surface conditioning effect. The ion beam parameters can include ion energy, ion species, ion incidence angle, and ion flux. By adjusting these parameters, the ion beam shaping technology can be tailored to the specific surface features and material properties, resulting in more efficient and precise surface smoothing.

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In one example, the ion energy can be adjusted to control the penetration depth of the ions into the surface material. Higher ion energies can result in deeper penetration and more aggressive etching, while lower ion energies can result in shallower penetration and more gentle etching. The optimal ion energy can depend on the specific surface features and material properties, as well as the desired surface smoothing effect.

In another example, the ion species can be selected based on the chemical reactivity with the surface material. Some ion species may be more effective at etching certain materials, while others may be less effective or even cause unwanted side effects, such as surface damage or contamination. The optimal ion species can depend on the specific surface features and material properties, as well as the desired surface smoothing effect.

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In yet another example, the ion incidence angle can be adjusted to control the directionality of the etching process. By directing the ion beam at an angle relative to the surface normal, the etching process can be made more selective, preferentially removing material from specific areas of the surface, such as the peaks of surface roughness features. The optimal ion incidence angle can depend on the specific surface features and material properties, as well as the desired surface smoothing effect.

In still another example, the ion flux can be adjusted to control the etching rate and uniformity. Higher ion fluxes can result in faster etching and more aggressive surface smoothing, while lower ion fluxes can result in slower etching and more gentle surface smoothing. The optimal ion flux can depend on the specific surface features and material properties, as well as the desired surface smoothing effect.

By optimizing the ion beam parameters, the integration of ion beam shaping technology with the surface conditioning method based on cyclic processing can provide more precise and efficient surface smoothing, resulting in improved surface quality and reduced surface roughness. This integration can be particularly advantageous for applications requiring high-quality surfaces, such as semiconductor devices, optical components, and other advanced technologies.

C6. Surface Conditioning for Various Surface Types

The surface conditioning method based on cyclic processing can be applied to various surface types, including patterned surfaces and non-patterned surfaces, as well as surfaces made of different materials such as semiconductor materials, metal materials, dielectric materials, and 2D materials. The method can be tailored to address the specific requirements of each surface type and material, providing a versatile and efficient approach to surface conditioning.

C6.1. Patterned Surfaces

In some examples, the surface conditioning method can be applied to patterned surfaces, which may comprise features such as lines, dots, pillars, vias, grids, and other patterns. The method can be adapted to address the specific challenges associated with conditioning patterned surfaces, such as preserving the original dimensions of the features while reducing surface roughness.

C6.1.1. Side Wall Surfaces

In one example, the surface conditioning method can be applied to side wall surfaces of patterned features. The method can be tailored to address the specific challenges associated with conditioning side wall surfaces, such as maintaining the original dimensions of the features while reducing surface roughness. The cyclic processing method, including activation, removal of excess materials, and low-energy particle treatment, can be optimized to achieve the desired surface smoothness on side wall surfaces without affecting the overall dimensions of the patterned features.

10 C6.1.2. Inclined Surfaces

In some examples, the surface conditioning method can be applied to inclined surfaces of patterned features. The method can be adapted to address the specific challenges associated with conditioning inclined surfaces, such as maintaining the original dimensions of the features while reducing surface roughness. The cyclic processing method, including activation, removal of excess materials, and low-energy particle treatment, can be optimized to achieve the desired surface smoothness on inclined surfaces without affecting the overall dimensions of the patterned features.

20 C6.2. Non-Patterned Surfaces

In one example, the surface conditioning method can be applied to non-patterned surfaces, such as the surface of a substrate 3100. The method can be tailored to address the specific challenges associated with conditioning non-patterned surfaces, such as reducing surface roughness without affecting the overall thickness of the substrate. The cyclic processing method, including activation, removal of excess materials, and low-energy particle treatment, can be optimized to achieve the desired surface smoothness on non-patterned surfaces while preserving the original thickness of the substrate.

30 C6.3. Material-Specific Surface Conditioning

The surface conditioning method based on cyclic processing can be adapted to address the specific requirements of different materials, such as semiconductor materials, metal materials, dielectric materials, and 2D materials. In some examples, the activation process, removal of excess materials, and low-energy particle treatment can be tailored to the specific material properties and requirements, ensuring optimal surface conditioning results.

For example, the selection of appropriate gases, chemical solutions, temperature ranges, and particle beams for the activation process can be based on the specific material properties and requirements. Similarly, the selection of appropriate low-energy particle treatments, such as etching or deposition processes, can be tailored to the specific material properties and requirements.

By adapting the surface conditioning method to the specific material properties and requirements, the method can provide efficient and effective surface conditioning results for various surface types and materials, ensuring optimal performance and reliability of the conditioned surfaces.

D. Method for etching sidewalls of features

Figures 14A-B show cross-sectional views of a substrate at various intermediate stages of angled particle beam etching without any masking layer. Figure 14A illustrates a substrate 4100 with features 4110 having field regions 4111 and sidewalls 4112. The features 4110 are also referred to as structures 4110 in the present disclosure. Figure 14A shows the initial features 4110 at the very beginning of the processing, and Figure 14B shows the same features at the end of the processing, where the original features 4110 are transformed into features 4120 with reduced lateral dimensions and height. Figure 14B thus shows the substrate 4100 after angled particle beam etching, where both the width and the height of the features 4110 are reduced. The main goal of the processing performed on the features 4110 is to change their lateral dimensions, and the height changes are unwanted.

Figures 15A-C present cross-sectional views of a substrate at various intermediate stages of angled particle beam etching with a hard mask layer 4300 and the following removal of the masking layer and the unwanted structures 4131 which is residual material. Figures 15A-C demonstrate one known in-the-field solution for avoiding unwanted height reduction using a mask layer. Figure 15A shows the substrate 4100 with features 4110 and a hard mask layer 4300 at the beginning of the process. Figure 15B shows that the original features 4110 are transformed into features 4130 after the angled particle beam etching and that the original mask 4300 is transformed into masking layer 4310.

Usually, the masking layer is being etched less, or at least differently, than the material of features 4110, this is why artifact structures 4131 of residual material are formed in the case of using standard masking layers. These artifact structures 4131 are shown in Figure 15B right after the remaining masking layer 4310 and are caused by the masking effect of the

overhanging masking layer 4310. Usually, the masking layer is selectively removed after the processing. However, artifact structures 4131 may stay there after the masking layer removal and need to be removed separately. For instance, the artifact structures 4131 can be removed with an additional etch process, which will then transform the critical structures 4130 into structures 4140 with a reduced height, which is unwanted, as shown in Figure 15C. Alternatively, artifact structures 4131 may stay after the masking layer 4310 removal, and in this case, they are likely to distort or even fail the final devices that are being manufactured with the help of the processing. Figure 15C thus shows the substrate 4100 after the removal of the hard mask layer 4300 and the unwanted structure 4131, leaving features 4130 with reduced height compared to the original height of the features 4110.

Figures 16A-C are a schematic illustration of a method according to the present disclosure for etching sidewalls 4112 of features 4110 on a substrate 4100. Cross-sectional views of the substrate 4100 at various intermediate stages of angled particle beam etching are shown with a compound masking layer comprising a first masking layer 4400 and a second masking layer 4300 over the first masking layer 4400. The method comprises providing the compound masking layer on the features 4110, whereby at least part of the field regions 4111 is masked and the sidewalls 4112 are unmasked by the compound masking layer. Figure 16A shows the substrate 4100 with features 4110, the first masking layer 4400, and the second masking layer 4300.

The method comprises etching the sidewalls 4112, whereby the second masking layer 4300 prevents etching of the first masking layer 4400. Figure 16B illustrates the substrate 4100 after angled particle beam etching 4200, where the second masking layer (denoted 4310 after the etching) prevents etching of the first masking layer, thereby maintaining the height (h_1) of the features and the first masking layer (denoted 4130 and 4410, respectively, after the etching), with respect to the substrate 4100.

The method comprises removing the first masking layer 4410, whereby any remaining part of the second masking layer 4310 is removed. Figure 16C shows the substrate 4100 after the removal of the compound masking layer, leaving features (denoted 4130 after the compound masking layer removal) with their original intended height (h_2), which corresponds to the height of the features 4110 in Figure 16A. The compound masking layer thus prevents height reduction of the features 4110 during sidewall etching such as during ion beam etching at a tilted angle.

Any residual material 4411 after the sidewall etching is separated from the features 4130 by the first masking layer 4410. The residual material 4411 is instead attached to the first masking layer 4410 and/or the second masking layer 4310, see Figure 16B. As further seen in Figure 16B the first masking layer 4410 may separate the features 4130 from the residual material 4411 so that the features 4130 have an essentially uninterrupted vertical sidewall with respect to the substrate 4100. The removal of the first masking layer 4410 will also remove any remaining part of the second masking layer 4310 as well as the residual material 4411. The features 4130 will thus be left on the substrate 4100 with their original intended height (h_2), while the lateral dimension has been reduced by the sidewall etching, see Figure 16C.

In some examples it is conceivable that the second masking layer 4300 prevents etching of the first masking layer 4400 but that the first masking layer 4400 may still be etched a relatively small amount with respect to its original thickness. A height (h_1) of the features 4110, 4130 and the first masking layer 4400, 4410, with respect to the substrate 4100 is in such case essentially maintained and in some examples only affected a few percent after the sidewall etching. The first masking layer 4410 will in such case still separate any residual material 4411 from the features 4130, and allow the subsequent removal of the compound masking layer and the residual material 4411 so that the original height (h_2) of the features 4110, 4130, is maintained after the sidewall etching. The second masking layer 4300 preventing etching of the first masking layer 4400 should thus be construed as essentially preventing the etching of the first masking layer 4400 or as reducing or substantially reducing the etching of the first masking layer 4400, while providing the advantageous benefits as described where the features 4110, 4130, maintain their original height (h_2) after the sidewall etching. In some examples the etching of the first masking layer 4400 is reduced by at least a factor of two by the second masking layer 4300.

In one example the second masking layer 4300 is made of Chromium, or SiO_2 , or Al_2O_3 , and the first masking layer 4400 is made of amorphous Si, and the features 4110 are made of crystalline Si. The masking layers 4300, 4400, the substrate 4100, and the features 4110 may be made of semiconductors, dielectrics, metals, and two-dimensional (2D) materials like graphene or transition-metal dichalcogenide monolayers.

Figures 17A-C are a schematic illustration of a further example of the method according to the present disclosure for etching sidewalls 4112 of features 4110 on a substrate 4100. The compound masking layer may comprise a third masking layer 4500. Cross-sectional views of the substrate 4100 at various intermediate stages of angled particle beam etching 4200 are shown with a compound masking layer comprising a third masking layer 4500, the first masking

layer 4400, and the second masking layer 4300. The third masking layer 4500 is arranged between the features 4110 and the first masking layer 4400, see Figure 17A. The material of the first masking layer 4400 is typically the same as the material of the features 4110, but in cases where it is difficult to find an appropriate material for the first masking layer 4400 it is advantageous to have a third masking layer 4500.

The material of the third masking layer 4500 is different from the material of the features 4110 in this example. The thickness of the third masking layer may be thinner than the first masking layer, and in some examples less than 10 nm. Figure 17B illustrates the substrate 4100 after angled particle beam etching, where the third masking layer 4500 separates the features 4130 from residual material 4411 after the sidewall etching. The features 4130 may accordingly have an essentially uninterrupted vertical sidewall with respect to the substrate 4100. The etch rate of sidewalls 4501 of the third masking layer 4500 corresponds at least to the etch rate of the sidewalls 4112 of the features 4110. Selective removal of the third masking layer, denoted 4510 in Figure 17B, results in removal of the entire compound masking layer after the sidewall etching, which leaves the features 4130 with the originally intended height, see Figure 17C.

The third masking layer 4500 is so thin that its etch properties significantly differ when processing the exposed material on the sides, which makes it, due to the small thickness of the material, effectively as soft, or even softer than the material of the sidewalls of the critical structure 4130 and this material is selected in such way that the whole masking layer can be easily removed later without attacking the critical structure as it is remaining after the processing.

In one example the second masking layer 4300 is made of Chromium, or SiO_2 , or Al_2O_3 , and the first masking layer 4400 is made of amorphous Si, or crystalline Si, or polycrystalline Si, and the third masking layer 4500 is made of SiO_2 , and the features 4110 are made of the same material as the first masking layer 4400.

In another example the second masking layer 4300 is made of Chromium, or SiO_2 , or Al_2O_3 , and the first masking layer 4400 is made of amorphous Si, or crystalline Si, or polycrystalline Si, and the third masking layer 4500 is made of graphene, and the features 4110 are made of the same material as the first masking layer 4400.

The masking layers 4300, 4400, 4500, the substrate 4100, and the features 4110 may be made of semiconductors, dielectrics, metals, and two-dimensional (2D) materials like

graphene or transition-metal dichalcogenide monolayers. It may be especially advantageous to have the third masking layer 4500 made of 2D materials.

Further examples of the method for etching sidewalls of features are described in the following.

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The method for etching sidewalls of features on a substrate involves a series of steps that are designed to maintain the height of the features while reducing their lateral dimensions. This is achieved through the use of a compound masking layer that is applied to the features on the substrate. The compound masking layer protects the features during the etching process, preventing unwanted height reduction. The operational process involves providing the compound masking layer on the features, etching the sidewalls of the features, and then removing the first masking layer.

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D1. Compound masking layer, sidewall etching and compound masking layer removal

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In one example of the disclosure, the etching method involves the use of two masking layers as a compound masking layer, as described above in relation to Figures 16A-C. The compound masking layer is provided on the features on the substrate. This compound masking layer comprises a first masking layer and a second masking layer. The compound masking layer is designed to mask at least part of the field regions of the features, leaving the sidewalls unmasked.

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In one configuration, the first masking layer is provided on the features on the substrate. This layer is configured to have the same etch properties as the features on the substrate. This means that the first masking layer and the features on the substrate can be removed at the same rate during the sidewall etching process. The material of the first masking layer is the same as the material of the features in one example. The first masking layer can also be selectively removed after the sidewall etching process.

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In some examples, the first masking layer separates the features on the substrate from any residual material that may be left after the sidewall etching process. This residual material is instead attached to the first masking layer and/or the second masking layer. This separation allows the features to have an essentially uninterrupted vertical sidewall with respect to the substrate after the sidewall etching process.

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The second masking layer is provided over the first masking layer. This second masking layer is designed to prevent the etching of the first masking layer during the sidewall etching process.

The etch rate of the second masking layer may be lower than that of the first masking layer, which helps to protect the first masking layer during the etching process. The second masking layer can also be selectively removed after the sidewall etching process.

5 In some configurations, the etching method involves the use of three masking layers, as described above in relation to Figures 17A-C. A third masking layer may be provided between the features and the first masking layer. The third masking layer may thus be applied directly to the features on the substrate. The first masking layer is applied over the third masking layer, and the second masking layer is applied over the first masking layer.

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This third masking layer is typically thinner than the first masking layer and is made of a different material from the features. The etch rate of the third masking layer corresponds at least to the etch rate of the sidewalls of the features. The third masking layer separates the features from any residual material that may be left after the sidewall etching process. This
15 allows the features to have an essentially uninterrupted vertical sidewall with respect to the substrate after the sidewall etching process. The third masking layer can also be selectively removed after the sidewall etching process, resulting in the removal of the entire compound masking layer as well as in the removal of any residual material.

20 In some configurations, the method for etching sidewalls of features on a substrate involves a series of steps that are designed to maintain the height of the features while reducing their lateral dimensions. This is achieved through the use of a compound masking layer that is applied to the features on the substrate. The compound masking layer is designed to protect the features during the etching process, preventing unwanted height reduction. The method
25 involves providing the compound masking layer on the features, etching the sidewalls of the features, and then removing the first masking layer.

In one configuration, the process of sidewall etching involves directing an etching agent at the sidewalls of the features. The compound masking layer protects the features during this
30 process, preventing unwanted height reduction. After the sidewall etching process, the first masking layer is removed. This also removes any remaining part of the second masking layer and any residual material that may be left after the sidewall etching process. The features are thus left on the substrate with their original intended height.

35 D2. Potential Applications

The method for etching sidewalls of features on a substrate has potential applications in various fields, including semiconductor manufacturing and microfabrication.

D2.1. Applications in Semiconductor Manufacturing

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In some examples, the method can be used in the manufacturing of semiconductors. The method allows for the etching of the sidewalls of features on a substrate without affecting the height of the features. This is particularly useful in the manufacturing of semiconductors, where it is often necessary to reduce the lateral dimensions of features without reducing their height.

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In one use case, the method can be used in the manufacturing of semiconductor devices such as transistors. The method allows for the etching of the sidewalls of the transistor gate without affecting the height of the gate. This can help to improve the performance of the transistor by reducing the gate length without reducing the gate height.

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D2.2. Applications in Microfabrication

In some examples, the method can be used in microfabrication processes. The method allows for the etching of the sidewalls of features on a substrate without affecting the height of the features. This can be particularly useful in microfabrication processes, where it is often necessary to create features with precise dimensions. In one use case, the method can be used in the fabrication of microelectromechanical systems (MEMS). The method allows for the etching of the sidewalls of features on a substrate without affecting the height of the features. This can be particularly useful in the fabrication of MEMS devices, where it is often necessary to create features with precise dimensions. For example, the method can be used in the fabrication of MEMS accelerometers, where the sidewalls of the accelerometer's sensing elements need to be etched without affecting their height.

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In another use case, the method can be used in the fabrication of microfluidic devices. The method allows for the etching of the sidewalls of channels in a microfluidic device without affecting the height of the channels. This can be particularly useful in the fabrication of microfluidic devices, where it is often necessary to create channels with precise dimensions. For example, the method can be used in the fabrication of microfluidic devices for lab-on-a-chip applications, where the sidewalls of the microfluidic channels need to be etched without affecting their height.

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In yet another use case, the method can be used in the fabrication of optical devices. The method allows for the etching of the sidewalls of optical waveguides without affecting the height

of the waveguides. This can be particularly useful in the fabrication of optical devices, where it is often necessary to create waveguides with precise dimensions. For example, the method can be used in the fabrication of integrated optical devices, where the sidewalls of the optical waveguides need to be etched without affecting their height.

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In summary, the method for etching sidewalls of features on a substrate has potential applications in various fields, including semiconductor manufacturing and microfabrication. The method allows for the etching of the sidewalls of features on a substrate without affecting the height of the features. This can be particularly useful in applications where it is necessary to create features with precise dimensions. The method comprises providing a compound masking layer on the features, etching the sidewalls of the features, and then removing the first masking layer. The compound masking layer comprises a first masking layer and a second masking layer, and optionally a third masking layer. The first masking layer is applied directly to the features, while the second masking layer is applied over the first masking layer. The third masking layer, if used, is provided between the features and the first masking layer. After the sidewall etching process, the first masking layer is removed. This also removes any remaining part of the second masking layer and any residual material that may be left after the sidewall etching process. The features are thus left on the substrate with their original intended height.

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The terminology used herein is for the purpose of describing particular aspects only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, actions, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, actions, steps, operations, elements, components, and/or groups thereof.

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It will be understood that, although the terms first, second, etc., may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element without departing from the scope of the present disclosure.

Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element to another element as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element, or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

It is to be understood that the present disclosure is not limited to the aspects described above and illustrated in the drawings; rather, the skilled person will recognize that many changes and modifications may be made within the scope of the present disclosure and appended claims. In the drawings and specification, there have been disclosed aspects for purposes of illustration only and not for purposes of limitation, the scope of the disclosure being set forth in the following claims.

Claims

1. A method for sidewall roughness control and structural defect reduction of features on a substrate, comprising:
adjusting the tilt angle of a particle beam for angled particle beam etching of at least one sidewall of the features.
2. The method of claim 1 further comprising a combination of conformal deposition and variable tilt angle etching to achieve the sidewall roughness control and structural defect reduction.
3. The method of claim 2, further comprising alternating deposition and etching steps to achieve the sidewall roughness control and structural defect reduction.
4. The method of any preceding claim further comprising a self-limiting reaction, such as chemisorption, deposition, extraction, oxidation, nitridation, or conversion.
5. The method of any preceding claim, wherein the particle beam comprises neutrals, radicals, photons, ions, electrons, or a combination thereof.
6. The method of any preceding claim, wherein the tilt angle of the particle beam ranges from 0-85 degrees from the angle of the normal of the substrate.
7. The method of any preceding claim, wherein the sidewall roughness control results in line edge roughness (LER) reduction of at least 50%.
8. The method of any preceding claim, wherein the sidewall roughness control and structural defect reduction comprise adjusting the tilt angle of the particle beam during angled etching or self-limiting reaction, or a combination thereof.
9. The method of claim 8, wherein the deposition or etching or self-limiting reactions or their combination are selectively applied to specific areas.
10. The method of any preceding claim, wherein the deposition is with atomic layer deposition (ALD).
11. The method of any preceding claim, wherein the features and particle beam are rotated with respect to each other during the angled etching.

12. The method of any preceding claim, wherein the sidewall roughness control results in sidewall roughness reduction.
13. The method of any previous claim, wherein the angled etching is performed using atomic layer etching (ALE).
14. The method of any previous claim, wherein the etch process is selective to silicon.
15. The method of claim 14, wherein the etch process is selective to silicon oxide.
16. The method of any previous claim, wherein the particle beam tilt can also be 0 degrees from the angle of the normal to the substrate, and therefore the process can be performed without adjusting the tilt angle of a particle beam during particle beam etching.
17. The method of any previous claim, wherein the deposited material is amorphous or glass-like.
18. The method of any previous claim, wherein the beam particles have a lower atomic mass than at least one of the components of the exposed surface.
19. The method of any previous claim, wherein the process further includes rapid surface temperature cycling.
20. The method of any previous claim, wherein the deposited material is the same as the material being etched.
21. A method for sidewall roughness reduction of features on a substrate, the features being spaced apart and having respective field regions and sidewalls, the method comprising
 - forming a patterned and selectively protecting masking layer so that at least part of the field regions are masked and the sidewalls are unmasked,
 - performing dry etching in a process chamber enclosing the substrate, comprising creating a horizontal component of a direction of the etching by setting a pressure in the process chamber to exceed a defined pressure threshold for a sidewall etching, whereby the horizontal component etches the unmasked sidewalls for said roughness reduction of the sidewalls.

22. The method according to claim 21, wherein the defined pressure threshold for sidewall etching is 40 mTorr.
23. The method according to claim 21 or 22, wherein the dry etching is self-limiting, whereby the dry etching stops when the sidewall roughness is reduced with a threshold amount.
24. The method according to any of claims 21 to 23, wherein the sidewall roughness is reduced by at least 50%.
25. The method according to any of claims 21 to 24, wherein a line edge roughness of the sidewalls is reduced to a value below 1 nm RMS.
26. The method according to any of claims 21 to 25, further comprising a self-limiting reaction such as chemisorption, deposition, extraction, oxidation, nitridation, or conversion.
27. The method according to claim 26, wherein the self-limiting reaction or dry etching is selectively applied to specific areas of the substrate.
28. The method according to any of claims 21 - 27, wherein the dry etching is a cyclic etching process.
29. The method according to any of claims 21 - 28, wherein the dry etching is performed using atomic layer etching (ALE).
30. The method according to any of claims 21 to 29, wherein the dry etching is selective to a material comprising any of silicon, silicon oxide, silicon nitride, hafnium oxide, aluminium oxide.
31. The method according to any of claims 21 to 30, further comprising rapid surface temperature cycling.
32. The method according to claim 31, wherein the rapid surface temperature cycling is done through surface exposure to plasma.
33. The method according to claim 31, wherein the rapid surface temperature cycling is assisted with flashlight.

34. The method according to claim 33, wherein the rapid surface temperature cycling assisted with flashlight is done using a laser light source.
35. The method according to any of claims 21 to 34, wherein the features on the substrate comprise any of micro- and nano-scale devices, waveguides, transistors, ridges, trenches, holes, and/or pillars.
36. A method for surface conditioning based on cyclic processing comprising:
activating a surface;
removing excess materials from the surface and surrounding environment;
applying a low-energy particle treatment to the surface; and
repeating the above steps until the surface has a desired smoothness.
37. The method according to claim 36, wherein the low-energy particle treatment uses ions.
38. The method according to claim 37, wherein the low-energy particle treatment is atomic layer etching (ALE).
39. The method according to claim 38, wherein the low-energy particle treatment is atomic layer etching (ALE) with molecular activation.
40. The method according to claim 36, wherein the cyclic processing comprises deposition steps.
41. The method according to claim 40, wherein the deposition steps result in an atomic layer deposition (ALD).
42. The method according to any one of claims 37 to 41, comprising a combination of etching and deposition.
43. The method according to any one of claims 37 to 42, comprising alternating etching and deposition.
44. The method according to any one of claims 36 to 43, wherein the repeating of the steps is performed until the process has no further effect on different processed surfaces.

45. The method according to any one of claims 36 to 44, further comprising ion beam shaping technology.
46. The method according to claim 45, further comprising angled particle beam etching.
47. The method according to any one of claims 36 to 46, wherein the surface is a side wall surface.
48. The method according to any one of claims 36 to 47, wherein the surface is an inclined surface.
49. The method according to any one of claims 36 to 48, wherein the surface is selected from the group consisting of semiconductor surfaces, metal surfaces, dielectric surfaces, and 2D material surfaces.
50. The method according to any one of claims 36 to 49, wherein the surface is a patterned surface.
51. The method according to any one of claims 36 to 50, wherein the surface is a non-patterned surface.
52. The method according to any one of claims 36 to 51, wherein the activation of the surface comprises applying a gas exposure to the surface.
53. The method according to any one of claims 36 to 52, wherein the activation of the surface comprises exposing the surface to a chemical solution.
54. The method according to any one of claims 36 to 53, wherein the activation of the surface comprises heating the surface to a specific temperature.
55. The method according to any one of claims 36 to 54, wherein the activation of the surface comprises applying a particle beam to the surface.
56. The method according to any preceding claim, wherein the low-energy particle treatment comprises a low-energy particle beam with a particle energy between 10 eV and 100 eV.

57. The method according to any one of claims 36 to 55, wherein the low-energy particle treatment comprises a low-energy plasma treatment with a plasma power between 1 W and 50 W.

58. A surface conditioned by the method according to any one of claims 36 to 57.

59. A method for etching sidewalls of features (4110) on a substrate (44100), the features being spaced apart and having respective field regions (4111) and sidewalls (4112), the method comprising

providing a compound masking layer on the features comprising a first masking layer (4400) and a second masking layer (4300) over the first masking layer, whereby at least part of the field regions is masked and the sidewalls are unmasked by the compound masking layer, the method further comprising

etching the sidewalls, whereby the second masking layer prevents etching of the first masking layer so that a height (h_1) of the features and the first masking layer with respect to the substrate is maintained, and

removing the first masking layer, whereby any remaining part of the second masking layer is removed.

60. Method according to claim 59, wherein the first masking layer has the same etch properties as the features on the substrate, whereby etching of the sidewalls (4112) of the features removes material of sidewalls (4401) of the first masking layer at least at the same rate as for the material of the features.

61. Method according to claim 59 or 60, wherein the second masking layer is formed of a material with a lower etch rate than the material of the first masking layer.

62. Method according to any of claims 59 - 61, wherein the first masking layer is selectively removed after etching of the sidewalls, whereby a height (h_2) of the features after the sidewall etching is the same as before the sidewall etching.

63. Method according to any of claims 59 - 62, wherein the first masking layer separates the features from residual material (4411) after the etching of the sidewalls.

64. Method according to claim 63, wherein the residual material is attached to the first and/or second masking layer and is thereby removed with the removal of the first masking layer.

65. Method according to claim 63 or 64, wherein the first masking layer separates the features from the residual material so that the features have an essentially uninterrupted vertical sidewall with respect to the substrate.

66. Method according to any of claims 59 - 65, wherein the compound masking layer comprises a third masking layer (4500), whereby the third masking layer is arranged between the features and the first masking layer, and wherein the material of the third masking layer is different from the material of the features.

67. Method according to claim 66, wherein the thickness of the third masking layer is less than the thickness of the first masking layer.

68. Method according to claim 66 or 67, wherein the thickness of the third masking layer is less than 10 nm.

69. Method according to any of claims 66 - 68, wherein an etch rate of sidewalls (4501) of the third masking layer corresponds at least to an etch rate of the sidewalls (4112) of the features (4110), upon said etching of the sidewalls of the features (4110).

70. Method according to any of claims 66 - 69, wherein the material of the first masking layer is the same as the material of the features.

71. Method according to any of claims 66 - 70, wherein the method comprises removing the third masking layer whereby the first masking layer and any remaining part of the second masking layer is removed.

72. Method according to any of claims 66 - 71, wherein the third masking layer separates the features from residual material after the etching of the sidewalls so that the features have an essentially uninterrupted vertical sidewall with respect to the substrate.

73. Method according to claim 72, wherein the third masking layer separates the first masking layer from the features so that the features and the third masking layer have an essentially uninterrupted vertical sidewall with respect to the substrate after the sidewall etching.