Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a substrate;

forming a conductive layer over the substrate;

forming a first insulating layer over the substrate and conductive layer;

removing a portion of the first insulating layer to expose the conductive layer and form a plurality of first micro-openings in the first insulating layer over the conductive layer; and

forming an interconnect structure over the conductive layer.providing a semiconductor die;

forming a first insulating layer over the semiconductor die;

forming a conductive layer over the first insulating layer;

forming a second insulating layer over the first insulating layer and conductive layer;

removing a portion of the second insulating layer to expose the conductive layer and form a plurality of first micro-vias partially through the second insulating layer over the conductive layer; and

forming a bump over the conductive layer, wherein the first micro-vias provide stress relief.

2. The method of claim 1, further including forming a second insulating layer over the substrate prior to forming the conductive layer.

~~3. The method of claim 2, further including:~~

~~forming a plurality of second micro-openings in the second insulating layer; and~~

~~forming the conductive layer over the second micro-openings.~~

~~4~~2. The method of claim 1, wherein removing the portion of the ~~first~~ second insulating layer leaves an island of the ~~first~~ second insulating layer over the conductive layer.

~~5~~3. The method of claim 1, further including forming a ~~second~~ third insulating layer in the first micro-~~openings~~vias over the ~~interconnect structure~~bump.

~~6. A method of making a semiconductor device, comprising:~~

~~providing a substrate;~~

~~forming a conductive layer over the substrate;~~

~~forming a first insulating layer having a plurality of first micro openings over the substrate and conductive layer; and~~

~~forming an interconnect structure over the conductive layer.~~

~~7. The method of claim 6, further including forming a second insulating layer over the substrate.~~

~~8~~4. The method of claim ~~7~~1, further including:

forming a plurality of second micro-~~openings~~vias in the ~~second~~first insulating layer; and

forming the conductive layer over the second micro-~~openings~~vias.

5. The method of claim 1, wherein a number of the first micro-vias in the second insulating layer ranges from 16 to 32.

~~9. The method of claim 6, further including forming an island of the first insulating layer over the conductive layer.~~

~~10. The method of claim 6, wherein the interconnect structure includes a bump.~~

~~11~~6. A method of making a semiconductor device, comprising:

providing a substrate;

forming a conductive layer ~~formed~~ over the substrate;

forming a first insulating layer ~~having a plurality of first micro-openings formed~~ over the substrate and conductive layer; ~~and~~

removing a portion of the first insulating layer to expose a portion of the conductive layer and form a plurality of first micro-openings partially through the first insulation layer around the exposed portion of the conductive layer; and

forming an interconnect structure ~~formed~~ over the conductive layer.

~~12~~7. The ~~semiconductor device~~ method of claim ~~11~~6, further including forming a second insulating layer ~~formed~~ over the substrate prior to forming the conductive layer.

8. The method of claim 7, further including:

forming a plurality of second micro-openings in the second insulating layer; and

forming the conductive layer over the second micro-openings.

~~13~~9. The ~~semiconductor device~~ method of claim ~~11~~6, wherein removing the portion of the first insulating layer leaves ~~further including~~ an island of the first insulating layer over the conductive layer.

1~~4~~0. The ~~semiconductor device~~method of claim ~~11~~6, further including ~~a~~ forming a second insulating layer formed in the first micro-openings over the interconnect structure.

151. The ~~semiconductor device~~ method of claim ~~11~~6, wherein the first micro-openings include micro-vias, micro-via rings, or micro-via slots.

12. The method of claim 6, wherein a width of the first micro-openings in the first insulating layer ranges from 0.5 to 10 micrometers.

13. The method of claim 6, wherein the interconnect structure includes a bump.

14. A method of making a semiconductor device, comprising:

providing a substrate;

forming a conductive layer over the substrate;

forming a first insulating layer including a plurality of first micro-openings partially through the first insulating layer and over the conductive layer; and

forming an interconnect structure over the conductive layer.

15. The method of claim 14, further including forming a second insulating layer over the substrate.

16. The method of claim 15, further including:

forming a plurality of second micro-openings in the second insulating layer; and

forming the conductive layer over the second micro-openings.

17. The method of claim 14, further including forming an island of the first insulating layer over the conductive layer.

18. The method of claim 14, further including forming a second insulating layer in the first micro-openings over the interconnect structure.

19. The method of claim 14, wherein the first micro-openings include micro-vias, micro-via rings, or micro-via slots.

20. The method of claim 14, wherein the interconnect structure includes a bump.

21. A method of making a semiconductor device, comprising:

providing a substrate;

forming a conductive layer over the substrate; and

forming a first insulating layer over the substrate and conductive layer and including a plurality of first micro-openings partially through the first insulating layer.

22. The method of claim 21, further including forming a second insulating layer over the substrate.

23. The method of claim 22, further including:

forming a plurality of second micro-openings in the second insulating layer; and

forming the conductive layer over the second micro-openings.

24. The method of claim 21, wherein the first micro-openings include micro-vias, micro-via rings, or micro-via slots.

25. The method of claim 21, further including forming a bump over the conductive layer.