FIG. 1

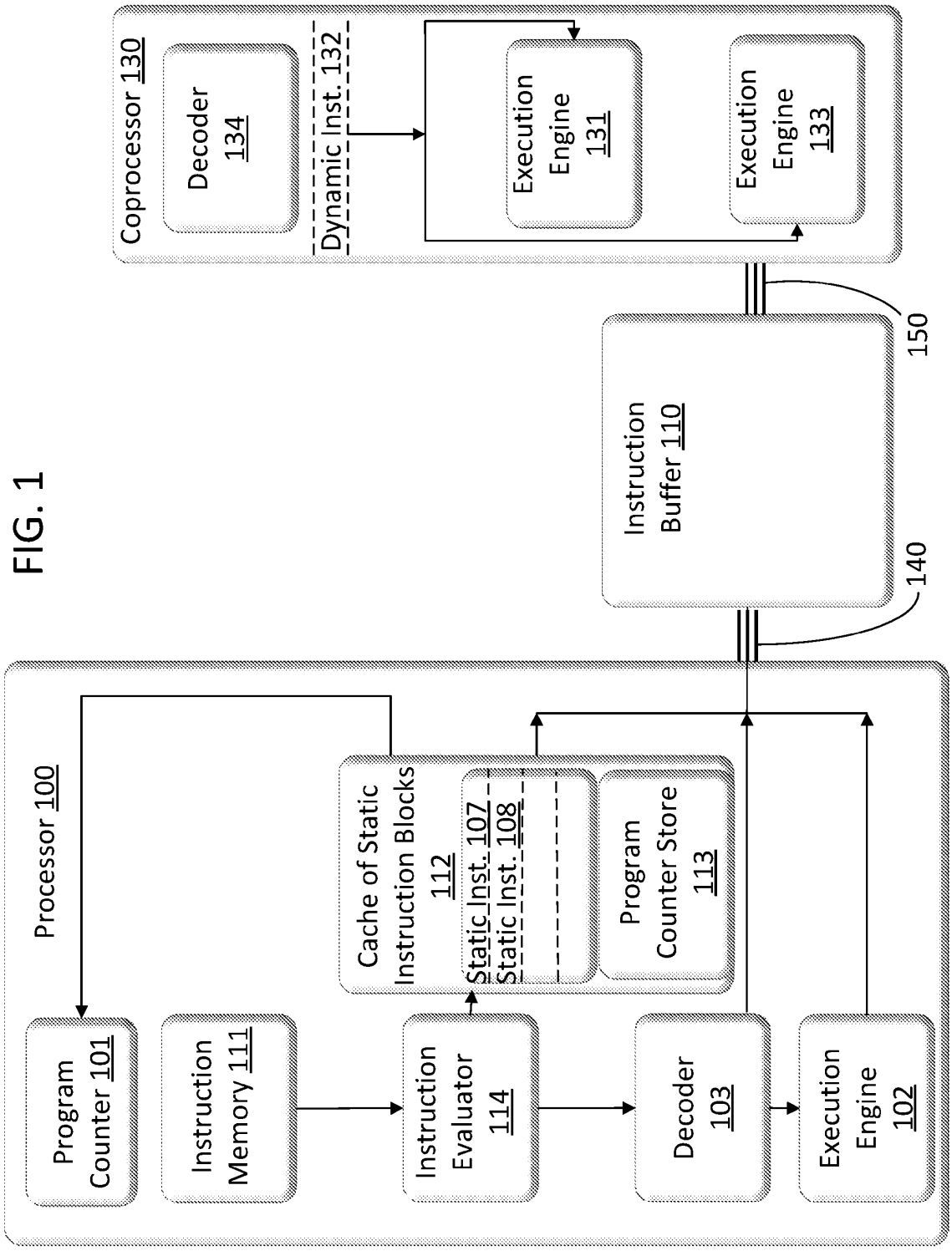

Coprocessor 130
Decoder 134
Dynamic Inst. 132
Execution Engine 131
Execution Engine 133
150
Instruction Buffer 110
140
Processor 100
Cache of Static Instruction Blocks 112
Static Inst. 107
Static Inst. 108
Program Counter Store 113
Program Counter 101
Instruction Memory 111
Instruction Evaluator 114
Decoder 103
Execution Engine 102

FIG. 2

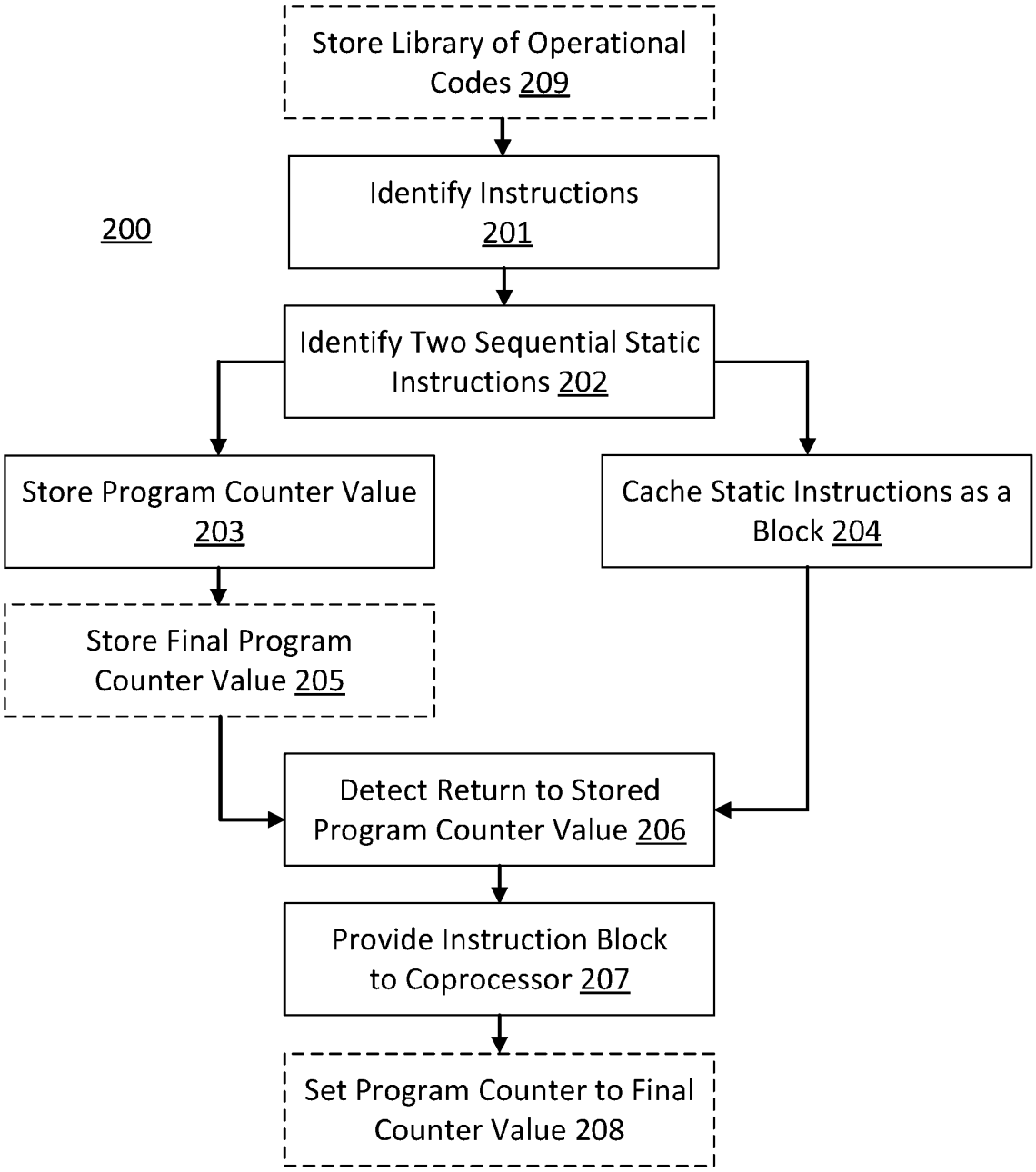
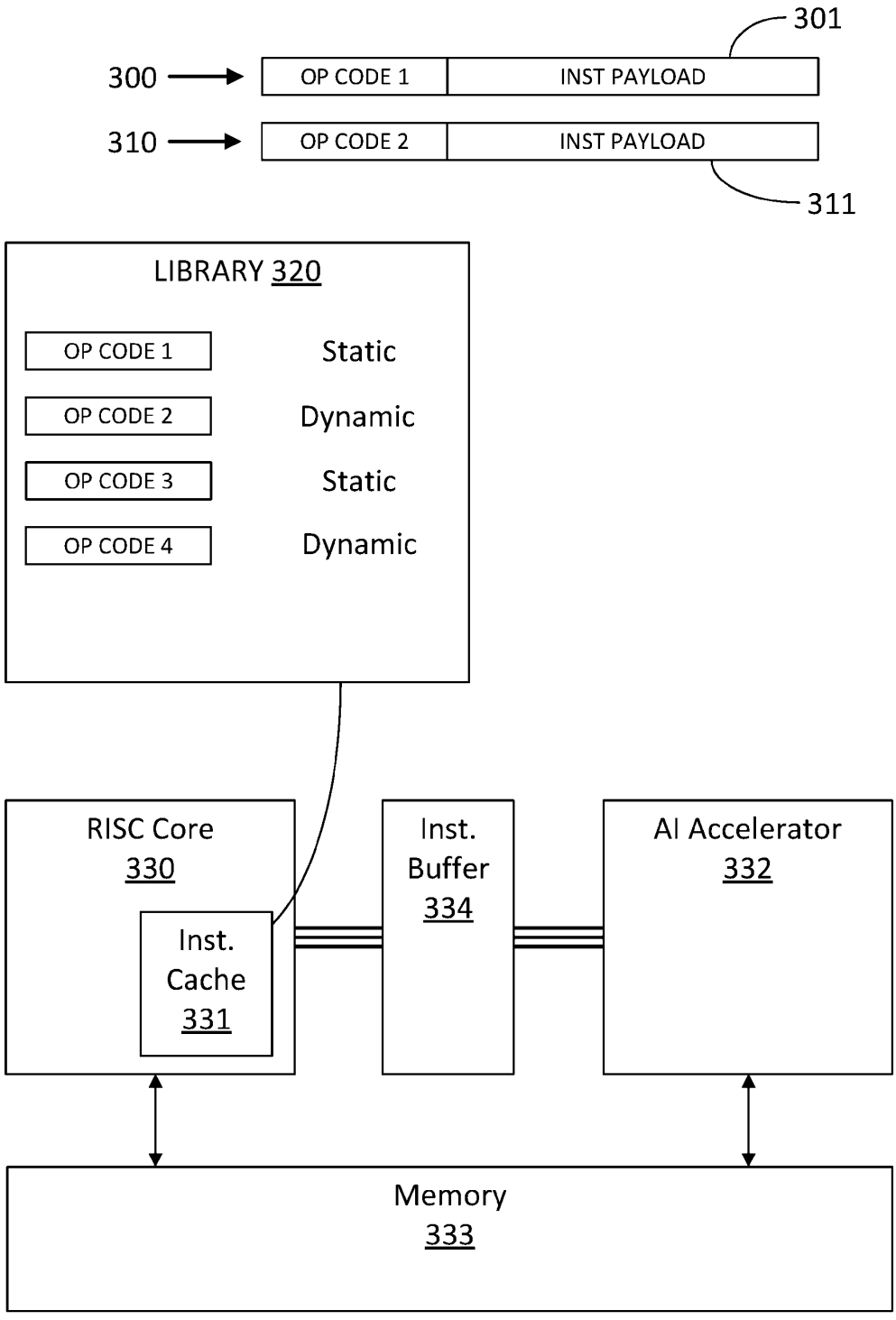

Store Library of Operational Codes 209
200
Identify Instructions 201
Identify Two Sequential Static Instructions 202
Store Program Counter Value 203
Cache Static Instructions as a Block 204
Store Final Program Counter Value 205
Detect Return to Stored Program Counter Value 206
Provide Instruction Block to Coprocessor 207
Set Program Counter to Final Counter Value 208

FIG. 3


301
300
OP CODE 1
INST PAYLOAD
310
OP CODE 2
INST PAYLOAD
311
LIBRARY 320
OP CODE 1
Static
OP CODE 2
Dynamic
OP CODE 3
Static
OP CODE 4
Dynamic
RISC Core
330
Inst.
Cache
331
Inst.
Buffer
334
AI Accelerator
332
Memory
333