A STRAINED CHANNEL TRANSISTOR AND METHOD OF FABRICATION THEREOF

Abstract

The present invention relates to semiconductor integrated circuits. More particularly, but not exclusively, the invention relates to strained channel complimentary metal oxide semiconductor (CMOS) transistor structures and fabrication methods thereof. A strained channel CMOS transistor structure (200) comprises a source stressor region (225) comprising a source extension stressor region (225A); and a drain stressor region (226) comprising a drain extension stressor region (226A); wherein a strained channel region (229) is formed between the source extension stessor region (225A) and the drain extension stressor region (226A), a width of said channel region (229) being defined by adjacent ends (225B, 226B) of said extension stressor regions (225A, 226A).

Fig. 2L

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