ABSTRACT OF THE DISCLOSURE

SILICIDE FORMATION FOR eSiGe USING SPACER OVERLAPPING eSiGe AND SILICON CHANNEL INTERFACE AND RELATED PFET

Methods of forming a silicide in an embedded silicon germanium (eSiGe) source/drain region using a silicide prevention spacer overlapping an interface between the eSiGe and the silicon channel, and a related PFET with an eSiGe source/drain region and a compressive stress liner in close proximity to a silicon channel thereof, are disclosed. In one embodiment, a method includes providing a gate having a nitrogen-containing spacer adjacent thereto and an epitaxially grown silicon germanium (eSiGe) region adjacent to a silicon channel of the gate; removing the nitrogen-containing spacer that does not extend over the interface between the eSiGe source/drain region and the silicon channel; forming a single silicide prevention spacer about the gate, the single silicide prevention spacer overlapping the interface; and forming the silicide in the eSiGe source/drain region using the single silicide prevention spacer to prevent the silicide from forming in at least an extension area of the silicon channel.

Fig 6