FIG. 1

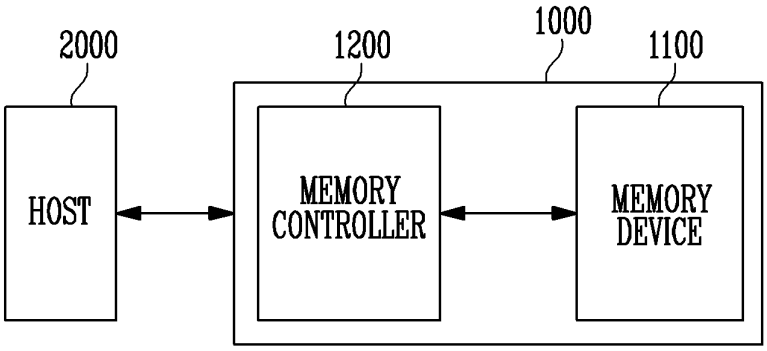


FIG. 2

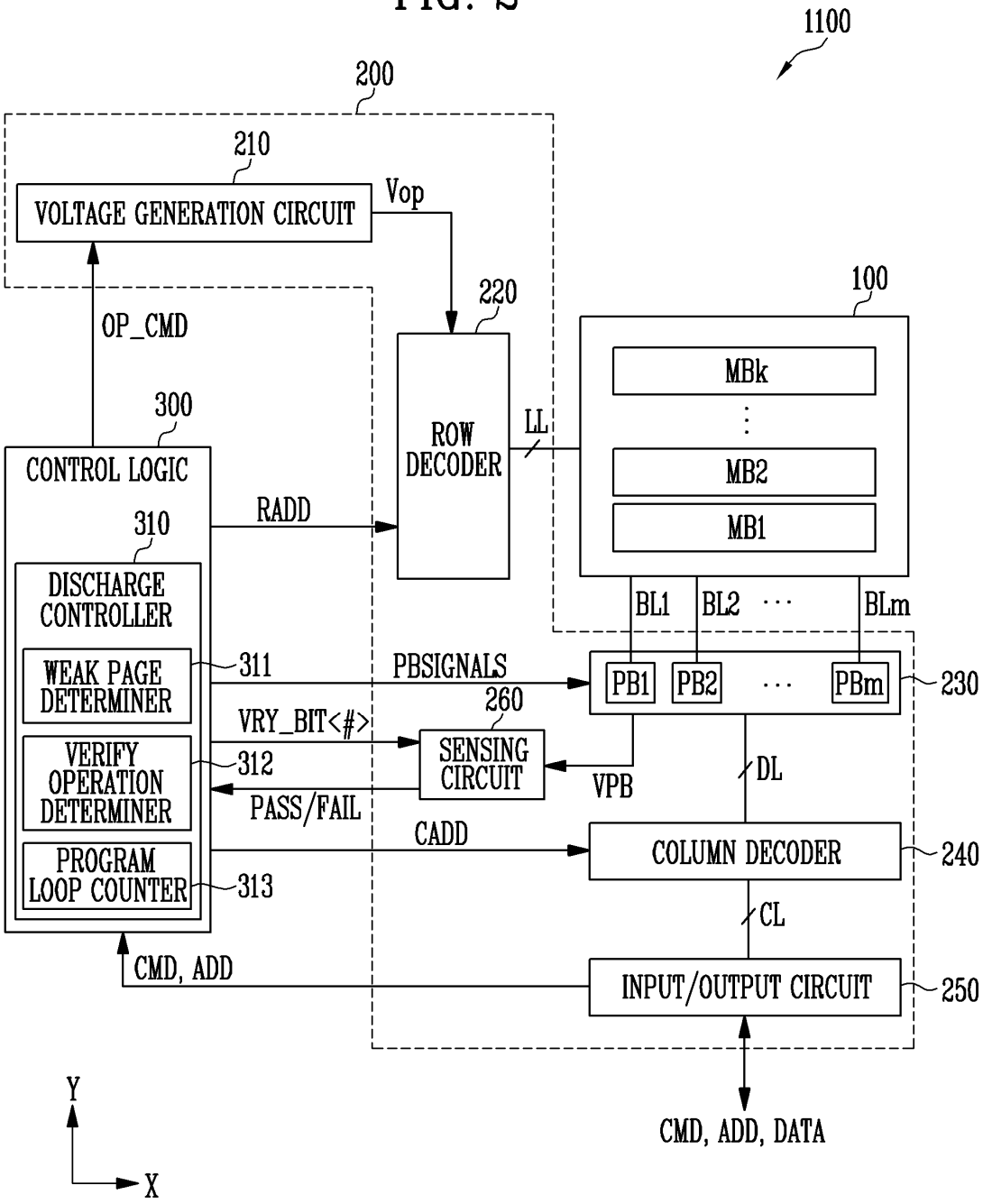

1100
200
210
VOLTAGE GENERATION CIRCUIT
Vop
220
100
OP_CMD
300
ROW DECODER
LL
MBk
MB2
MB1
CONTROL LOGIC
RADD
310
DISCHARGE CONTROLLER
BL1
BL2
BLm
WEAK PAGE DETERMINER
311
PBSIGNALS
PB1
PB2
PBm
230
260
VRY_BIT<#>
VERIFY OPERATION DETERMINER
312
SENSING CIRCUIT
VPB
DL
PASS/FAIL
CADD
COLUMN DECODER
240
PROGRAM LOOP COUNTER
313
CL
CMD, ADD
INPUT/OUTPUT CIRCUIT
250
CMD, ADD, DATA
Y
X

FIG. 3

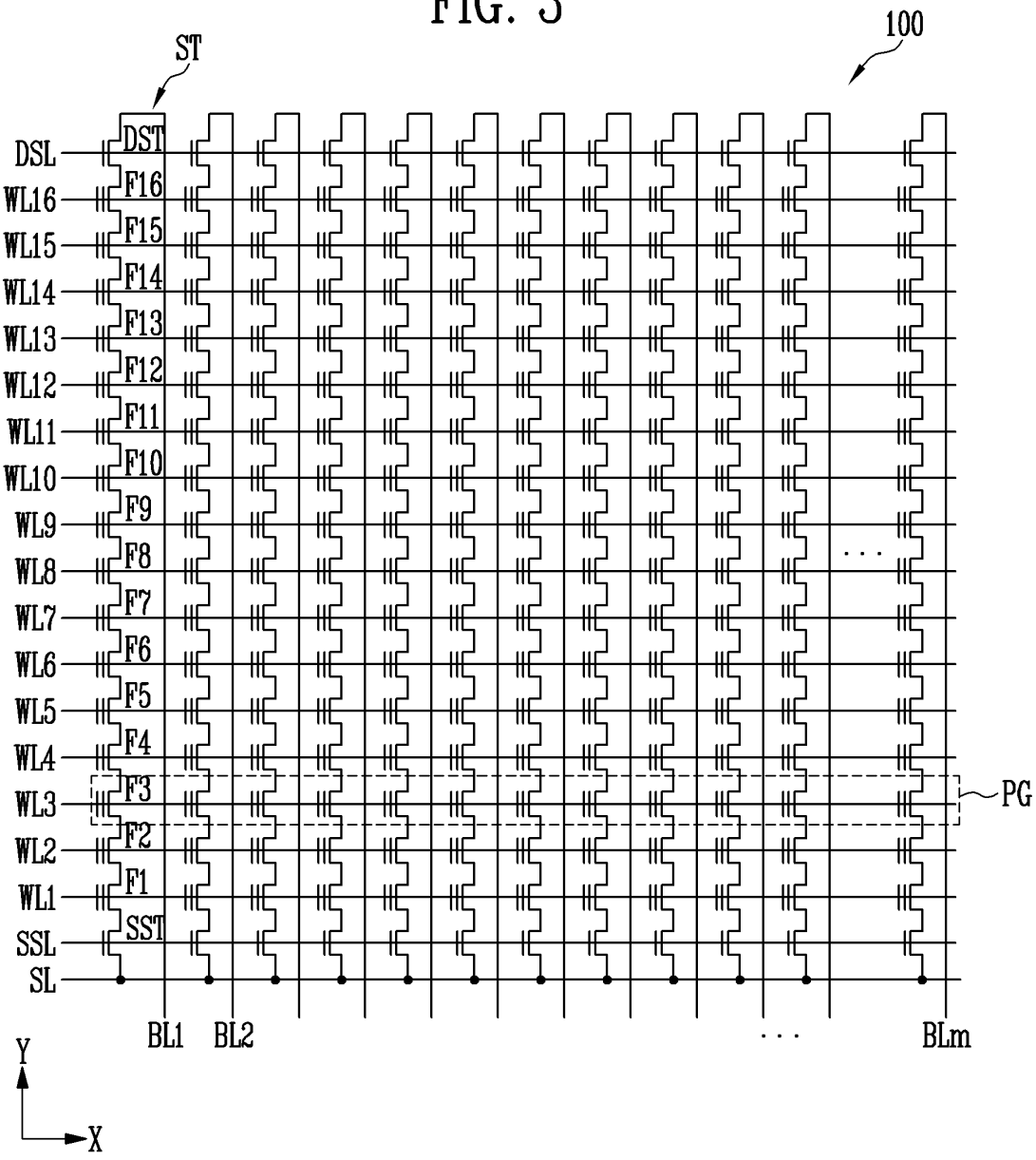

100
ST
DST
F16
F15
F14
F13
F12
F11
F10
F9
F8
F7
F6
F5
F4
F3
F2
F1
SST
DSL
WL16
WL15
WL14
WL13
WL12
WL11
WL10
WL9
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
SSL
SL
PG
BL1
BL2
BLm
Y
X

FIG. 4

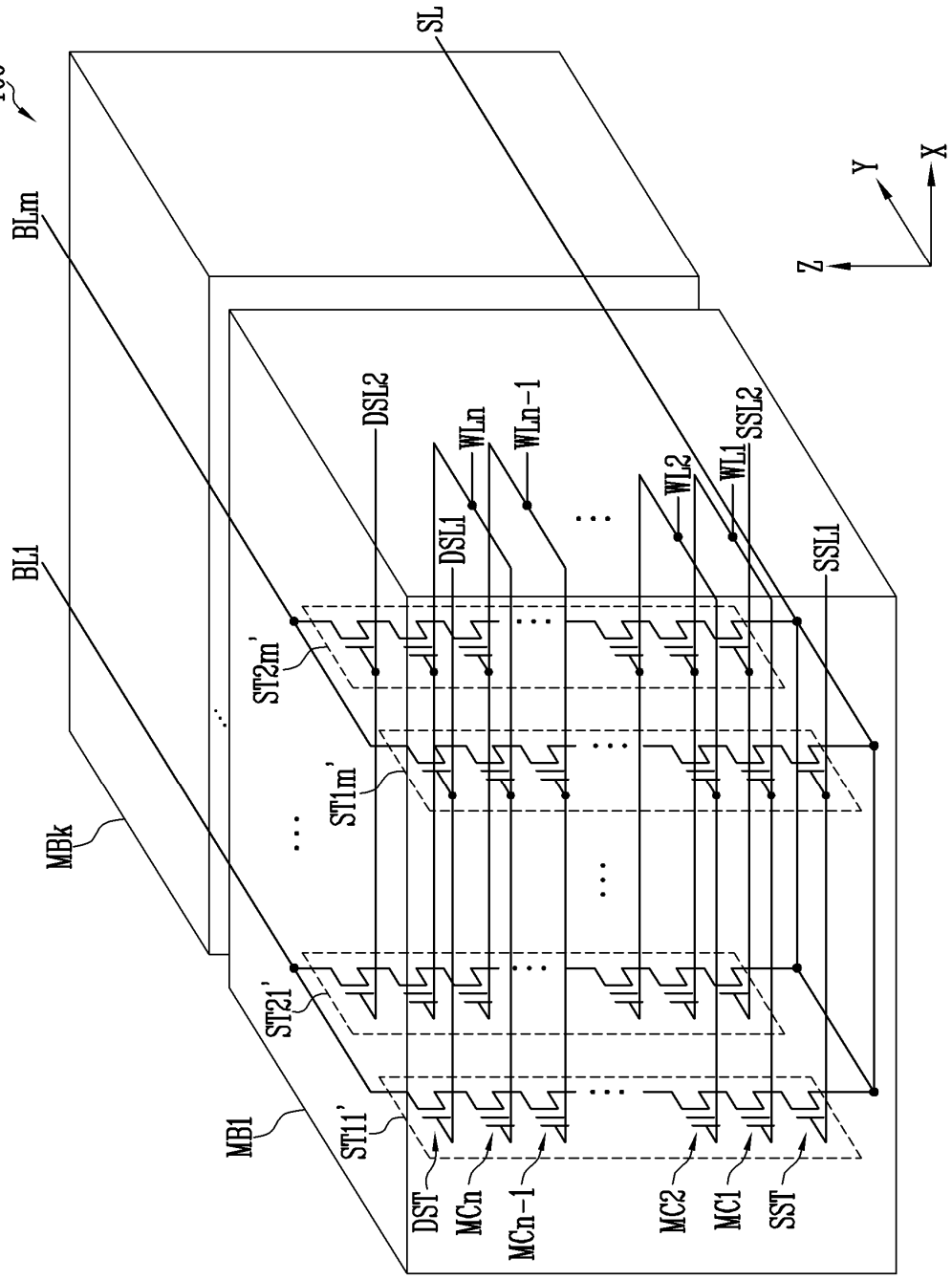

100
SL
BLm
BL1
MBk
MB1
DSL2
DSL1
WLn
WLn-1
WL2
WL1
SSL2
SSL1
ST2m'
ST1m'
ST21'
ST11'
DST
MCn
MCn-1
MC2
MC1
SST
Y
X
Z

FIG. 5

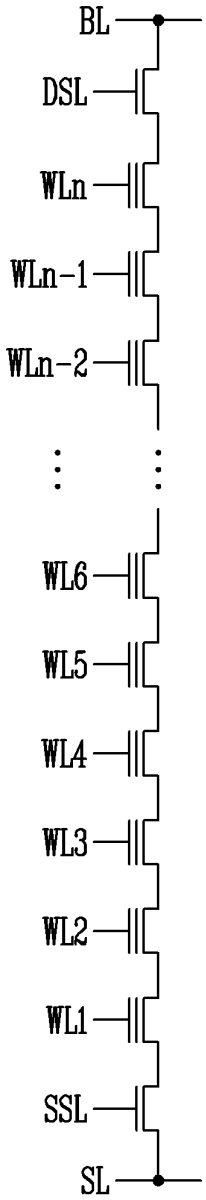

BL
DSL
WLn
WLn-1
WLn-2
WL6
WL5
WL4
WL3
WL2
WL1
SSL
SL

FIG. 6

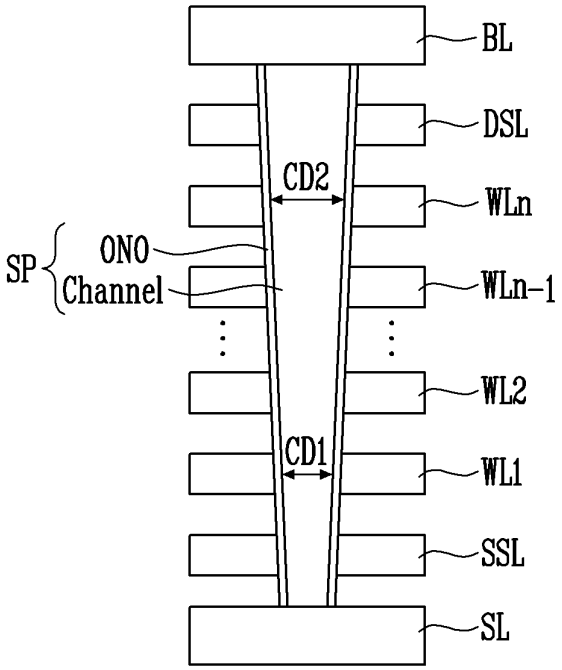

BL
DSL
CD2
WLn
SP
ONO
Channel
WLn-1
WL2
CD1
WL1
SSL
SL

FIG. 7

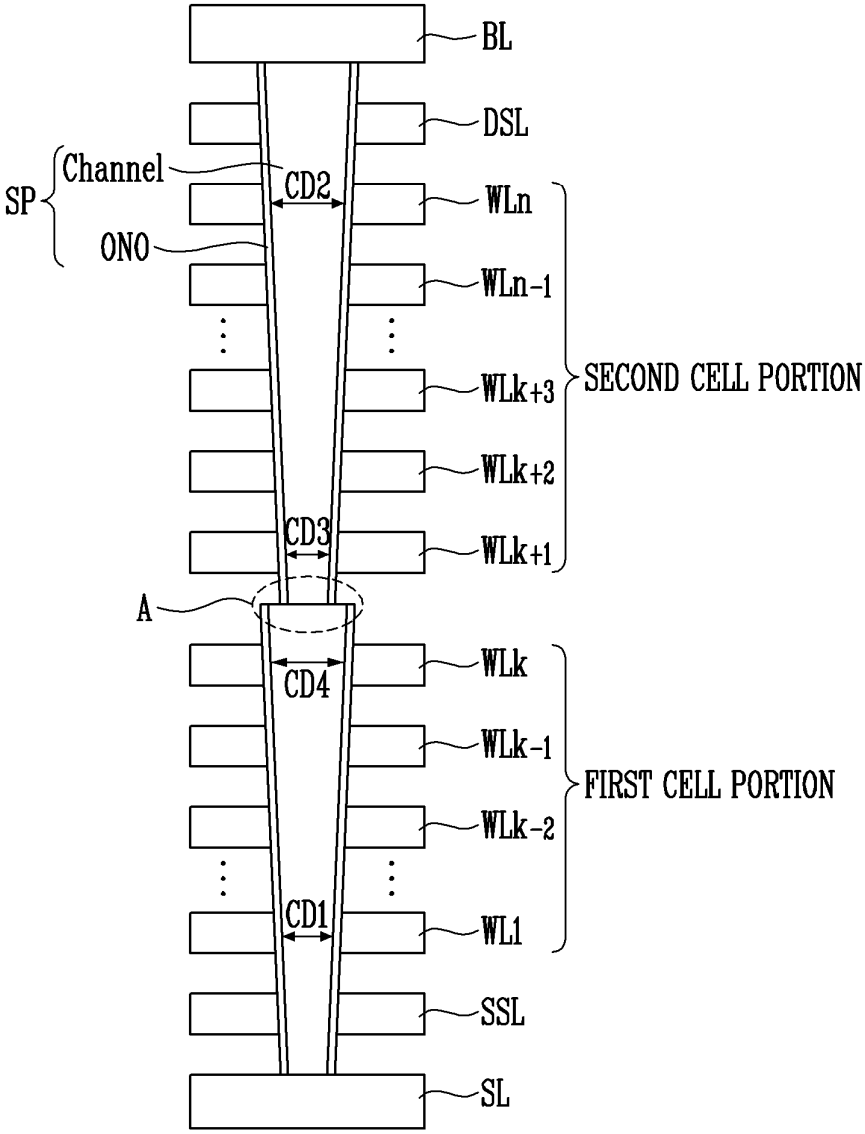

BL
DSL
SP
Channel
ONO
CD2
WLn
WLn-1
WLk+3
WLk+2
WLk+1
SECOND CELL PORTION
CD3
A
CD4
WLk
WLk-1
WLk-2
FIRST CELL PORTION
CD1
WL1
SSL
SL

FIG. 8

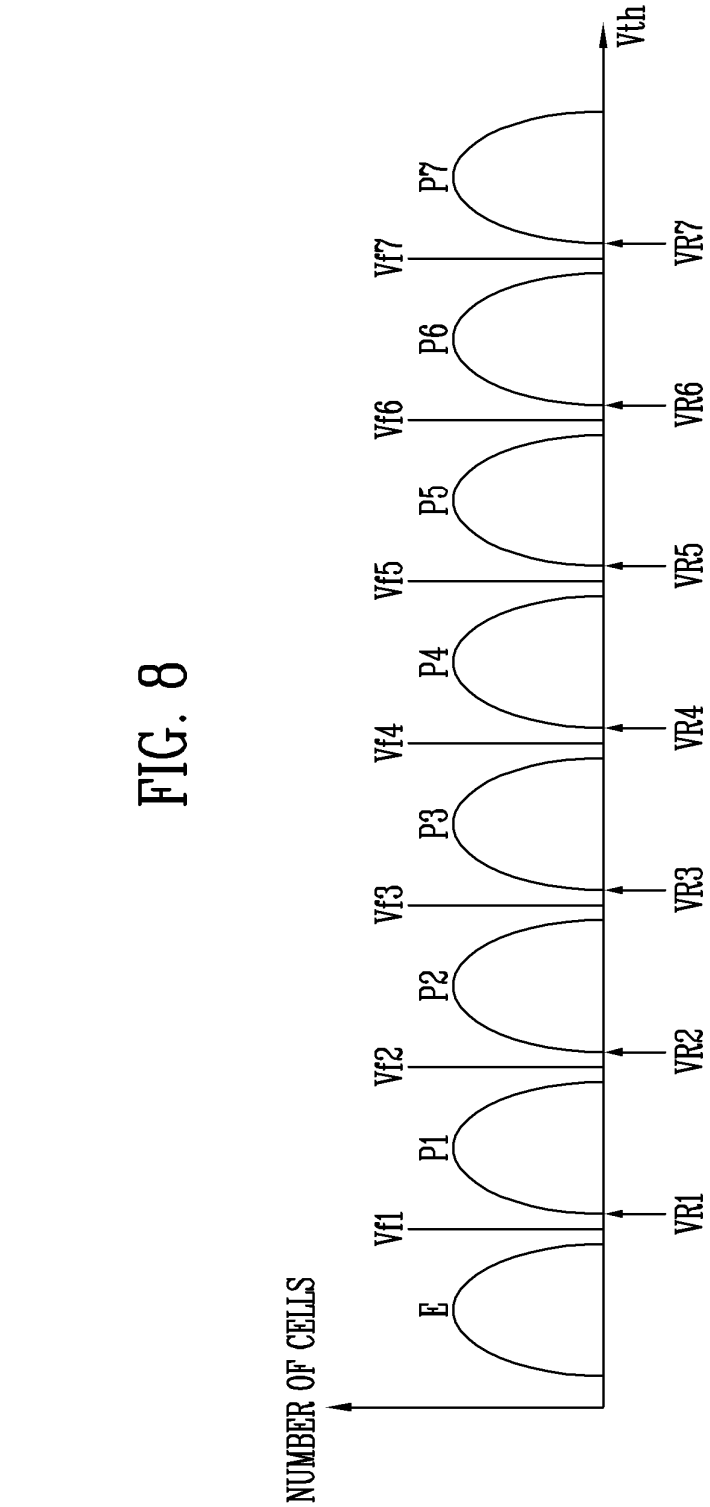

NUMBER OF CELLS
Vth
E
P1
P2
P3
P4
P5
P6
P7
Vf1
Vf2
Vf3
Vf4
Vf5
Vf6
Vf7
VR1
VR2
VR3
VR4
VR5
VR6
VR7

FIG. 9

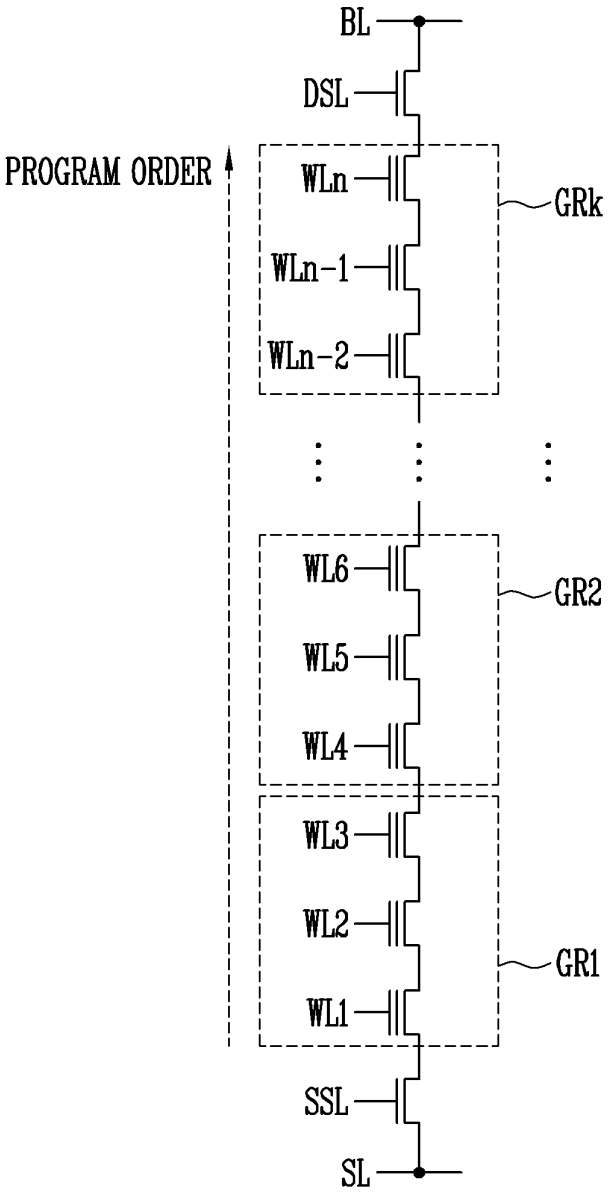

BL
DSL
PROGRAM ORDER
WLn
WLn-1
WLn-2
GRk
WL6
WL5
WL4
GR2
WL3
WL2
WL1
GR1
SSL
SL

FIG. 10

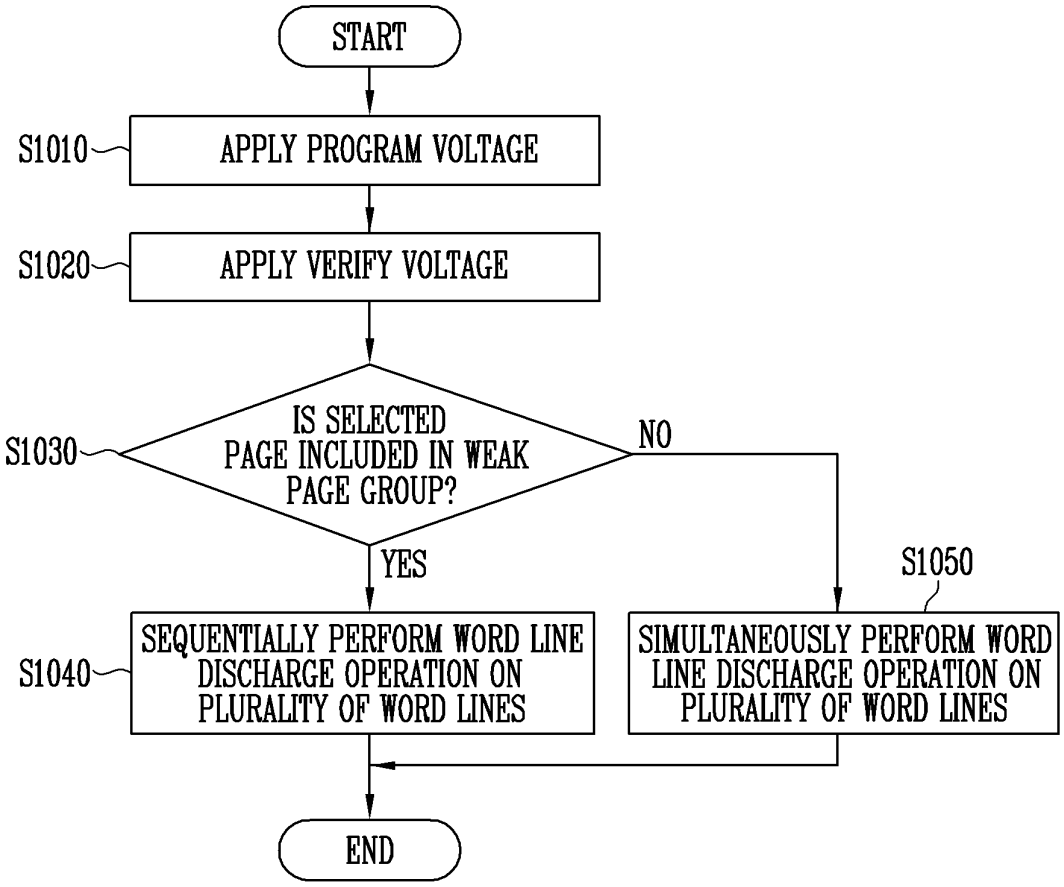

START
S1010
APPLY PROGRAM VOLTAGE
S1020
APPLY VERIFY VOLTAGE
S1030
IS SELECTED PAGE INCLUDED IN WEAK PAGE GROUP?
NO
YES
S1040
SEQUENTIALLY PERFORM WORD LINE DISCHARGE OPERATION ON PLURALITY OF WORD LINES
S1050
SIMULTANEOUSLY PERFORM WORD LINE DISCHARGE OPERATION ON PLURALITY OF WORD LINES
END

FIG. 11

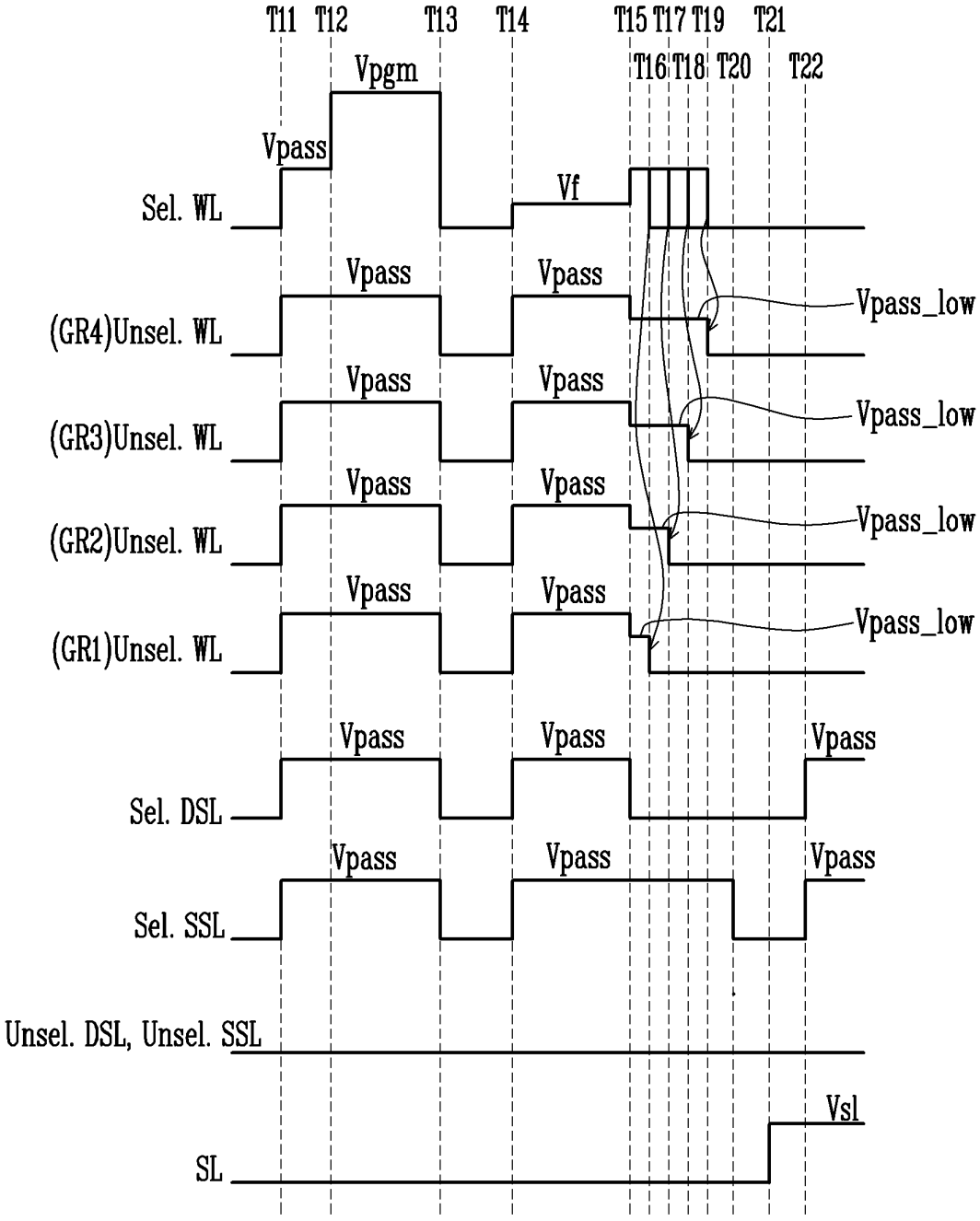

T11
T12
T13
T14
T15
T16
T17
T18
T19
T20
T21
T22
Vpgm
Vpass
Vf
Sel. WL
(GR4)Unsel. WL
(GR3)Unsel. WL
(GR2)Unsel. WL
(GR1)Unsel. WL
Vpass_low
Sel. DSL
Sel. SSL
Unsel. DSL, Unsel. SSL
Vsl
SL

FIG. 12

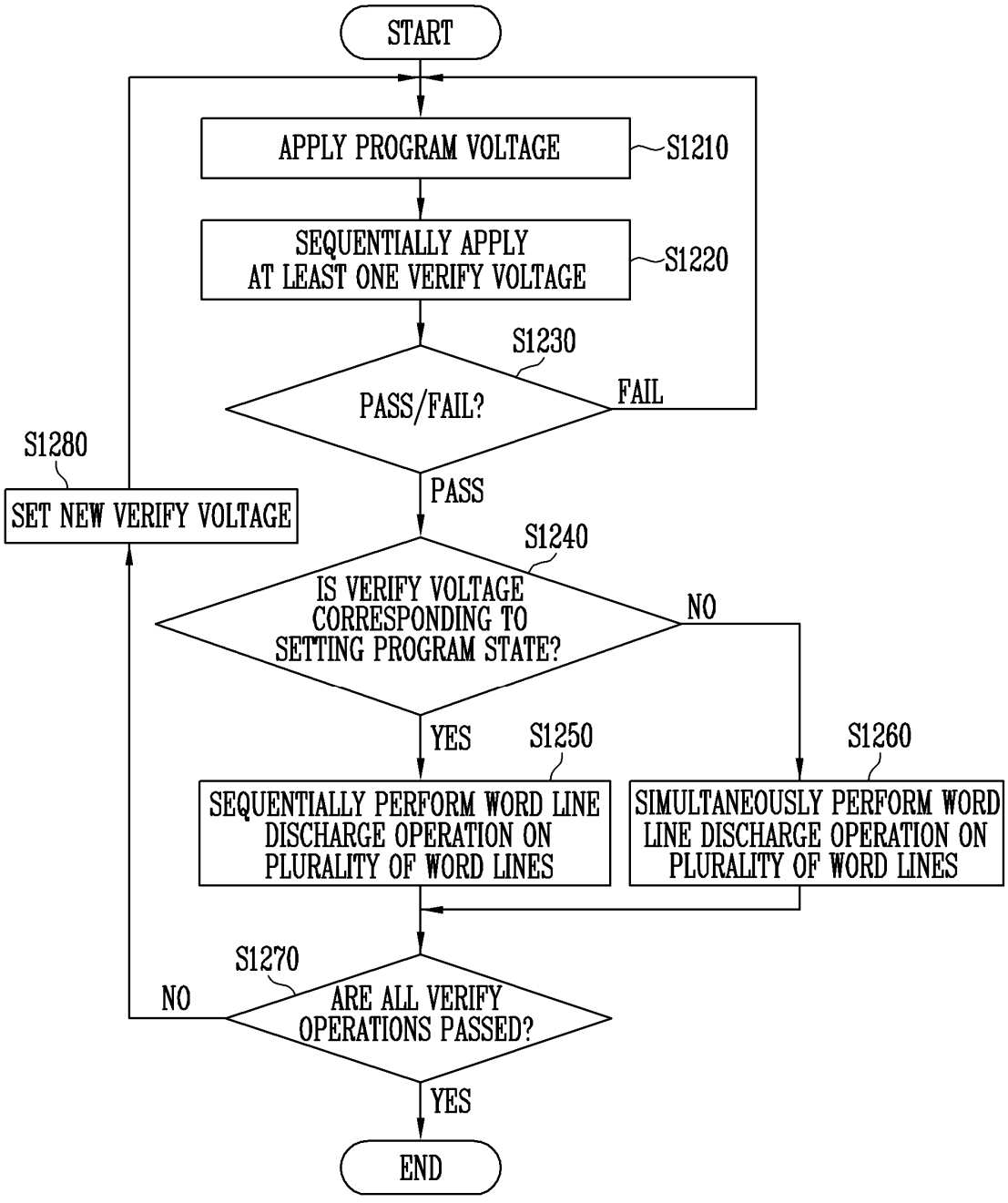

START
APPLY PROGRAM VOLTAGE
S1210
SEQUENTIALLY APPLY AT LEAST ONE VERIFY VOLTAGE
S1220
S1230
PASS/FAIL?
FAIL
PASS
S1280
SET NEW VERIFY VOLTAGE
S1240
IS VERIFY VOLTAGE CORRESPONDING TO SETTING PROGRAM STATE?
NO
YES
S1250
SEQUENTIALLY PERFORM WORD LINE DISCHARGE OPERATION ON PLURALITY OF WORD LINES
S1260
SIMULTANEOUSLY PERFORM WORD LINE DISCHARGE OPERATION ON PLURALITY OF WORD LINES
S1270
NO
ARE ALL VERIFY OPERATIONS PASSED?
YES
END

FIG. 13

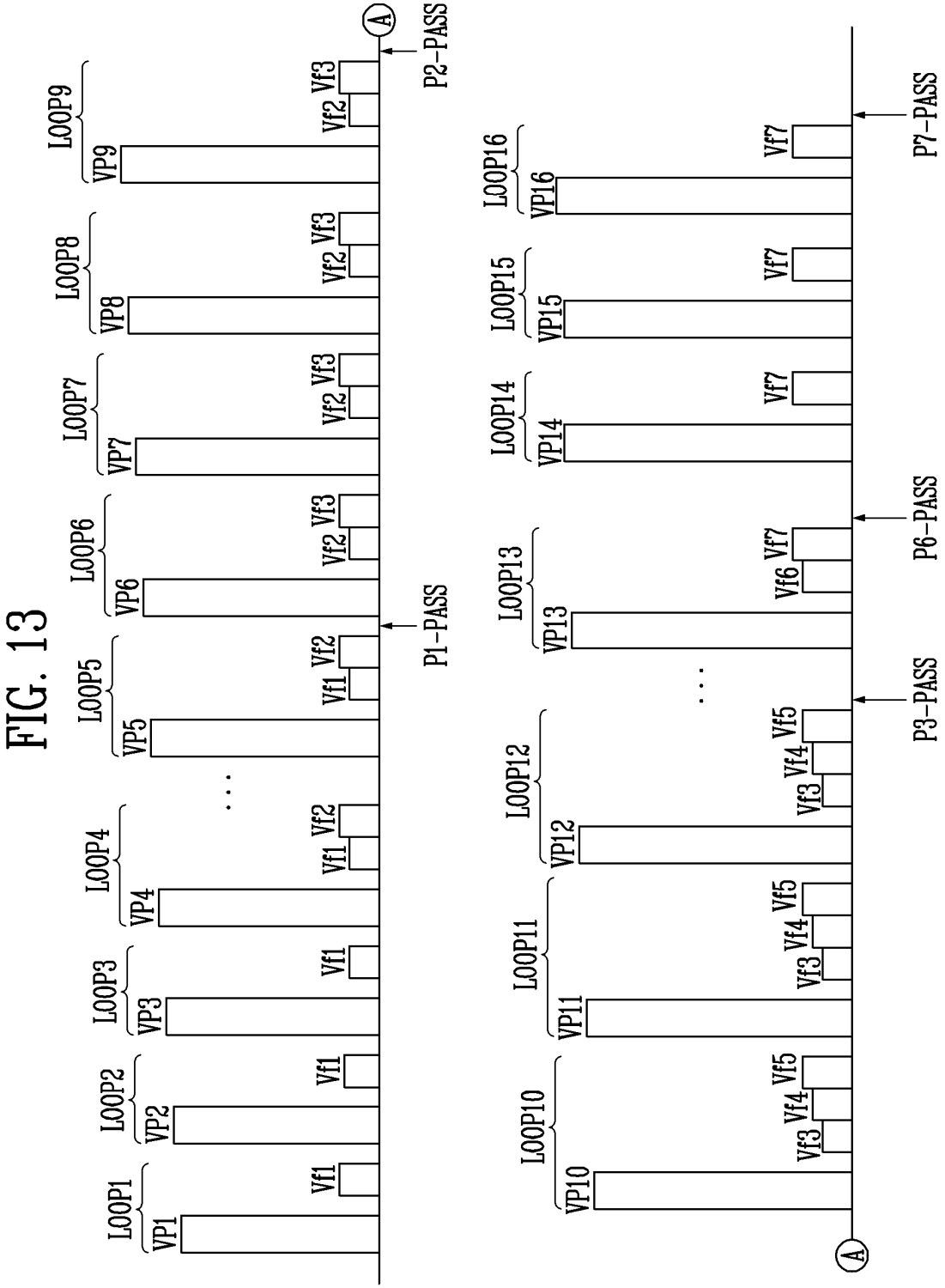

LOOP1
VP1
Vf1
LOOP2
VP2
Vf1
LOOP3
VP3
Vf1
LOOP4
VP4
Vf1
Vf2
LOOP5
VP5
Vf1
Vf2
P1-PASS
LOOP6
VP6
Vf2
Vf3
LOOP7
VP7
Vf2
Vf3
LOOP8
VP8
Vf2
Vf3
LOOP9
VP9
Vf2
Vf3
A
P2-PASS
LOOP10
VP10
Vf3
Vf4
Vf5
LOOP11
VP11
Vf3
Vf4
Vf5
LOOP12
VP12
Vf3
Vf4
Vf5
P3-PASS
LOOP13
VP13
Vf6
Vf7
P6-PASS
LOOP14
VP14
Vf7
LOOP15
VP15
Vf7
LOOP16
VP16
Vf7
P7-PASS
A

FIG. 14

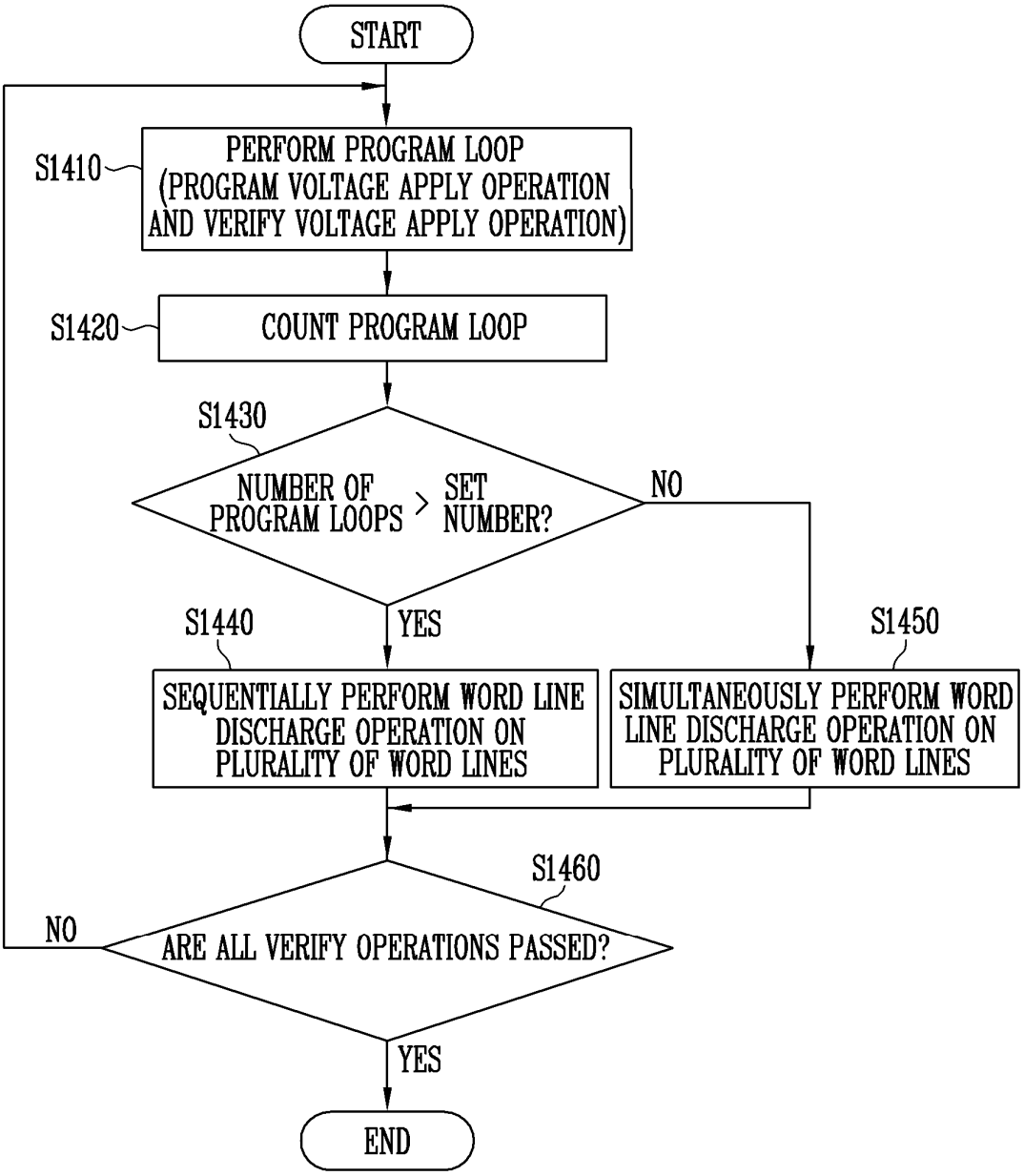

START
S1410
PERFORM PROGRAM LOOP (PROGRAM VOLTAGE APPLY OPERATION AND VERIFY VOLTAGE APPLY OPERATION)
S1420
COUNT PROGRAM LOOP
S1430
NUMBER OF PROGRAM LOOPS > SET NUMBER?
NO
YES
S1440
SEQUENTIALLY PERFORM WORD LINE DISCHARGE OPERATION ON PLURALITY OF WORD LINES
S1450
SIMULTANEOUSLY PERFORM WORD LINE DISCHARGE OPERATION ON PLURALITY OF WORD LINES
S1460
ARE ALL VERIFY OPERATIONS PASSED?
NO
YES
END

FIG. 15

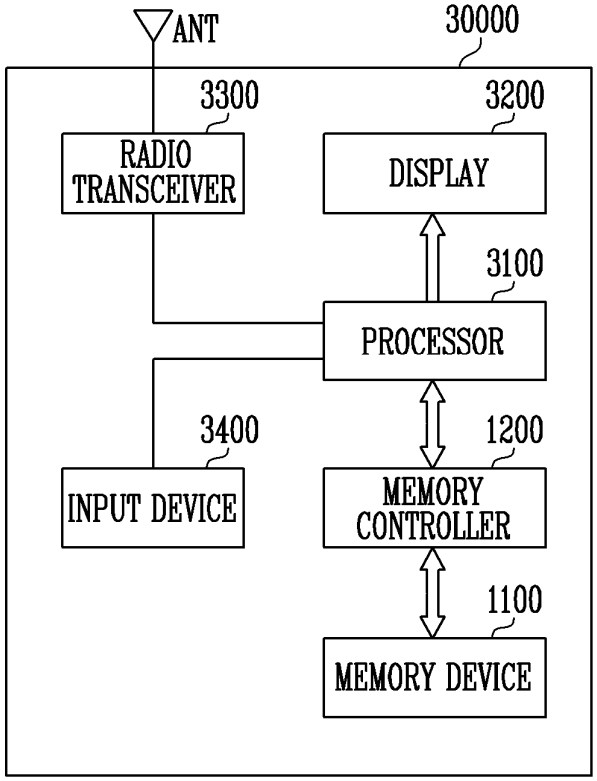

ANT
30000
3300
3200
RADIO TRANSCEIVER
DISPLAY
3100
PROCESSOR
3400
1200
INPUT DEVICE
MEMORY CONTROLLER
1100
MEMORY DEVICE

FIG. 16

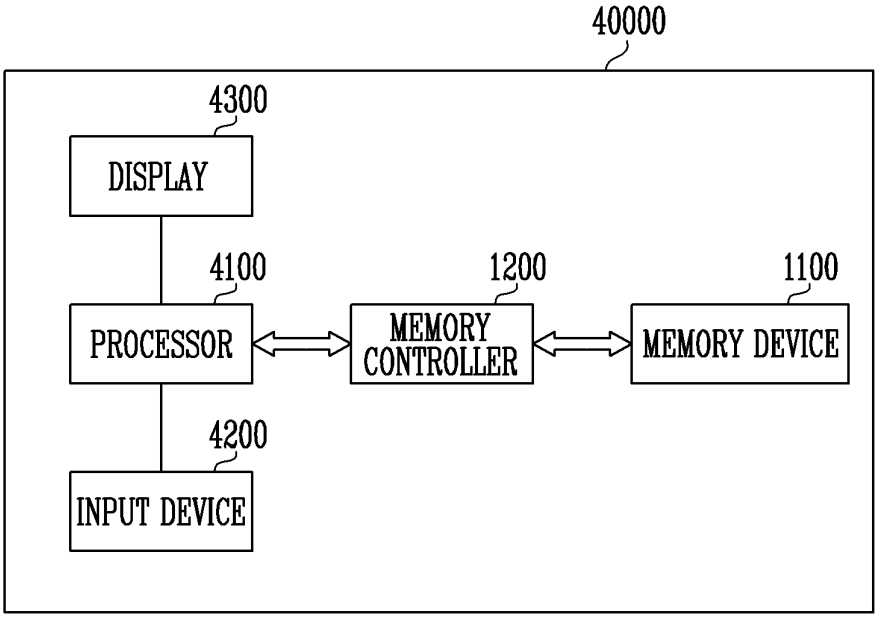

40000
4300
DISPLAY
4100
1200
1100
PROCESSOR
MEMORY CONTROLLER
MEMORY DEVICE
4200
INPUT DEVICE

FIG. 17

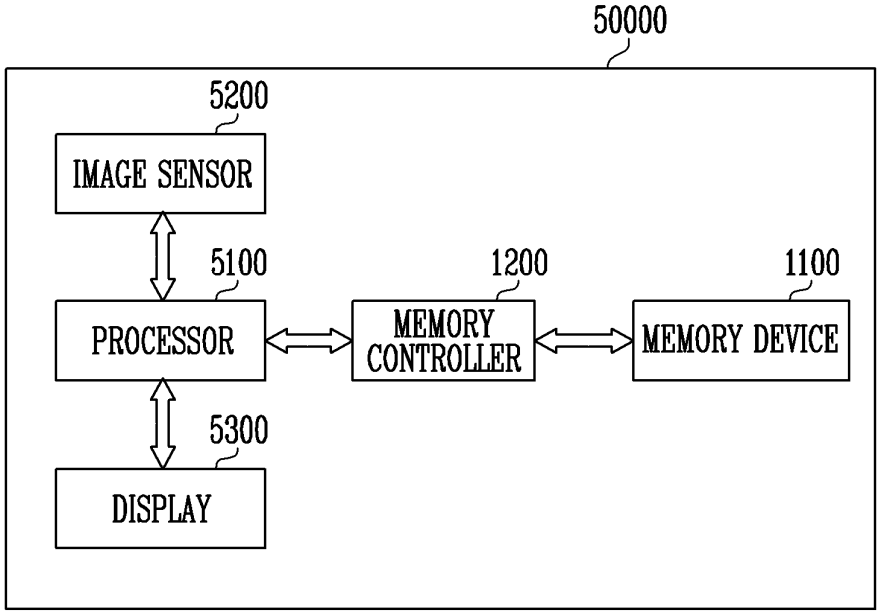
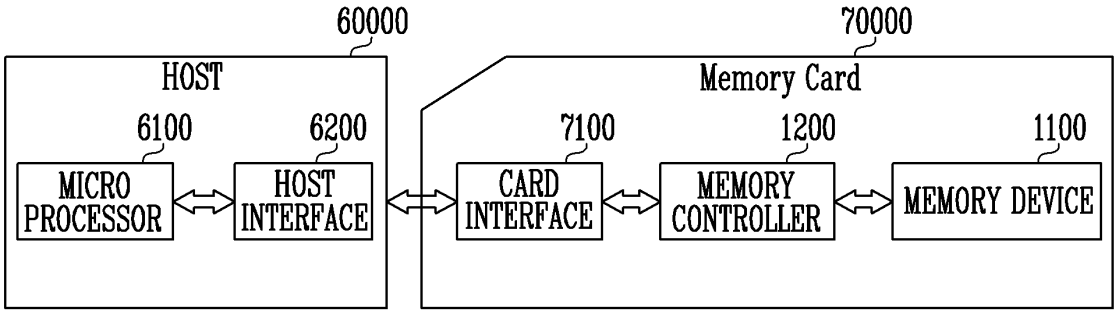

50000
5200
IMAGE SENSOR
5100
PROCESSOR
1200
MEMORY CONTROLLER
1100
MEMORY DEVICE
5300
DISPLAY

FIG. 18


60000
HOST
6100
MICRO PROCESSOR
6200
HOST INTERFACE
70000
Memory Card
7100
CARD INTERFACE
1200
MEMORY CONTROLLER
1100
MEMORY DEVICE