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(71) Applicant (for all designated States except US): **APPLIED MATERIALS** [US/US]; Legal Department, P.O. Box 450A, Santa Clara, CA 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **ARGHAVANI, Reza** [US/US]; 192 Twin Pines Drive, Scotts Valley, CA 95066 (US). **YEH, Ellie** [US/US]; 5888 Pistola Way, San Jose, CA 95138 (US). **M'SAAD, Hichem** [TN/US]; 3500 Granada Ave #364, Santa Clara, CA 95051 (US).

(74) Agent: **JANAH, Ashok**; Janah & Associates, PC, 650 De-lancey Street, Suite 106, San Francisco, CA 94107 (US).

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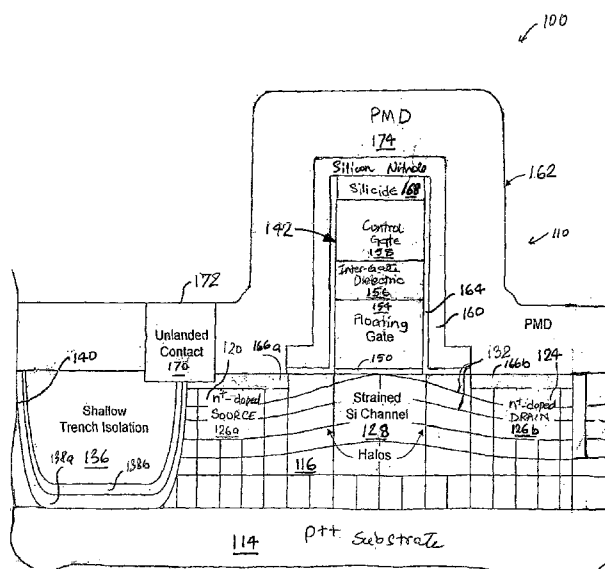
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(54) Title: MEMORY CELL HAVING STRESSED LAYERS



(57) Abstract: A memory cell comprises a p-doped substrate with a pair of spaced apart n-doped regions on the substrate that form a source and drain about the channel. A stack of layers on the channel comprises, in sequence, (i) a tunnel oxide layer, (ii) a floating gate, (iii) an inter-gate dielectric, and (iv) a control gate. A polysilicon layer is on the source and drain. A cover layer covering the stack of layers comprises a spacer layer and a pre-metal-deposition layer. Optionally, contacts are used to contact each of the source, drain, and suicide layers, and each have exposed portions. A shallow isolation trench is provided about n-doped regions, the trench comprising a stressed silicon oxide layer having a tensile stress of at least about 200 MPa. The stressed layer reduces leakage of charge held in the floating gate during operation of the memory cell.



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