FIG. 1

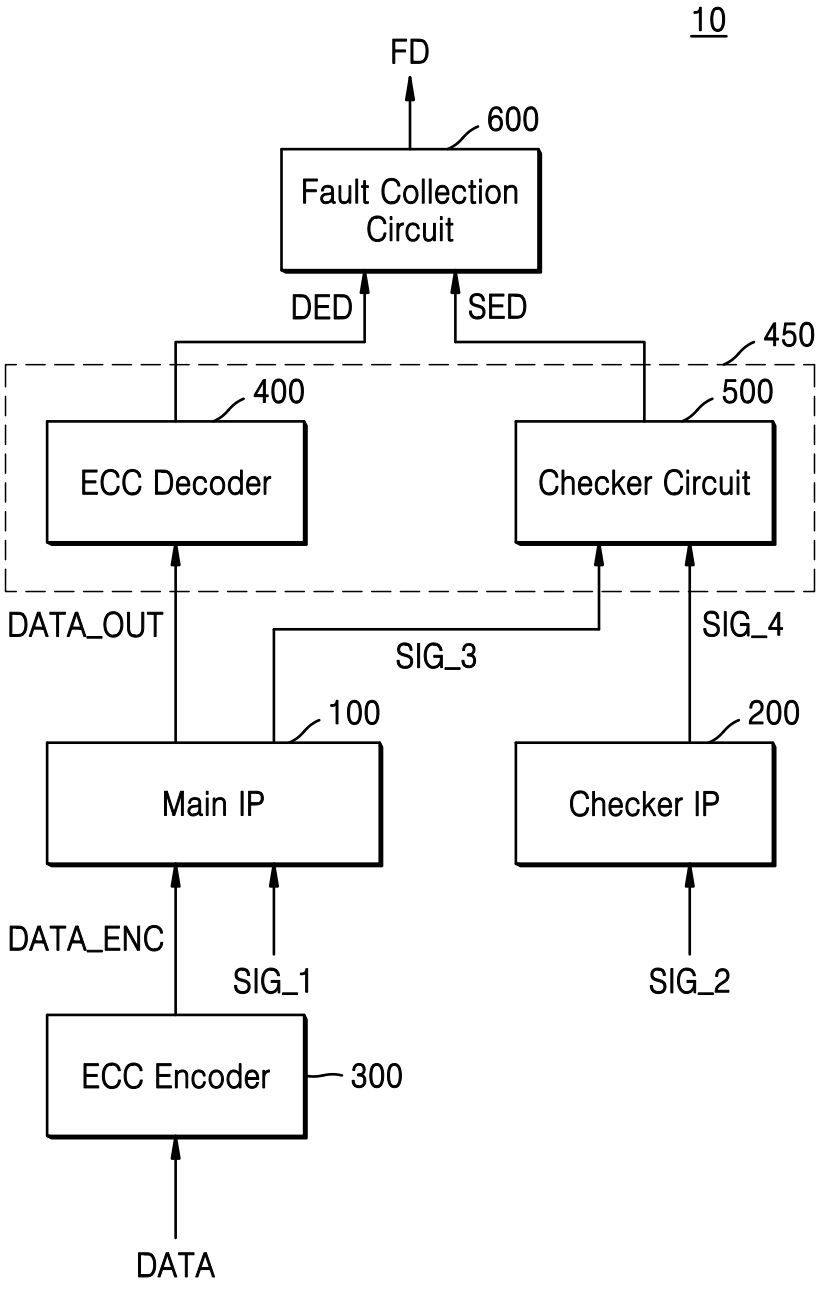

10
FD
600
Fault Collection Circuit
DED
SED
450
400
500
ECC Decoder
Checker Circuit
DATA_OUT
SIG_3
SIG_4
100
200
Main IP
Checker IP
DATA_ENC
SIG_1
SIG_2
ECC Encoder
300
DATA

FIG. 2

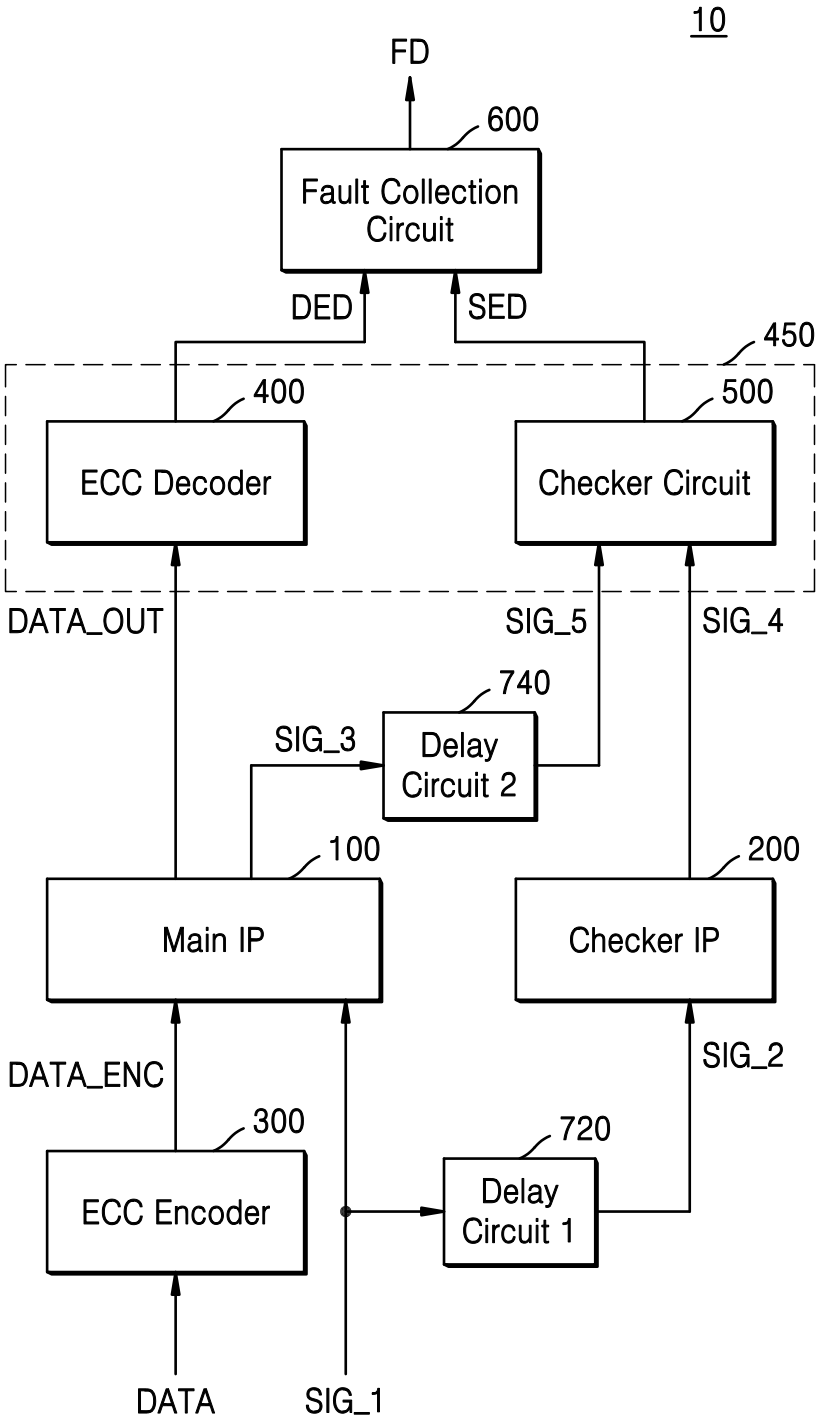

10
FD
600
Fault Collection Circuit
DED
SED
450
400
500
ECC Decoder
Checker Circuit
DATA_OUT
SIG_5
SIG_4
740
SIG_3
Delay Circuit 2
100
200
Main IP
Checker IP
DATA_ENC
SIG_2
300
720
ECC Encoder
Delay Circuit 1
DATA
SIG_1

FIG. 3

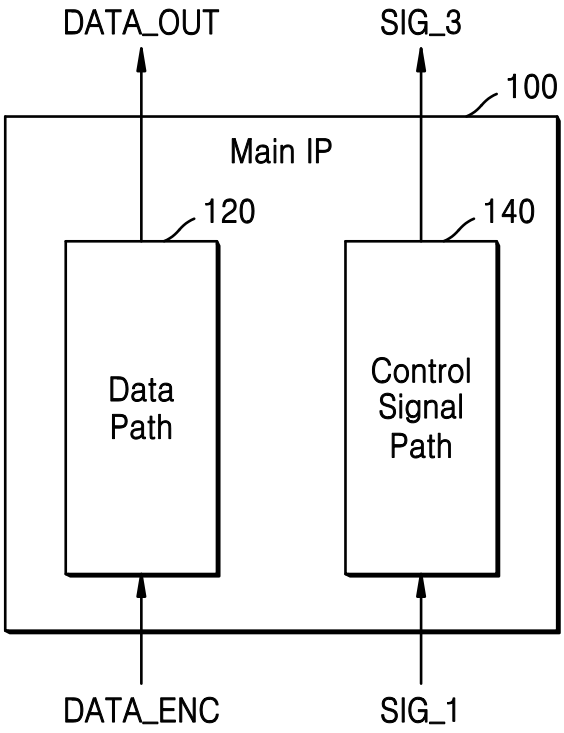

DATA_OUT
SIG_3
100
Main IP
120
140
Data Path
Control Signal Path
DATA_ENC
SIG_1

FIG. 4

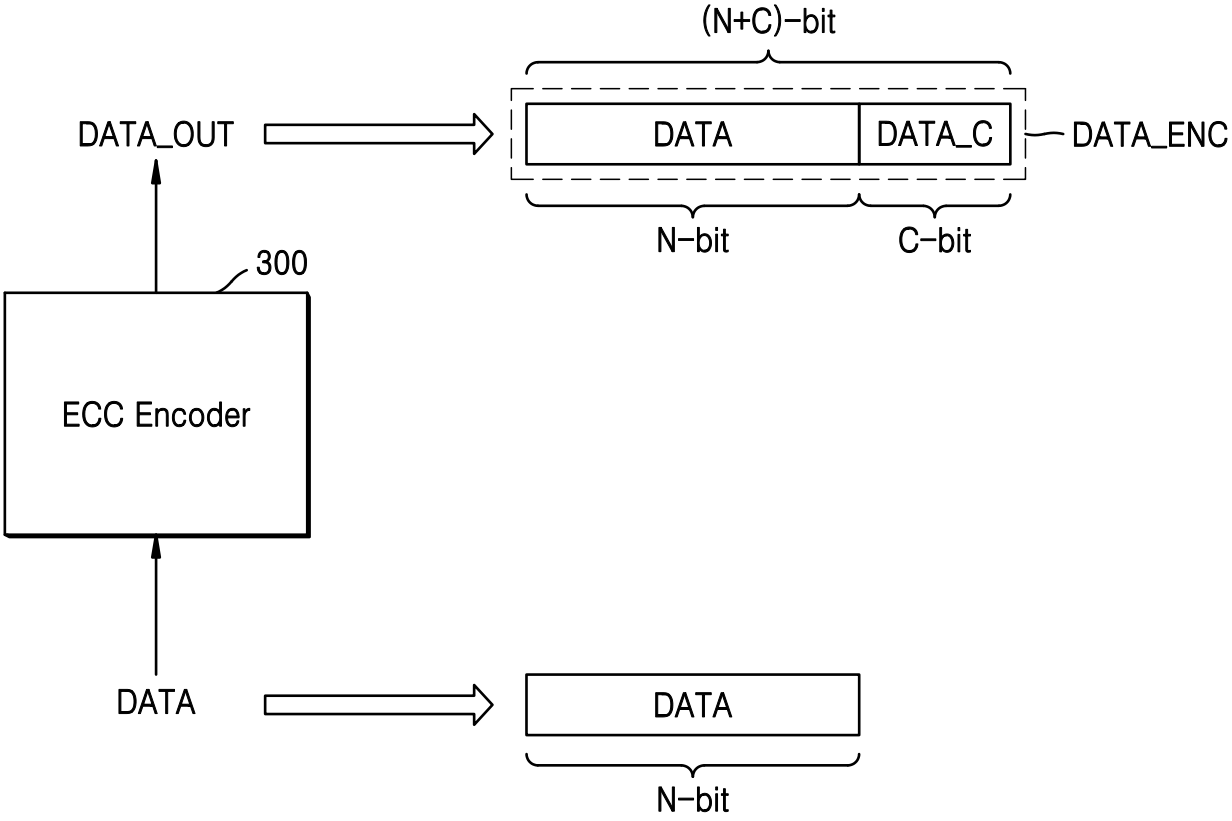

(N+C)-bit
DATA_OUT
DATA
DATA_C
DATA_ENC
N-bit
C-bit
300
ECC Encoder
DATA
DATA
N-bit

FIG. 5

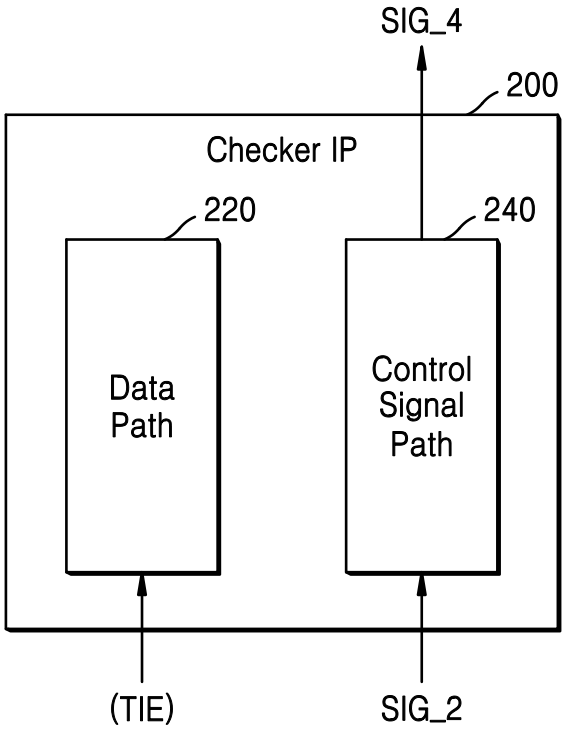

SIG_4
200
Checker IP
220
240
Data Path
Control Signal Path
(TIE)
SIG_2

FIG. 6

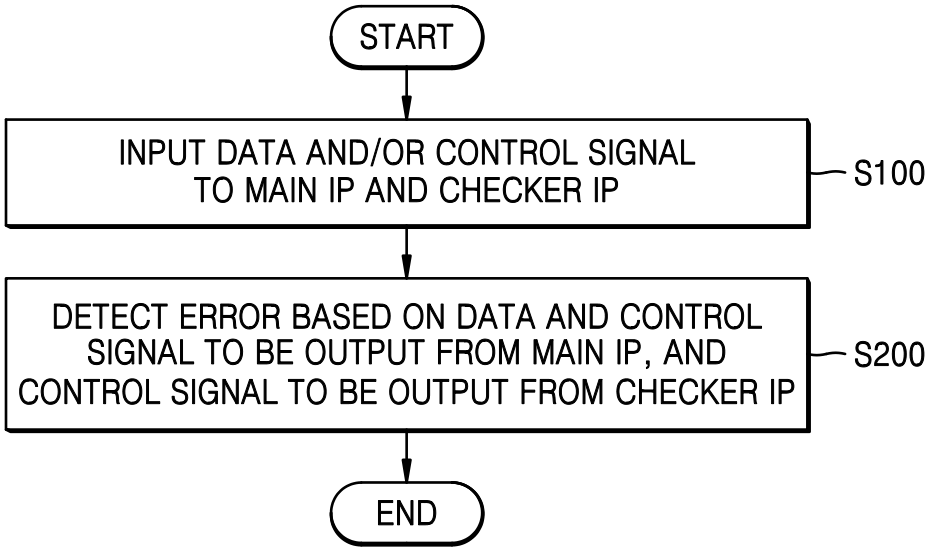

START
INPUT DATA AND/OR CONTROL SIGNAL TO MAIN IP AND CHECKER IP
S100
DETECT ERROR BASED ON DATA AND CONTROL SIGNAL TO BE OUTPUT FROM MAIN IP, AND CONTROL SIGNAL TO BE OUTPUT FROM CHECKER IP
S200
END

FIG. 7

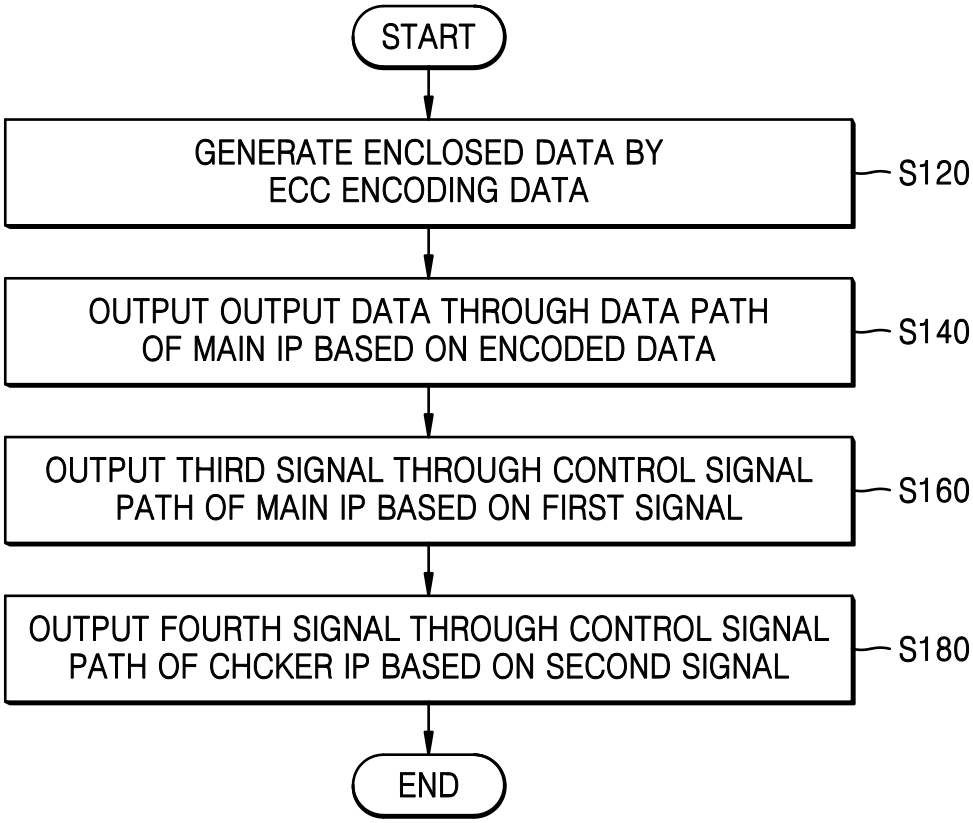

START
GENERATE ENCLOSED DATA BY ECC ENCODING DATA
S120
OUTPUT OUTPUT DATA THROUGH DATA PATH OF MAIN IP BASED ON ENCODED DATA
S140
OUTPUT THIRD SIGNAL THROUGH CONTROL SIGNAL PATH OF MAIN IP BASED ON FIRST SIGNAL
S160
OUTPUT FOURTH SIGNAL THROUGH CONTROL SIGNAL PATH OF CHCKER IP BASED ON SECOND SIGNAL
S180
END

FIG. 8

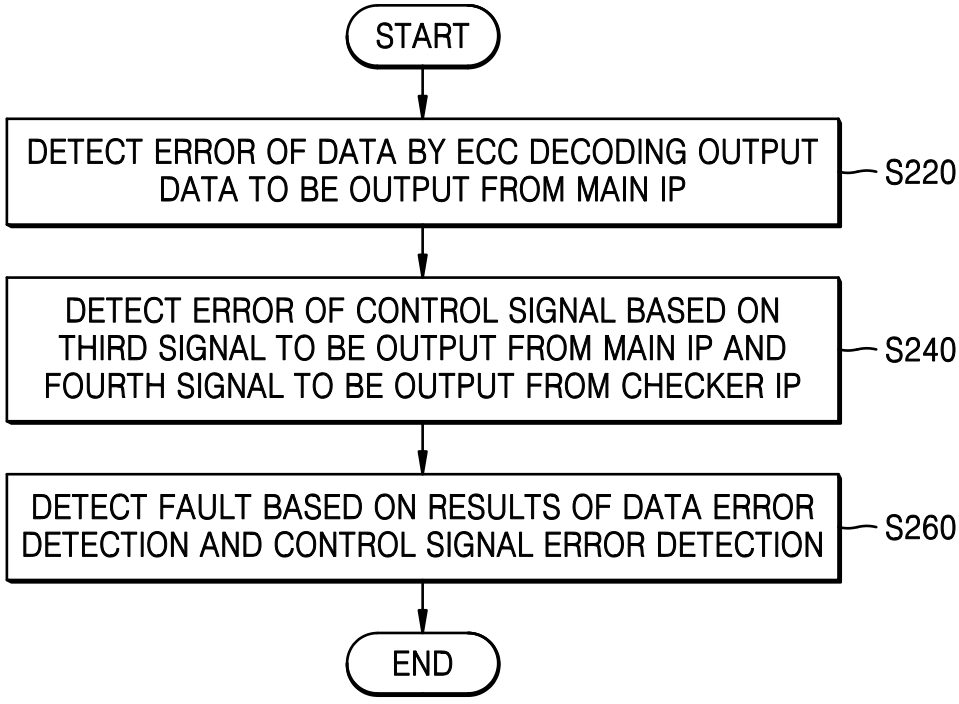

START
DETECT ERROR OF DATA BY ECC DECODING OUTPUT DATA TO BE OUTPUT FROM MAIN IP
S220
DETECT ERROR OF CONTROL SIGNAL BASED ON THIRD SIGNAL TO BE OUTPUT FROM MAIN IP AND FOURTH SIGNAL TO BE OUTPUT FROM CHECKER IP
S240
DETECT FAULT BASED ON RESULTS OF DATA ERROR DETECTION AND CONTROL SIGNAL ERROR DETECTION
S260
END

FIG. 9

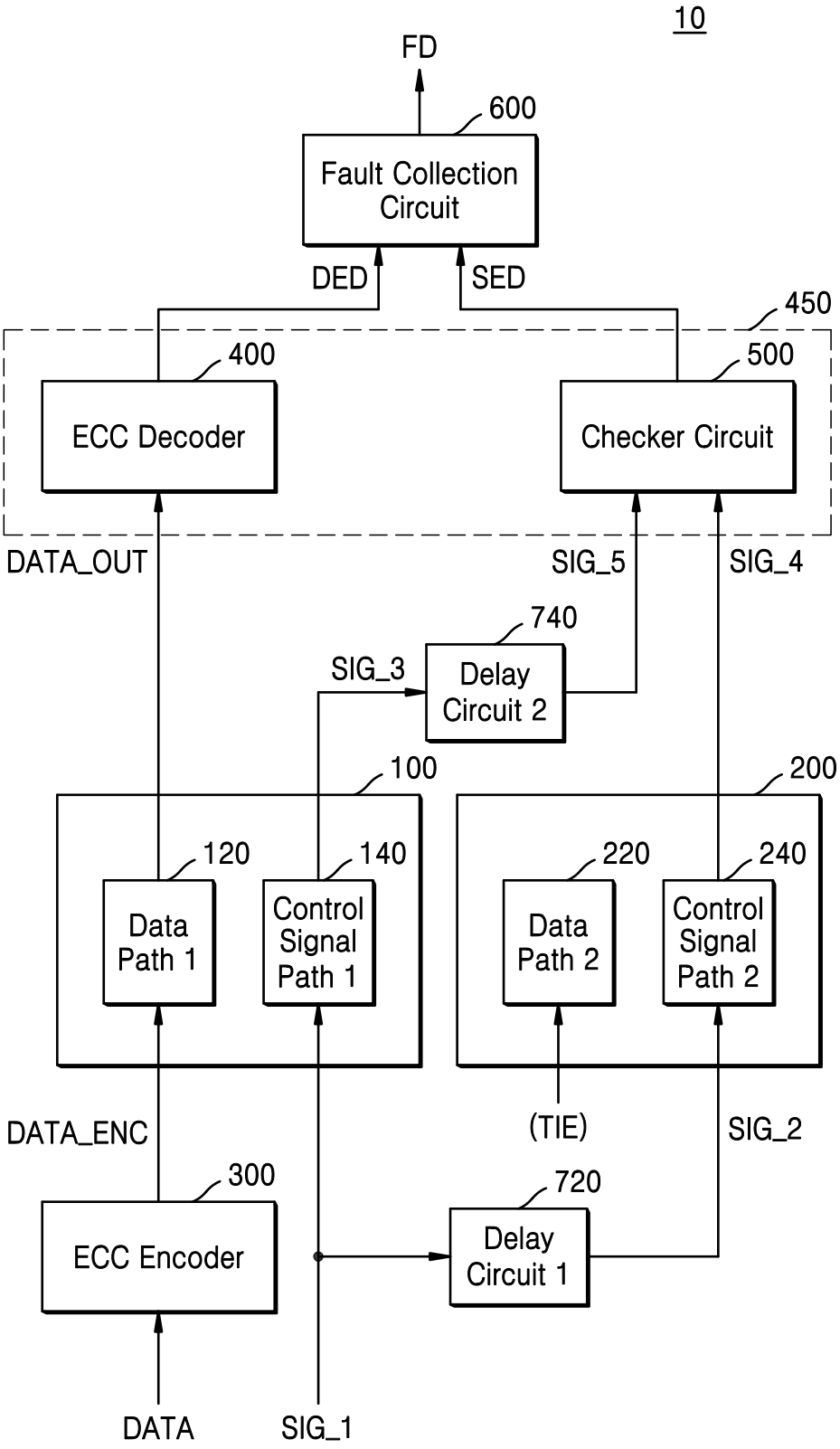

10
FD
600
Fault Collection Circuit
DED
SED
450
400
ECC Decoder
500
Checker Circuit
DATA_OUT
SIG_5
SIG_4
740
SIG_3
Delay Circuit 2
100
200
120
140
Data Path 1
Control Signal Path 1
220
240
Data Path 2
Control Signal Path 2
DATA_ENC
(TIE)
SIG_2
300
720
ECC Encoder
Delay Circuit 1
DATA
SIG_1

FIG. 10

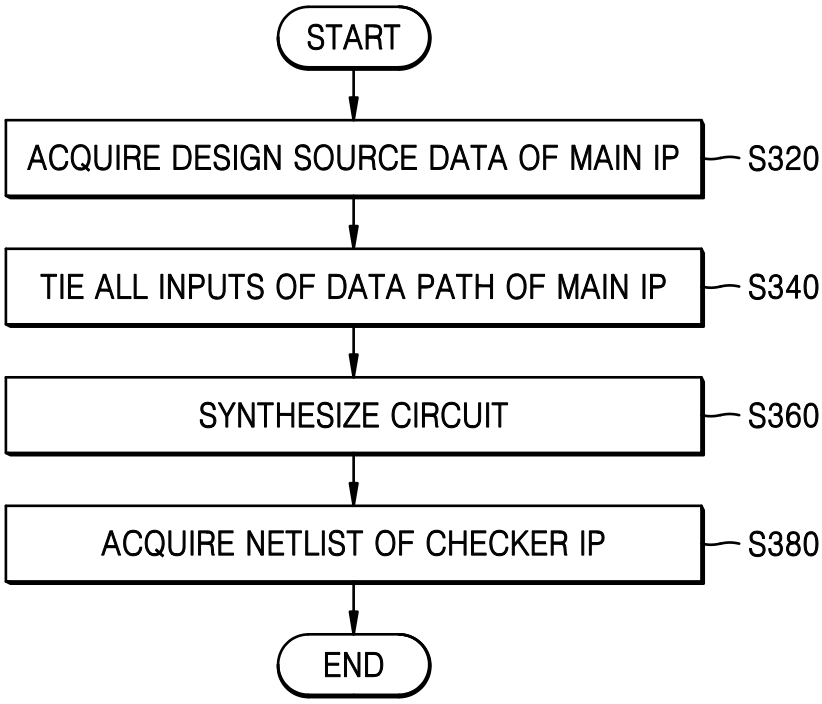

START
ACQUIRE DESIGN SOURCE DATA OF MAIN IP
S320
TIE ALL INPUTS OF DATA PATH OF MAIN IP
S340
SYNTHESIZE CIRCUIT
S360
ACQUIRE NETLIST OF CHECKER IP
S380
END

FIG. 11

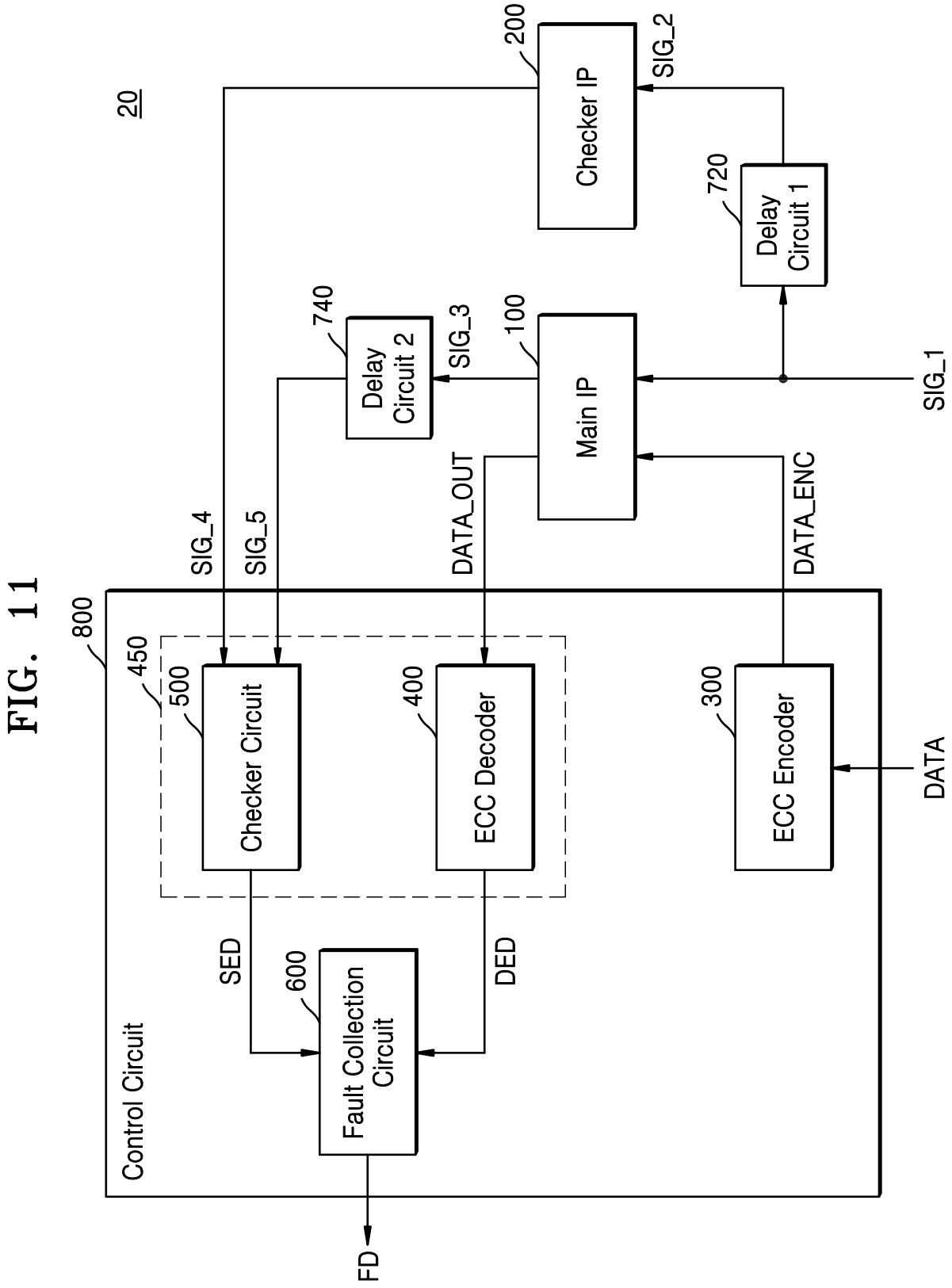

20
200
Checker IP
SIG_2
720
Delay Circuit 1
740
Delay Circuit 2
SIG_3
100
Main IP
SIG_1
SIG_4
SIG_5
DATA_OUT
DATA_ENC
800
450
500
Checker Circuit
400
ECC Decoder
300
ECC Encoder
DATA
SED
600
Fault Collection Circuit
DED
Control Circuit
FD

FIG. 12

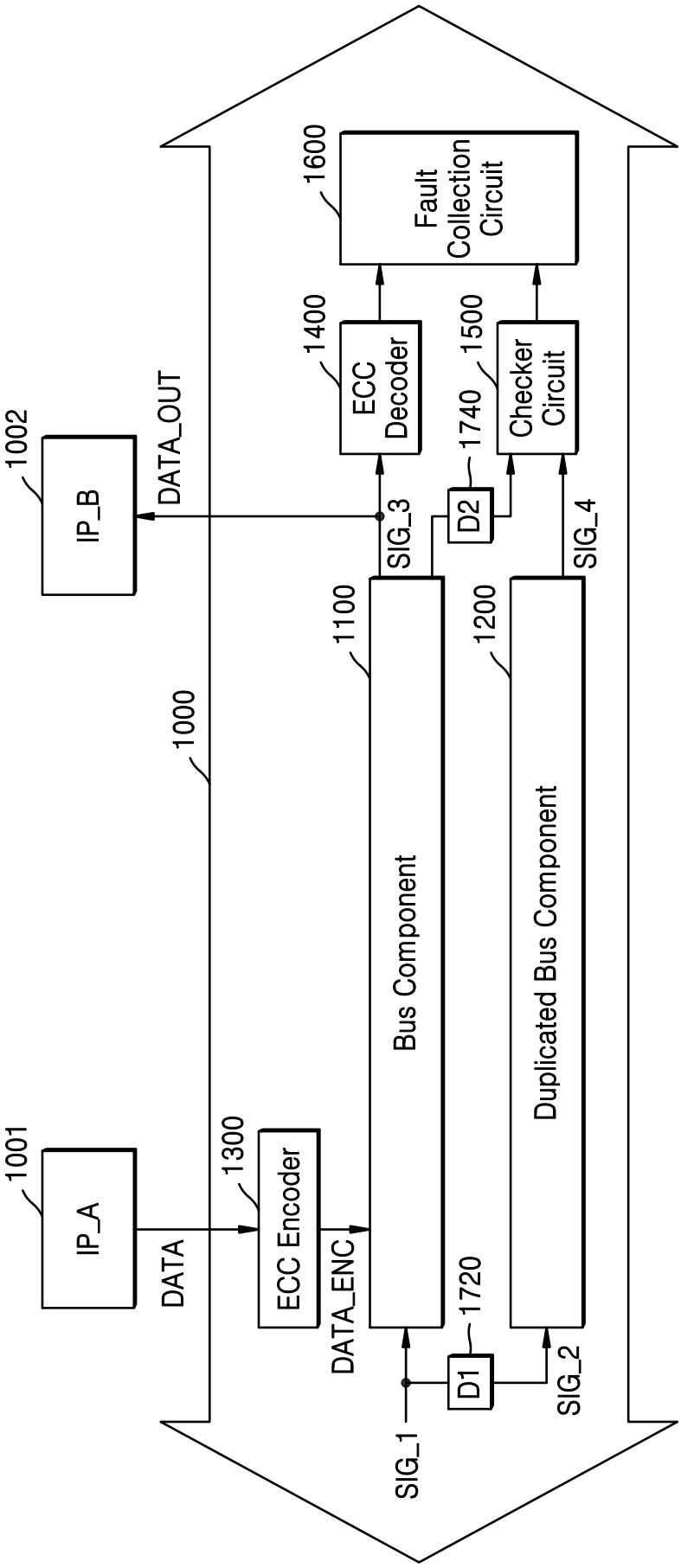
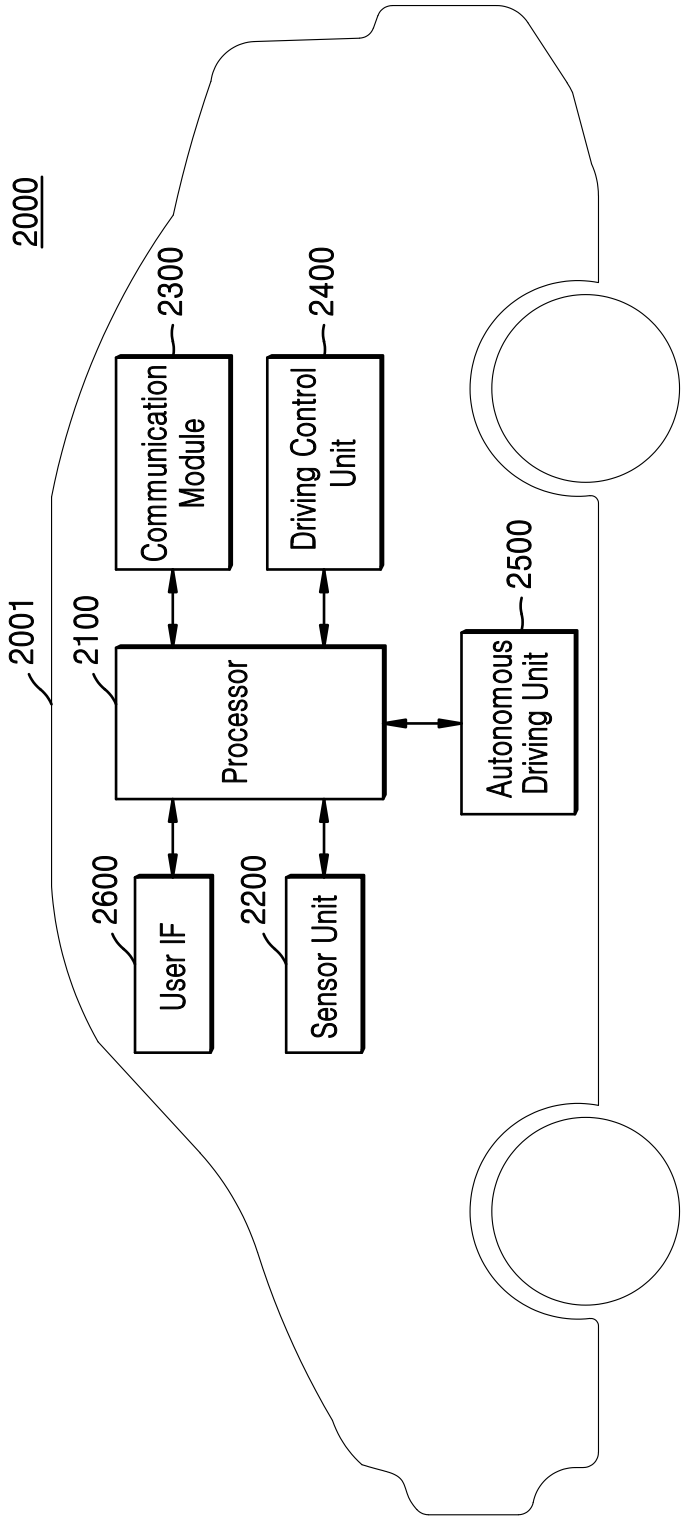

1000
1001
IP_A
DATA
1300
ECC Encoder
DATA_ENC
1100
Bus Component
1200
Duplicated Bus Component
1002
IP_B
DATA_OUT
1400
ECC Decoder
1500
Checker Circuit
1600
Fault Collection Circuit
SIG_1
SIG_2
SIG_3
SIG_4
D1
1720
D2
1740

FIG. 13


2000
2001
2100
Processor
2300
Communication Module
2400
Driving Control Unit
2500
Autonomous Driving Unit
2600
User IF
2200
Sensor Unit