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(54) IMPROVEMENTS IN OR RELATING TO INFORMATION STORAGE DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to information storage devices and more particularly to so-called "charge coupled devices" (CCD's), in which mobile electric charge representing information is stored and moved in a suitable storage medium by application of electric fields.

Previously proposed forms of such devices e.g., the three-phase form described in U.K. copending patent application no. 21832/71 (Serial No. 1340619) and the two-phase form described in copending patent application no. 21833/71 (Serial No. 1340620) possess certain disadvantages.

For example, the three-phase form cannot readily be provided with a serpentine data pattern without an unduly complicated interconnection pattern. Such a pattern, whilst not difficult to fabricate, does require an appreciable amount of space, and the result is an often unacceptably large area per bit of information.

The two-phase form can readily be provided with a serpentine data pattern but this form of device can be difficult to fabricate. Also, the built-in asymmetry in such a device precludes the possibility of electronically reversing the direction of data transfer.

According to this invention an information storage device includes a storage medium in which electric charge is storeable and moveable in response to an appropriate electric field, and means for providing, when energized, said electric field, said means comprising a succession of pairs of electrodes overlying and insulated from a surface of said medium, a second electrode of each of said pairs being insulated from and disposed partly between and partly overlapping first electrodes of that pair and the next adjacent pair of electrodes in said succession.

Because the insulation thickness between each second electrode and the first electrodes it overlaps can be small, fabrication of very closely spaced electrodes is possible. This is especially advantageous because very closely spaced electrodes, e.g., about 1000 Å separation, are desirable if optimum performance is to be obtained in a charge coupled device.

The overlapping of electrodes results in a device in which all portions of the information channel are covered by one or more electrodes and thus the channel is effectively sealed from contamination which otherwise might deleteriously affect it.

The first electrodes of alternate pairs of electrodes may be interconnected, the second electrodes of alternate pairs of electrodes may be interconnected, the first electrodes of the intervening pairs of electrodes may be interconnected, and the second electrodes of the intervening pairs of electrodes may be interconnected. There may be provided means for applying four phase voltage, each phase being connected to a respective group of interconnected electrodes. Alternatively there may be provided means for applying a d.c. voltage between the first and second electrodes of each of said pairs of electrodes, and means for applying two-phase voltage one phase to each alternate pair of electrodes and the other phase to each intervening pair of electrodes.

The four-phase mode e.g. by applying sinusoidal or other periodic voltages differing by one-fourth cycle, e.g., by 90 degrees, simultaneously to the electrodes yields greatest operational flexibility and highest speed operation because greatest advantage can be taken of field-enhanced charge transfer.

[Price 25p]

In the two-phase mode the d.c. voltage is adjusted to provide the requisite asymmetry to the potential wells to ensure unidirectionality of charge transfer. The direction of charge transfer can be charged simply by reversing the polarity of the d.c. voltage.

The capacitive coupling between first and second electrodes in each of said pairs of electrodes may be greater than that between the first electrode in that pair and the second electrode adjacent thereto in an adjacent pair of electrodes. There may be provided means for applying two-phase voltage one phase to one electrode in each alternate pair of electrodes, and the other phase to the corresponding one electrode in each intervening pair of electrodes. Preferably said greater capacitive coupling is provided by an overlap between the first and second electrodes of each of said pairs of electrodes greater than that between the first electrode in that pair and the second electrode adjacent thereto in an adjacent pair of electrodes.

The two-phase voltage applied e.g. to the second electrodes, causes voltages of lesser magnitude to be induced on the first electrodes because of the capacitive coupling there-between. (The induced voltage is of lesser magnitude than the applied voltage because of capacitive voltage division between the interelectrode capacitance and the capacitance of the first electrode with respect to the surface of the storage medium.) Because the induced voltage is less than the applied voltage, the resulting asymmetry in the potential wells under each pair of electrodes causes the direction of charge transfer to be, in this case, from the first electrodes toward the second electrodes.

The invention will now be described with reference to the accompanying drawings, in which:

Fig. 1 is a cross-sectional view taken along the channel of a charge coupled device in accordance with the invention;

Fig. 2 is a plan view of a device of which Fig. 1 is substantially a cross-section;

Fig. 3 is a cross-sectional view similar to Fig. 1 but showing capacitive and resistive coupling between each pair of electrodes;

Fig. 4 is a plan view of another device in accordance with the invention adapted to operate as described with reference to Fig. 3; and

Figs. 5 and 6 show first and second level metallization patterns which are shown superposed in Fig. 7 to provide a serpentine data pattern.

It will be appreciated that for simplicity and clarity the figures have not necessarily been drawn to scale.

With reference now to Fig. 1, the device shown includes a bulk portion 11 which for purposes of illustration only, is shown as N-type semiconductor. As will be appreciated from U.K. copending patent application no. 21832/71 (Serial No. 1340619), the bulk portion 11 may be selected from a wide variety of suitable storage media, such as, for example, semiconductors, semi-insulators, and insulators.

A first insulating layer 12 overlies the storage medium 11. Layer 12 advantageously is a dual-thickness layer which is relatively thin, e.g., 1000 Å, over the channel shown in the cross-section, and relatively thick outside the channel area so that voltages applied to conduction paths and other overlay contacts outside the channel area do not substantially perturb the surface potential of the storage medium outside the intended channel. Overlying layer 12 are a plurality of spaced electrodes designated 13, followed by an alphabetic subscript *a, b, c, d,* etc. Overlying each electrode 13 is a second insulating coating 14 which may be formed in situ by oxidizing electrodes 13 or may be deposited, as desired.

Disposed primarily between but partially overlapping electrodes 13 are a second plurality of electrodes 15, similarly designated, and which constitute a second level of metallization.

In the following discussion, the electrodes of the above-described device will often be considered in pairs, each pair including one electrode, e.g., 13a of the first level of metallization, and the next adjacent electrode, e.g., 15a of the second level of metallization. This terminology is convenient because of the symmetries involved.

It will be appreciated that the device can be fabricated in a variety of ways. For example, so-called "silicon gate" technology, (see U.S. Patent No. 3,475,234) can be used. In this case, the first level of "metallization" (electrodes 13) is formed by depositing a layer of silicon, defining the silicon into electrode geometries by a photolithographic process, oxidizing the remaining silicon electrodes, depositing a layer of a suitable metal such as platinum, palladium, gold, or aluminum, and photolithographically defining this second layer of metallization into the geometric patterns desired for electrodes 15.

Alternatively, a so-called "film-forming" metal, such as the oxidizable metals tungsten, zirconium, aluminum, hafnium, molybdenum, or nickel, may be substituted for silicon for the first layer of metallization. Still another alternative which may be employed is to use any suitably conductive material instead of silicon for the first level of metallization and then to deposit, e.g. by sputtering, an insulating coating thereover rather than to form the insulating coating by chemical conversion.

It will be appreciated that the overlapping of electrodes illustrated in Fig. 1 is an important feature of the invention because

it results in a device in which all portions of the information channel are covered by one or more electrodes. In this manner the channel is effectively sealed from contamination otherwise could penetrate the insulating coatings and deleteriously affect the device.

The above-described device can be operated in a four-phase mode using four electrodes (two pairs) per bit by applying sinusoidal or periodic voltages differing by one-fourth cycle successively to every fourth electrode.

This is depicted schematically in Fig. 1 where every fourth electrode is shown connected to a common one of four conduction paths 16—19. Application of four-phase clock voltages ϕ_1—ϕ_4 to these conduction paths in a manner similar to that described in U.K. copending patent application no. 21832/71 (Serial No. 1340619), for three-phase applications results in a travelling potential minimum within the storage medium 11 to which mobile charges can be coupled for storing and transferring information. Clearly the four-phase mode yields great operational flexibility and high speed operation because the direction of charge transfer can be reversed merely by changing the applied clock potentials and because greatest advantage can be taken of field-enhanced charge transfer.

Because of the repetitive symmetries involved, the four-phase clock voltages advantageously are applied through two pairs of conduction paths disposed one pair on either side of the channel. This is illustrated by the plan view shown in Fig. 2. The cross-sectional view shown in Fig. 1 is substantially that which would be seen in a cross-section taken on line 1′—1′ in Fig. 2.

In Fig. 2, the information channel is between parallel broken lines 21 and 22 where a relatively thin insulating layer, e.g., 1000 Å of silicon oxide, overlies and is contiguous with the surface of a storage medium 11.

Outside the channel, a thicker insulating layer 12, e.g., 10,000 Å of silicon oxide or silicon nitride, overlies and is contiguous with the rest of the surface of the storage medium, these outlying portions being thicker to prevent voltages applied to the conduction paths from substantially perturbing the surface potential of the storage medium outside the channel.

Over this dual-thickness insulating coating, two conduction paths 13′ and 13″, constituting a first level of metallization, are disposed one on either side of the channel. Conduction 13′ and 13″ include interdigitated rectangular portions 13a, 13b, 13c, 13d, and 13e which extend over the channel and serve as field plate electrodes. Electrodes 13a, 13c, and 13e are a part of conduction path 13″; electrodes 13b and 13d are a part of conduction path 13′.

A second insulating coating is disposed over at least the electrodes of the first level of metallization; and two other conduction paths 15′ and 15″, constituting a second level of metallization, are disposed one on either side of the channel over conduction paths 13′ and 13″, respectively. Conduction paths 15′ and 15″ also include interdigitated rectangular portions, 15a—15e, which extend over the channel and serve as field plate electrodes. Electrodes 15a, 15c, and 15e are a part of conduction path 15′; electrodes 15b and 15d are a part of conduction path 15″.

In four-phase operation, phase one (ϕ_1) is applied to conduction path 13″; phase two (ϕ_2) is applied to conduction path 15′; phase three (ϕ_3) is applied to conduction path 13′; and phase four (ϕ_4) is applied to conduction path 15″.

An important feature of the conduction path arrangement shown in Fig. 2 is that the conduction path (15″) for phase four overlies the conduction path (13″) for phase one, and the conduction path (15′) for phase two overlies the conduction path (13′) for phase three. Whether conduction path 15″ overlies 13″ or vice versa is not important. What is important is the parasitic capacitive coupling resulting from the illustrated juxtaposition. In structures where silicon or any other material exhibiting substantial resistance is used for the first level of metallization, e.g., conduction paths 13′ and 13″, the series resistance may be 100 ohms/square or higher. Because of this resistance and the distributed capacitive coupling to the storage medium, such conduction paths act as transmission lines and thus can substantially retard the phase of signals thereon. However, because ϕ_4 is 90 degrees ahead of ϕ_1 and because ϕ_2 is 90 degrees ahead of ϕ_3, ϕ_4 will tend to advance the phase of ϕ_1 if their conduction paths are capacitively coupled, and ϕ_2 will tend to advance the phase of ϕ_3 if their conduction paths are capacitively coupled. This phase-advancing effect can be used to compensate for the phase-retarding effect of resistive conduction paths. This happens in the device of Fig. 2.

To avoid the complications inherent in generating, synchronizing, and transmitting four-phase clockpulses, the devices depicted in Figs. 1 and 2 can also be operated with a two-phase clock simply by providing, in addition to the two-phase clock signals, a DC offset voltage to the conduction paths so as to create a corresponding DC offset voltage between the first and second electrodes of each pair. In this case, the clock voltages, phase one and phase two, are alternately applied to pairs of the four conduction paths so that each of said pairs of electrodes is driven by the same clock phase at the same time. The function of the DC offset

voltage is to provide the requisite asymmetry to the potential wells to ensure unidirectionality of charge transfer.

Thus with reference to Fig. 1, for two-phase operation a DC voltage could be applied between conduction paths 16 and 17 and between conduction paths 18 and 19 so as to make electrodes 15 all positive (or all negative) with respect to electrodes 13. Clock phase one then would be applied to conduction paths 16 and 17 simultaneously, and clock phase two would be applied to conduction paths 18 and 19 simultaneously. At the next clock cycle, phase one would be applied to conduction paths 18 and 19 simultaneously, and phase two would be applied to 16 and 17 simultaneously. In this way information would advance two electrodes to the left (or right, depending on the polarity of the DC offset voltage) at each reversal of the clock.

Inasmuch as the direction of charge transfer is dependent on the polarity of the DC offset voltage, the direction can be reversed electronically simply by reversing the polarity of that voltage. And, of course, it will be appreciated that the DC offset voltage need not be applied between lines 16 and 17 and between lines 18 and 19, but may as well be applied between lines 17 and 18 and between 16 and 19, in which case the clock phases would be applied simultaneously to the newly-paired lines, i.e., to 17 and 18 and to 16 and 19.

If four conduction paths, or the four-phase clock, or the two-phase clock plus DC offset are considered a problem in any particular application, similar operating results can be obtained with a two-phase clock and two conduction paths per channel merely by providing capacitive and resistive coupling between the first and second electrodes of each pair.

This is illustrated schematically in Fig. 3 where elements 31a—31d represent capacitors, and elements 32a—32d represent resistors in parallel pairs with the capacitors coupling electrodes 13 to 15. Every other one of electrodes 15 is shown coupled to a common one of a pair of conduction paths 33 and 34 to which two-phase clock pulses ϕ_1 and ϕ_2 are applied.

In operation, two-phase clock voltages cause voltages of lesser magnitude to be induced on electrodes 13 because of the capacitive coupling. This induced voltage is of lesser magnitude than the clock voltages because of capacitive voltage division between the capacitors 21 and the capacitance of electrodes 13 with respect to the surface of storage medium 11. Because the voltage induced on electrodes 13 is of lesser magnitude than the voltages applied to electrodes 15, the surface potential under electrodes 13 is less than the surface potential induced under electrodes 15 for any given negative clock voltage.

Resistors 32 are included not for coupling voltage pulses from electrodes 15 to electrodes 13 but rather for "bleeding" charge from electrodes 13 to prevent charge from accumulating thereon. Consequently the resistance of resistors 32 should be much greater than the impedance of capacitors 31 and much less than the resistance of the insulator between electrodes 13 and the surface of storage medium 11 to prevent spurious discharge. For resistors 32, resistances between 10^5 and 10^{11} ohms, typically about 10^6—10^8 ohms, normally are appropriate. It will be appreciated, however, that although the exact resistance value is not critical the function which these resistors serve is important to prevent undue charge accumulation on electrodes 13.

Of course, it will be appreciated that these bleeder resistors need not be used in situations where spurious discharge and other effects of charge accumulation are not a problem. It will also be appreciated that it is not necessary to use a separate bleeder resistor between each pair of electrodes. Rather a plurality of electrodes 13 may be connected to a common conduction path and a single bleeder resistor can be connected between that conduction path and the conduction path to which a corresponding plurality of electrodes 15 are connected. More specifically, with reference to Fig. 3, since electrodes 15a and 15c are connected to a common conduction path 33, electrodes 13a and 13c can be connected to another conduction path (not shown) and then a bleeder resistor can be connected between conduction path 33 and the path to which electrodes 13a and 13c are connected.

In Fig. 3, broken line 35 represents schematically the surface potential (depth of the potential wells) adjacent the surface of storage medium 11. Where, as here, the storage medium is semiconductive, broken line 35 also may be considered as representing schematically the boundaries of depletion regions corresponding to the surface potential. It should be observed that because of the capacitive coupling between electrodes each of the combined potential wells under each pair of electrodes is asymmetrical in such a manner as to cause the preferred direction of positive charge transfer to be from the first electrode, e.g., 13a, of each pair toward the second electrode, 15a, of that pair.

With reference now to Fig. 4 there is shown a plan view of a portion of apparatus adapted to operate in the manner described with reference to Fig. 3. In Fig. 4, the information channel is between broken lines 41 and 42 where, as in Fig. 2, an insulating layer is disposed over the channel and is thinner than the rest thereof.

Over this dual-thickness insulating coating are disposed a plurality of localized elec-

trodes 43a—43f (indicated by broken line rectangles correspondingly labelled), constituting a first level of metallization.

A second insulating coating is disposed over at least the electrodes of the first level of metallization, and a pair of conduction paths, 44′ and 44″ are disposed one on either side of the channel. Conduction paths 44′ and 44″ include interdigitated rectangular portions 44a—44e which extend over the channel and serve as field plate electrodes. As can be seen, electrodes 44a, 44c, and 44e are a part of conduction path 44′, while electrodes 44b and 44d are a part of conduction path 44″.

In operation two-phase clock voltages are applied alternately (with respect to the storage medium) to conduction paths 44′ and 44″. One of electrodes 43 (of the first level of metallization) serves as the first electrode of each pair of electrodes, and one of electrodes 44 serves as the second electrode of each pair of electrodes.

To provide the capacitive coupling between the electrodes of each pair, each electrode 44 overlies the preceding electrode 43 more than it overlies the succeeding electrode 43. More specifically, electrode 44b overlies 43b more than it (electrode 44b) overlies 43c; electrode 44c overlies 43c more than 43d; etc. It will be appreciated that the amount of capacitive coupling between any given electrode 44 and any given electrode 43 is proportional to the area by which the one overlies the other.

In more detail now, consider electrodes 43a, 44a, 44b, and 43c. It is advantageous that electrode 44a overlaps 43a more than 43b, i.e., greater capacitive coupling to 43a than to 43b, so that a voltage of greater magnitude is induced on 43a than is induced on 43b. This tends to enhance the asymmetry in the potential wells so that unidirectionality of charge transfer also is enhanced. This asymmetry in the potential wells is also enhanced by the fact that the two electrodes 44 overlying any given electrode 43 are connected to opposite clock phases. For example, electrodes 44a and 44b both overlie electrode 43b, and electrode 44a is part of conduction path 44′ which is driven by one phase and electrode 44b is part of conduction path 44″ which is driven by the opposite phase. Because of this, the "net overlap", i.e., the amount by which the area of 44b's overlap exceeds the area of 44a's overlap, is important. The general rule of thumb is that as net overlap increases the difference between the surface potential under electrodes 43b and 44b decreases. By way of example, a net overlap area equal to about 20% of the total area of electrode 43 will be suitable in devices where the insulating layer between electrodes 43 and 44 is about 1000 Å of silicon oxide and where the two-phase clock voltages are pulses of −6 volts and −30 volts, respectively.

At least about 4 kT, i.e., about 0.1 volt, difference in surface potential, i.e., potential well asymmetry, between adjacent potential wells is required to provide desired directionality of charge transfer. In practice, however, for optimum operation this asymmetry advantageously is made about equal to one-half the difference between the peak-to-peak variations in surface potential between adjacent electrodes or electrode pairs. Thus, where applied clock voltages are −6 volts and −16 volts, a potential well asymmetry of about 5 volts (one-half the difference) is effective.

If sepentine data patterns are desired, the device of Fig. 4 may be modified to that shown in Figs. 5—7.

Figs. 5 and 6 depict, respectively, first level and second level metallization patterns which are combined with an insulating coating therebetween, as in the foregoing embodiments, and disposed over a dual-thickness insulating coating on a storage medium to achieve the apparatus depicted in Fig. 7. More specifically, geometric patterns 51a—51d in Fig. 5 are the electrode configurations used for the first level of metallization in Fig. 7, and geometric patterns 53a—53d are the electrode configurations used for the second level of metallization in Fig. 7. In Fig. 7 the electrode patterns are labelled to correspond with the patterns of Figs. 5 and 6.

Two information channels are depicted in Fig. 7, a first one lying between parallel broken lines 61 and 62 and a second one lying between parallel broken lines 63 and 64. It should be noted that in contradistinction to the foregoing embodiments, the electrode and conduction path metallizations, i.e., patterns 51a—51d and 53a—53d, are disposed transverse to the channels in Fig. 7, whereas in Figs. 2 and 4 the conduction path metallizations are disposed longitudinally with respect to the channels.

In Fig. 7 the stippled portions of the second level of metallization, i.e., of patterns 53a—53d, are those portions of those patterns which overlie some portion of the first level of metallization. It is, of course, these stippled overlap portions which provide the capacitive coupling desired for operation in a manner similar to that described with reference to Figs. 3 and 4.

In more detail now, note that with respect to the first channel (between lines 61 and 62), electrode 53a overlaps electrode 51a in stippled dumbbell-shaped portion 70a more than in (53a) overlaps electrode 51b (stippled hexagonal-shaped portion 71a). Similarly, the stippled dumbbell-shaped portion 70b by which electrode 53b overlaps electrode 51b is larger than the stippled hexagonal-shaped

portion 71b by which electrode 53b overlaps electrode 51c. In all cases, over the first channel (between lines 61 and 62) each electrode of the second level of metallization overlaps to the left more than it overlaps to the right. Accordingly, the net capacitive coupling is to the left, and so, as described with reference to Figs. 3 and 4, the direction of charge transfer is to the right in the first channel in Fig. 7.

With respect to the second channel (between lines 63 and 64), the stippled dumbbell-shaped overlap portion 81a by which electrode 53a overlaps electrode 51a is larger than the stippled hexagonal-shaped portion 80a by which electrode 53a overlaps the previous electrode (not labelled) of the first level of metallization. Similarly, the stippled dumbbell-shaped portion 81b by which electrode 53b overlaps electrode 51b is larger than the stippled hexagonal-shaped portion 80b by which electrode 53b overlaps electrode 51a. In all cases, over the second channel (between lines 63 and 64) each electrode of the second level of metallization overlaps to the right more than it overlaps to the left. Accordingly, the net capacitive coupling is to the right, and so the direction of charge transfer is to the left in the second channel.

It will be understood that application of two-phase clock voltages to electrodes 53 through clock lines 65 and 66 connected thereto causes information to advance to the right in the first channel and to the left in the second channel. This is a basic feature required for serpentine data flow.

Of course, the channels must be coupled together at the ends so that information at the end of one channel is coupled into the beginning of the next channel. Means for such coupling are indicated schematically in Fig. 7 by a Regeneration Means 90 with electrodes 91 and 92 extending toward the first and second channels, respectively.

Devices in accordance with the invention are in practice subject to some charge loss upon each charge transfer, and thus regenerating the signal while coupling to the next channel will be preferred in most digital applications. A variety of suitable regenerators are known, some of which are described in copending U.K. patent application no. 48499/71 (Serial No. 1344645).

It will be understood that the metallization patterns of Figs. 5—7 are not limited to use over two channels but may be extended in a similar fashion over many channels to provide information transfer in opposite directions in successive channels. Also, of course, devices such as shown in Fig. 4 and in Fig. 7 can be operated in a four-phase mode, if desired, by applying four-phase voltages to every electrode of both levels of metallization.

WHAT WE CLAIM IS:—

1. An information storage device including a storage medium in which electric charge is storeable and moveable in response to an appropriate electric field, and means for providing, when energized, said electric field, said means comprising a succession of pairs of electrodes overlying and insulated from a surface of said medium, a second electrode of each of said pairs being insulated from and disposed partly between and partly overlapping first electrodes of that pair and the next adjacent pair of electrodes in said succession.

2. A device as claimed in claim 1 wherein the first electrodes of alternate pairs of electrodes are interconnected, the second electrodes of alternate pairs of electrodes are interconnected, the first electrodes of the intervening pairs of electrodes are interconnected, and the second electrodes of the intervening pairs of electrodes are interconnected.

3. A device as claimed in claim 2 including means for applying four-phase voltage, each phase being connected to a respective group of interconnected electrodes.

4. A device as claimed in claim 2 including means for applying a d.c. voltage between the first and second electrodes of each of said pairs of electrodes, and means for applying two-phase voltage one phase to each alternate pair of electrodes and the other phase to each intervening pair of electrodes.

5. A device as claimed in claim 1 wherein the capacitive coupling between the first and second electrodes in each of said pairs of electrodes is greater than that between the first electrode in that pair and the second electrode adjacent thereto in an adjacent pair of electrodes.

6. A device as claimed in claim 5 including means for applying two-phase voltage one phase to one electrode in each alternate pair of electrodes, and the other phase to the corresponding one electrode in each intervening pair of electrodes.

7. A device as claimed in claim 5 or 6 wherein the said greater capacitive coupling is provided by an overlap between the first and second electrodes of each of said pairs of electrodes greater than that between the first electrode in that pair and the second electrode adjacent thereto in an adjacent pair of electrodes.

8. A device as claimed in any one preceding claim wherein said first electrodes are of silicon or film-forming metal.

9. A device as claimed in any one of claims 1 to 7 wherein said storage medium is silicon, said electrodes are insulated from said surface by a layer of silicon oxide, said first electrodes are of silicon or other oxidizable metal, and said second electrodes are insulated from

portion 71b by which electrode 53b overlaps electrode 51c. In all cases, over the first channel (between lines 61 and 62) each electrode of the second level of metallization overlaps to the left more than it overlaps to the right. Accordingly, the net capacitive coupling is to the left, and so, as described with reference to Figs. 3 and 4, the direction of charge transfer is to the right in the first channel in Fig. 7.

With respect to the second channel (between lines 63 and 64), the stippled dumbbell-shaped overlap portion 81a by which electrode 53a overlaps electrode 51a is larger than the stippled hexagonal-shaped portion 80a by which electrode 53a overlaps the previous electrode (not labelled) of the first level of metallization. Similarly, the stippled dumbbell-shaped portion 81b by which electrode 53b overlaps electrode 51b is larger than the stippled hexagonal-shaped portion 80b by which electrode 53b overlaps electrode 51a. In all cases, over the second channel (between lines 63 and 64) each electrode of the second level of metallization overlaps to the right more than it overlaps to the left. Accordingly, the net capacitive coupling is to the right, and so the direction of charge transfer is to the left in the second channel.

It will be understood that application of two-phase clock voltages to electrodes 53 through clock lines 65 and 66 connected thereto causes information to advance to the right in the first channel and to the left in the second channel. This is a basic feature required for serpentine data flow.

Of course, the channels must be coupled together at the ends so that information at the end of one channel is coupled into the beginning of the next channel. Means for such coupling are indicated schematically in Fig. 7 by a Regeneration Means 90 with electrodes 91 and 92 extending toward the first and second channels, respectively.

Devices in accordance with the invention are in practice subject to some charge loss upon each charge transfer, and thus regenerating the signal while coupling to the next channel will be preferred in most digital applications. A variety of suitable regenerators are known, some of which are described in copending U.K. patent application no. 48499/71 (Serial No. 1344645).

It will be understood that the metallization patterns of Figs. 5—7 are not limited to use over two channels but may be extended in a similar fashion over many channels to provide information transfer in opposite directions in successive channels. Also, of course, devices such as shown in Fig. 4 and in Fig. 7 can be operated in a four-phase mode, if desired, by applying four-phase voltages to every electrode of both levels of metallization.

WHAT WE CLAIM IS:—

1. An information storage device including a storage medium in which electric charge is storeable and moveable in response to an appropriate electric field, and means for providing, when energized, said electric field, said means comprising a succession of pairs of electrodes overlying and insulated from a surface of said medium, a second electrode of each of said pairs being insulated from and disposed partly between and partly overlapping first electrodes of that pair and the next adjacent pair of electrodes in said succession.

2. A device as claimed in claim 1 wherein the first electrodes of alternate pairs of electrodes are interconnected, the second electrodes of alternate pairs of electrodes are interconnected, the first electrodes of the intervening pairs of electrodes are interconnected, and the second electrodes of the intervening pairs of electrodes are interconnected.

3. A device as claimed in claim 2 including means for applying four-phase voltage, each phase being connected to a respective group of interconnected electrodes.

4. A device as claimed in claim 2 including means for applying a d.c. voltage between the first and second electrodes of each of said pairs of electrodes, and means for applying two-phase voltage one phase to each alternate pair of electrodes and the other phase to each intervening pair of electrodes.

5. A device as claimed in claim 1 wherein the capacitive coupling between the first and second electrodes in each of said pairs of electrodes is greater than that between the first electrode in that pair and the second electrode adjacent thereto in an adjacent pair of electrodes.

6. A device as claimed in claim 5 including means for applying two-phase voltage one phase to one electrode in each alternate pair of electrodes, and the other phase to the corresponding one electrode in each intervening pair of electrodes.

7. A device as claimed in claim 5 or 6 wherein the said greater capacitive coupling is provided by an overlap between the first and second electrodes of each of said pairs of electrodes greater than that between the first electrode in that pair and the second electrode adjacent thereto in an adjacent pair of electrodes.

8. A device as claimed in any one preceding claim wherein said first electrodes are of silicon or film-forming metal.

9. A device as claimed in any one of claims 1 to 7 wherein said storage medium is silicon, said electrodes are insulated from said surface by a layer of silicon oxide, said first electrodes are of silicon or other oxidizable metal, and said second electrodes are insulated from

said first electrodes by silicon oxide or an oxide of said other oxidizable metal respectively.

10. A device as claimed in any one of claims 1 to 8 wherein said storage medium is an insulator, a semi-insulator or a semiconductor.

11. Information storage devices substantially as herein described with reference to the accompanying drawings.

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